100+ GHz Transistor Electronics: Present and Projected Capabilities

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THz Transistors
Why Build THz Transistors?

- THz amplifiers → THz radios
- → imaging, sensing, communications

500 GHz digital logic → fiber optics

- precision analog design at microwave frequencies → high-performance receivers
- Higher-Resolution Microwave ADCs, DACs, DDSs

Transistor Power Gain, dB

Frequency, Hz
Transistor figures of Merit / Cutoff Frequencies

$H_{21} = \text{short-circuit current gain}$

$MAG = \text{maximum available power gain: impedance-matched}$

$U = \text{unilateral power gain: feedback nulled, impedance-matched}$
What Determines Digital Gate Delay?

\[ T_{gate} \approx \tau_f + \frac{\Delta V_L}{I_C} \left( C_{je} + 6C_{cbx} + 6C_{cbi} + C_{wire} \right) \\
+ \left( \frac{kT}{qI_C} \right) \left( 0.5C_{je} + C_{cbx} + C_{cbi} + 0.5\tau_f \frac{I_C}{\Delta V_L} \right) \\
+ R_{ex} \left( 0.5C_{cbx} + 0.5C_{cbi} + 0.5\tau_f \frac{I_C}{\Delta V_L} \right) \\
+ R_{bb} \left( 0.5C_{je} + C_{cbi} + 0.5\tau_f \frac{I_C}{\Delta V_L} \right). \]

\[ \leftarrow \text{CV/I terms dominate} \]

analog ICs have somewhat similar bandwidth considerations...
How to Make THz Transistors
High-Speed Transistor Design

Depletion Layers

\[ C = \varepsilon \cdot \frac{A}{T} \]

\[ \tau = \frac{T}{2v} \]

\[ I_{\text{max}} = \frac{4\varepsilon v_{\text{sat}} (V_{\text{appl}} + \phi)}{A T^2} \]

Bulk and Contact Resistances

\[ R \approx \rho_{\text{contact}} / A \quad \text{contact terms dominate} \]

Fringing Capacitances

\[ C_{\text{fing}} / L \sim \varepsilon \]

Thermal Resistance

\[ R_{\text{th}} \approx \frac{1}{\pi K_{\text{th}} L} \ln \left( \frac{L}{W} \right) + \frac{1}{\pi K_{\text{th}} L} \]
Frequency Limits and Scaling Laws of (most) Electron Devices

$\tau \propto \text{thickness}$

$C \propto \text{area} / \text{thickness}$

$R_{top} \propto \rho_{contact} / \text{area}$

$R_{bottom} \propto \frac{\rho_{contact}}{\text{area}} + \frac{\rho_{\text{sheet}}}{4} \cdot \frac{\text{width}}{\text{length}}$

$I_{\text{max, space-charge-limit}} \propto \text{area} / (\text{thickness})^2$

$\Delta T \propto \frac{\text{power}}{\text{length}} \times \log\left(\frac{\text{length}}{\text{width}}\right)$

To double bandwidth,

- reduce thicknesses 2:1
- Improve contacts 4:1
- reduce width 4:1, keep constant length
- increase current density 4:1
Changes required to double transistor bandwidth

<table>
<thead>
<tr>
<th>HBT parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter &amp; collector junction widths</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density (mA/μm²)</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>current density (mA/μm)</td>
<td>constant</td>
</tr>
<tr>
<td>collector depletion thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.4:1</td>
</tr>
<tr>
<td>emitter &amp; base contact resistivities</td>
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**nearly constant junction temperature → linewidths vary as (1 / bandwidth)²**

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<td>channel density of states</td>
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<tr>
<td>source &amp; drain contact resistivities</td>
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**fringing capacitance does not scale → linewidths scale as (1 / bandwidth)**
Electron Plasma Resonance: Not a Dominant Limit

\[
L_{\text{kinetic}} = \frac{T}{A q^2 nm^*} \\
R_{\text{bulk}} = \frac{T}{A q^2 nm^* \tau_m}
\]

\[
C_{\text{displacement}} = \frac{\varepsilon A}{T}
\]

dielectric relaxation frequency
\[
f_{\text{dielectric}} = \frac{1}{2\pi} \frac{1}{C_{\text{displacement}} R_{\text{bulk}}}
= \frac{1}{2\pi} \frac{\sigma}{\varepsilon}
\]

scattering frequency
\[
f_{\text{scattering}} = \frac{1}{2\pi} \frac{R_{\text{bulk}}}{L_{\text{kinetic}}}
= \frac{1}{2\pi \tau_m}
\]

plasma frequency
\[
f_{\text{plasma}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{kinetic}} C_{\text{displacement}}}}
\]

<table>
<thead>
<tr>
<th>Material</th>
<th>$f_{\text{plasma}}$ (THz)</th>
<th>$f_{\text{scattering}}$ (THz)</th>
<th>$f_{\text{dielectric}}$ (THz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-InGaAs</td>
<td>74</td>
<td>7</td>
<td>800</td>
</tr>
<tr>
<td>3.5 $\cdot 10^{19}$ / cm$^3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>p-InGaAs</td>
<td>31</td>
<td>12</td>
<td>80</td>
</tr>
<tr>
<td>7 $\cdot 10^{19}$ / cm$^3$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Thermal Resistance Scaling: Transistor, Substrate, Package**

\[ \Delta T_{\text{substrate}} \approx \frac{P}{\pi K_{\text{InP}} L_e} \ln \left( \frac{L_e}{W_e} \right) + \frac{P}{\pi K_{\text{InP}}} \left( \frac{1}{L_e} - \frac{1}{D} \right) + \frac{P}{K_{\text{InP}}} \cdot \left( \frac{T_{\text{sub}} - D/2}{D^2} \right) \]

- Cylindrical heat flow near junction increases logarithmically.
- Spherical flow for \( r > L_e \) is insignificant.
- Planar flow for \( r > D_{\text{HBT}}/2 \) increases quadratically if \( T_{\text{sub}} \) is constant.

\[ \Delta T_{\text{package}} \approx \left( \frac{1}{4} + \frac{1}{\pi} \right) \frac{P_{\text{chip}}}{K_{\text{Cu}} W_{\text{chip}}} \]

- Junction temperature rise, Kelvin
- Master-slave D-Flip-Flop clock frequency, GHz
- Substrate: cylindrical+spherical regions
- Substrate: planar region
- Package
- Total

**Wiring lengths** scale as \( 1/\text{bandwidth} \). Power density scales as \( \text{(bandwidth)}^2 \).
Thermal Resistance Scaling: Transistor, Substrate, Package

\[ \Delta T_{\text{sub}} \approx \frac{P}{\pi K_{\text{InP}} L_e} \ln \left( \frac{L_e}{W_e} \right) + \frac{P}{\pi K_{\text{InP}}} \left( \frac{1}{L_e} - \frac{1}{D} \right) + \frac{P}{K_{\text{InP}}} \cdot \left( \frac{T_{\text{sub}} - D / 2}{D^2} \right) \]

- cylindrical heat flow near junction for \( r > L_e \)
- spherical flow increase logarithmically
- planar flow for \( r > D_{HBT} / 2 \) increase quadratically if \( T_{\text{sub}} \) is constant

\[ \Delta T_{\text{package}} \approx \left( \frac{1}{4} + \frac{1}{\pi} \right) \frac{P_{\text{chip}}}{K_{\text{Cu}} W_{\text{chip}}} \]

Probable best solution:

**Thermal Vias ~500 nm below InP subcollector**

...over full active IC area.

\[ T_{\text{sub}} = 40 \mu m \cdot (150 \text{ GHz} / f_{\text{clock}}) \]
Bipolar Transistors
256 nm InP HBT

340 GHz dynamic frequency divider
M. Seo, UCSB/TSC

340 GHz VCO
M. Seo, UCSB/TSC
IMS 2010

324 GHz amplifier
J. Hacker, TSC
IMS 2010

204 GHz static frequency divider
Z. Griffith, TSC
CSIC 2010: to be presented

150 nm thick collector

10^9 10^10 10^11 10^12
f = 780 GHz
f_max = 424 GHz

70 nm thick collector

10^9 10^10 10^11 10^12
f = 560 GHz
f_max = 560 GHz

much better results in press ...
# InP Bipolar Transistor Scaling Roadmap

<table>
<thead>
<tr>
<th>Component</th>
<th>Width (nm)</th>
<th>Contact Width (nm)</th>
<th>Contact Resistance (Ω·μm²)</th>
<th>Current Density (mA/μm²)</th>
<th>Breakdown Voltage (V)</th>
<th>fₜ (GHz)</th>
<th>f_max (GHz)</th>
<th>Power Amplifiers (GHz)</th>
<th>Digital 2:1 Divider (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter</td>
<td>32</td>
<td>1</td>
<td>1 × 10⁻⁶</td>
<td>72</td>
<td>2</td>
<td>1400</td>
<td>2800</td>
<td>1400</td>
<td>660</td>
</tr>
<tr>
<td>Base</td>
<td>30</td>
<td>2.5</td>
<td>1.25 × 10⁻⁶</td>
<td>72</td>
<td>2.5</td>
<td>245</td>
<td>430</td>
<td>1000</td>
<td>240</td>
</tr>
<tr>
<td>Collector</td>
<td>37.5</td>
<td>36</td>
<td>72 × 10⁻⁶</td>
<td>72</td>
<td>2</td>
<td>150</td>
<td>240</td>
<td>1000</td>
<td>330</td>
</tr>
</tbody>
</table>

- **Emitter Contact Width**: 1 nm
- **Base Contact Resistance**: 1.25 Ω·μm²
- **Collector Thickness**: 37.5 nm
- **Current Density**: 72 mA/μm²
- **Breakdown Voltage**: 2-2.5 V
Fabrication Process for 128 nm & 64 nm InP HBTs

- dry-etched refractory emitter electrode
- in-situ refractory MO contact
- thin, wet-etched emitter
- upper low resistivity Au base contact
- lower refractory base contact

70 nm
**Initial Results: Refractory-Contact HBT Process**

### 110 nm emitter width

- **Gain (dB)**
- **Freq (Hz)**
- $f_t = 370 \text{ GHz}$
- $f_{max} = 700 \text{ GHz}$
- $A_{je} = 0.11 \mu m \times 3.5 \mu m$

### 270 nm emitter width

- **Gain (dB)**
- **Freq (Hz)**
- $f_t = 430 \text{ GHz}$
- $f_{max} = 800 \text{ GHz}$
- $A_{je} = 0.27 \mu m \times 3.5 \mu m$

**Need to add E-beam defined base, best base contact technology**
InP DHBTs: August 2010

\[ f_t \text{ or } f_{\text{max}} \text{ alone} \]
\[ \left( \frac{f_t + f_{\text{max}}}{2} \right)^{\frac{1}{2}} \]
\[ \left( \frac{1}{f_t} + \frac{1}{f_{\text{max}}} \right)^{-1} \]

**popular metrics:**
- PAE, associated gain, mW/\( \mu m \)
- Low noise amplifiers:
  - \( F_{\text{min}} \), associated gain,
- Digital:
  - \( f_{\text{clock}} \), hence
    - \( C_{cb} \Delta V / I_c \),
    - \( R_{ex} I_c / \Delta V \),
    - \( R_{bb} I_c / \Delta V \),
    - \( \tau_b + \tau_c \)

**much better metrics:**
- Teledyne DHBT
- UIUC DHBT
- NTT DBHT
- ETHZ DHBT
- UIUC SHBT
- UCSB DHBT
- NGST DHBT
- HRL DHBT
- IBM SiGe
- Vitesse DHBT

Updated Aug 2010
670 GHz Transceiver Simulations in 128 nm InP HBT

transmitter exciter

receiver

3-layer thin-film THz interconnects
thick-substrate --> high-Q TMIC
thin -> high-density digital

Simulations @ 670 GHz (128 nm HBT)

LNA: 9.5 dB Fmin at 670 GHz
PA: 9.1 dBm Pout at 670 GHz

VCO:
-50 dBc (1 Hz)
@ 100 Hz offset
at 620 GHz (phase 1)

Dynamic divider:
novel design,
simulates to 950 GHz

Mixer:
10.4 dB noise figure
11.9 dB gain
THz Field-Effect Transistors

(THz HEMTs)
**FET Scaling Laws**

Changes required to double device / circuit bandwidth.

*laws in constant-voltage limit:*

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<tr>
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<td>increase 2:1</td>
</tr>
<tr>
<td>electron mass in transport direction</td>
<td>constant</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
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HEMT/MOSFET Scaling: Four Major Challenges

- **gate dielectric:** need thinner barriers → tunneling leakage
- **contact regions:** need reduced access resistivity
- **channel:** need higher charge density yet keep high carrier velocity
- **channel:** need thinner layers
## THz FET Scaling Roadmap

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>35</th>
<th>25</th>
<th>18</th>
<th>13</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>nm</td>
<td>35</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>Gate barrier EOT</td>
<td>nm</td>
<td>0.83</td>
<td>0.58</td>
<td>0.41</td>
<td>0.29</td>
<td>0.21</td>
</tr>
<tr>
<td>Well thickness</td>
<td>nm</td>
<td>5.7</td>
<td>4.0</td>
<td>2.8</td>
<td>2.0</td>
<td>1.4</td>
</tr>
<tr>
<td>S/D resistance</td>
<td>Ω–μm</td>
<td>150</td>
<td>100</td>
<td>74</td>
<td>53</td>
<td>37</td>
</tr>
<tr>
<td>Effective mass</td>
<td>*m₀</td>
<td>0.05</td>
<td>0.05</td>
<td>0.08</td>
<td>0.08</td>
<td>0.08</td>
</tr>
<tr>
<td># band minima</td>
<td></td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>$f_τ$</td>
<td>GHz</td>
<td>700</td>
<td>770</td>
<td>1100</td>
<td>1600</td>
<td>2300</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>GHz</td>
<td>810</td>
<td>930</td>
<td>1400</td>
<td>2000</td>
<td>2900</td>
</tr>
<tr>
<td>$f_{divider}$</td>
<td>GHz</td>
<td>150</td>
<td>220</td>
<td>300</td>
<td>430</td>
<td>580</td>
</tr>
<tr>
<td>$I_d / W_g@ 200$ mV overdrive</td>
<td>mA/μm</td>
<td>0.54</td>
<td>0.69</td>
<td>0.95</td>
<td>1.4</td>
<td>1.8</td>
</tr>
</tbody>
</table>

- **high-K gate dielectrics**
- **source / drain regrowth**
- **Γ-L transport**
III-V MOSFETs with Source/Drain Regrowth

27 nm InGaAs MOSFET

N+ source regrowth
Mo contact
pulse doping
InGaAs well

100 nm
Regarding Mixed-Signal ICs & Waveform Generation
Clock Timing Jitter in ADCs and DACs

Timing jitter is quantitatively specified by the single-sideband phase noise spectral density $L(f)$.

IC oscillator phase noise varies as $\sim 1/f^2$ or $\sim 1/f^3$ near carrier

Impact on ADCs and DACs: imposition of $1/f^n$ sidebands on signal of relative amplitude $L(f)$ ...not creation of a broadband noise floor.

Dynamic range of electronic DACs & ADCs is limited by factors other than the phase noise of the sampling clock
Why ADC Resolution Decreases With Sample Rate

Dynamic Range Determined by Circuit Settling Time vs. Clock Period

1. IC time constants → Resolution decreases at high sample rates

- IC time constants
- Resolution decreases at high sample rates
Fast IC Waveform Generation: General Prospects

Waveform generator → fast digital memory & DAC

Parallel digital memory and 200 Gb/s MUX is feasible
cost limits: power & system complexity vs. # bits, GS/s

Performance limit: speed vs. resolution of DAC
faster technologies → increased sample rates

Feasible ADC resolution:
12 SNR bits @ 4 GS/s feasible using 500 nm (400GHz) InP HBT.
Feasible sample rate will scale with technology speed..
THz Transistors & Mixed-Signal ICs
Few-THz Transistors

**Few-THz InP Bipolar Transistors: can it be done?**

Scaling limits: contact resistivities, device and IC thermal resistances.

62 nm (1 THz $f_\tau$, 1.5 THz $f_{\text{max}}$) scaling generation is feasible.

- 700 GHz amplifiers, 450 GHz digital logic

*Is the 32 nm (1 THz amplifiers) generation feasible?*

**Few-THz InP Field-Effect Transistors: can it be done?**

Challenges are gate barrier, vertical scaling, source/drain access resistance, channel density of states.

- 2DEG carrier concentrations must increase.

S/D regrowth offers a path to lower access resistance.

Solutions needed for gate barrier: possibly high-$k$ (MOSFET)

**Implications:** 1 THz radio ICs, ~200-400 GHz digital ICs, 20 GHz ADCs/DACs