A Self-Aligned Epitaxial Regrowth Process for Sub-100-nm III-V FETs

Mark. Rodwell,
University of California, Santa Barbara

A. D. Carter, G. J. Burek, M. A. Wistey*, B. J. Thibeault, A. Baraskar, U. Singisetti,
J. Cagnon, S. Stemmer, A. C. Gossard, C. Palmstrøm
University of California, Santa Barbara
*Now at Notre Dame

B. Shin, E. Kim, P. C. McIntyre
Stanford University

Y.-J. Lee
Intel

B. Yue, L. Wang, P. Asbeck, Y. Taur
University of California, San Diego
III-V MOS: What is needed?

**True MOS device structures at ~10 nm gate lengths**

10nm gate length, < 10nm electrode spacings, < 10nm contact widths
< 3 nm channel, < 1 nm gate-channel separation, < 3nm deep junctions


**Drive currents >> 1 mA/micron @ 1/2-Volt V_{dd}**

Low access resistances.
Density-of-states limits.

**Dielectrics:** < 0.6 nm EOT, D_{it} < 10^{12}/cm^{2}-eV

impacts I_{on}, I_{off}, ...

Low dielectric D_{it} must survive FET process.

...and the channel must be grown on Silicon
FETs
FET Scaling Laws

Changes required to double device / circuit bandwidth.

*laws in constant-voltage limit:*

<table>
<thead>
<tr>
<th>FET parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/µm), $g_m$ (mS/µm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>channel 2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>electron mass in transport direction</td>
<td>constant</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel density of states</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>source &amp; drain contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

Current densities should double
Charge densities must double
Semiconductor Capacitances Must Also Scale

\[ (V_{gs} - V_{th}) \]

\[ c_{ox} \]

\[ c_{\text{depth}} = \varepsilon / T_{\text{inversion}} \]

\[ (E_f - E_{\text{well}}) / q \]

\[ c_{\text{dos}} = q^2 g_m^* / 2\pi\hbar^2 \]

\[ \text{channel charge} = qn_s = c_{\text{dos}} (V_f - V_{\text{well}}) = q(E_f - E_{\text{well}}) \cdot (g_m^* / 2\pi\hbar^2) \]

Inversion thickness & density of states must also both scale.
Calculating Current: Ballistic Limit

Channel Fermi voltage = voltage applied to $c_{dos}$
determines Fermi velocity $v_f$ through $E_f = qV_f = m \cdot v_f^2 / 2$

mean electron velocity $= \bar{v} = (4 / 3\pi)v_f$

Channel charge: $\rho_s = c_{dos}(V_f - V_c) = \frac{c_{dos}c_{equiv}}{c_{equiv} + c_{dos}}(V_{gs} - V_{th})$

c_{dos} = \frac{q^2 gm^*}{2\pi \hbar^2} = c_{dos,o} \cdot g \cdot (m^* / m_o)$, where $g$ is the # of band minima

$\Rightarrow J = \left(\frac{84 \ mA}{\mu m}\right) \cdot \frac{g \cdot (m^* / m_o)^{1/2}}{\left(1 + \left(c_{dos,o} / c_{ox}\right) \cdot g \cdot (m^* / m_o)\right)^{3/2}} \left(\frac{V_{gs} - V_{th}}{1 \ V}\right)^{3/2}$

Do we get highest current with high or low mass?
**Drive Current Versus Mass, # Valleys, and EOT**

\[
J = K \cdot \left( \frac{84 \text{ mA}}{\mu \text{m}} \right) \cdot \left( \frac{V_{gs} - V_{th}}{1 \text{ V}} \right)^{3/2}, \quad \text{where} \quad K = \frac{g \cdot \left( \frac{m^*/m_o}{g} \right)^{1/2}}{\left( 1 + (c_{dos,o} / c_{equiv}) \cdot g \cdot \left( \frac{m^*/m_o}{g} \right)^3 \right)}
\]

---

**Standard InGaAs MOSFETs** have superior \( I_d \) to Si at large EOT. Standard InGaAs MOSFETs have **inferior** \( I_d \) to Si at small EOT.
Transit Delay versus Effective Mass

\[ \tau_{ch} = K_2 \cdot \left( \frac{L_g}{2.52 \cdot 10^7 \text{ cm/s}} \right) \cdot \left( \frac{1 \text{ Volt}}{V_{gs} - V_{th}} \right)^{1/2} \]

where \( K_2 = \left( \frac{m^*}{m_0} \right)^{1/2} \cdot \left( 1 + \frac{c_{dos,o}}{c_{eq}} \cdot g \cdot \frac{m^*}{m_0} \right)^{1/2} \)

Low \( m^* \) gives lowest transit time, lowest \( C_{gs} \) at any \( EOT \).

Lower mass $\rightarrow$ Higher Carrier Velocity $\rightarrow$ lower input capacitance
improved gate delay in transistor-capacitance-limited gates
not relevant in wiring-capacitance-limited gates (i.e. most of VLSI)

More importantly: potential for higher drive current
improved gate delay in wiring-capacitance-limited gates (VLSI)

But this advantage is widely misunderstood in community
InGaAs channels $\rightarrow$ higher $I_d / W_g$ than Si only for thick dielectrics
....LOWER $I_d / W_g$ than Si for thin dielectrics
break-even point is at $\sim 0.5$ nm EOT

We will introduce (DRC2010) candidate III-V channel designs
providing higher $I_d / W_g$ than Si even for small EOT
Contacts: Low Resistivity, High Current Density

For <10% impact on drive current,

\[ I_D R_S / (V_{DD} - V_{th}) < 0.1 \]

Target \( I_D / W_g \sim 1.5 \text{ mA/\mu m} @ (V_{DD} - V_{th}) = 0.3 \text{ V} \)

\[ \rightarrow R_s W_g < 20 \Omega - \mu \text{m} \]

10 nm wide contact \( \rightarrow \rho_c < 0.2 \Omega - \mu \text{m}^2 (!) \)

current density in contact = 150 mA/\mu m^2 \( \rightarrow \) refractory contacts
FET: Key Regions, Key Challenges

For each 2:1 reduction in gate length:

**gate dielectric:**
2:1 reduction in thickness limit: tunneling → high-K limit (high-K): defects

**contacts:**
4:1 reduction in contact resistivity
2:1 shallower
4:1 higher J

**channel:**
2:1 increase in electron density @ same voltage
limit: # available electron states / area / energy "density of states bottleneck"; perceived to be fundamental
Highly Scaled FET Process Flows
Scalable nm III-V MOSFET: what is needed

True MOS device structures at ~10 nm gate lengths

10 nm gate length, < 10nm electrode spacings, < 10nm contact widths
< 3 nm channel, < 1 nm gate-channel separation, < w nm deep junctions

Self-aligned source/drain defined by MBE regrowth\(^2\)

Self-aligned in-situ Mo contacts\(^3\)

Process flow & dimensions selected for 10-30 nm L\(_g\) design;

\(^1\)Singisetti, ISCS 2008
\(^2\)Wistey, EMC 2008
\(^3\)Baraskar, EMC 2009
Regrown S/D process: key features

Self-aligned & low resistivity
...source / drain N+ regions
...source / drain metal contacts

Vertical S/D doping profile set by MBE
no n+ junction extension below channel
abrupt on few-nm scale

Gate-first

gate dielectric formed after MBE growth
uncontaminated / undamaged surface
Process flow*  

- cap metal
- InGaAs well barrier
- SI substrate
- MBE growth gate dielectric
dielectric cap
- blanket gate deposition
- etch gate, etch dielectric
to form sidewall
- MBE regrowth in-situ S/D metal
- planarize

- InGaAs well barrier
- SI substrate
- etch
- mesa isolate S/D
- Posts, planarization, pads

* Singisetti et al, 2008 ISCS, September, Freiburg
Key challenge in S/D process: gate stack etch

Requirement: avoid damaging semiconductor surface:

Approach: Gate stack with multiple selective etches*

FIB Cross-section
Damage free channel

Process scalable to ~10 nm gate lengths

Challenge in S/D process: dielectric sidewall

- $n_s$ under sidewall: electrostatic spillover from source, gate
- Sidewall must be kept thin: avoid carrier depletion, avoid source starvation
MBE Regrowth → Gap Near Gate → Source Resistance

- **Shadowing by gate: No regrowth next to gate**

- **Gap region is depleted of electrons**

  *High source resistance because of electron depletion in the gap*

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti
Migration Enhanced Epitaxial (MEE) S/D Regrowth*

*Wistey, EMC 2008
Wistey, ICMBE 2008

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti
Regrown S/D III-V MOSFET: Images

Cross-section after regrowth, but before Mo deposition

Top view of completed device
**Source Resistance: electron depletion near gate**

- **Electron depletion in regrowth shadow region** ($R_1$)

- **Electron depletion in the channel under $\text{SiN}_x$ sidewalls** ($R_2$)
Regrowth profile dependence on As flux*

multiple InGaAs regrowths with InAlAs marker layers

Uniform filling with lower As flux

* Wistey et al, EMC 2009
Wistey et al NAMBE 2009

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti
InAs source/drain regrowth

**Improved InAs regrowth with low As flux for uniform filling**\(^1\)

*InAs less susceptible to electron depletion: Fermi pinning above \(E_c\)*\(^2\)

\(^1\) Wistey *et al*, EMC 2009

Wistey *et al* NAMBE 2009.

\(^2\) Bhargava *et al*, APL 1997
In-Situ Refractory Ohmics on MBE Regrown N-InGaAs

**In-situ Mo on n-InAs**

- $\rho_c = 0.6 \pm 0.4 \, \Omega \cdot \mu m^2$
- $n = 1 \times 10^{20} \, cm^{-3}$

**In-situ Mo on n-InGaAs**

- $\rho_c = 1.0 \pm 0.6 \, \Omega \cdot \mu m^2$
- $n = 5 \times 10^{19} \, cm^{-3}$

- HAADF-STEM

TEM by Dr. J. Cagnon, Stemmer Group, UCSB

A. Baraskar
Benefits of refractory contacts

15 nm Pd/Ti diffusion

After 250°C anneal, Pd/Ti/Pd/Au diffuses 15nm into semiconductor
deposited Pd thickness: 2.5nm

Refractory Mo contacts do not diffuse measurably

Refractory, non-diffusive metal contacts for thin semiconductor layers
Resistivity of MEE Regrowth

15 µm TLM width

~50 nm InAs regrowth has ~22 Ω sheet resistivity
Contact resistivity is ~1.2 Ω-µm².
Self-Aligned Contacts: Height Selective Etching*

- Mo
- InGaAs
- InGaAs well
- barrier
- SI substrate

MBE regrowth
in-situ S/D metal

PR

InGaAs well
barrier
SI substrate

planarize

O₂ ash

InGaAs well
barrier
SI substrate

etch

strip PR

Fully Self-Aligned III-V MOSFET Process

50 nm N+ (4x10^{19}/cm^3) InGaAs regrowth
5 nm In_{0.53}Ga_{0.47}As channel
5 nm Al_{0.52}As barrier
P doped substrate

25 nm SiN sidewall
self-aligned in-situ Mo contacts

L_g = 200 nm W_g = 8 \mu m
V_{gs} : 0 to 4 V in 0.5 V steps

drain current I_D (mA/\mu m)
V_{DS} (V)

Gate InAs regrowth
top of gate	side of gate
Mo S/D metal with N+ InAs underneath

Acc.V Spot Magn Det WD 100 nm
10.0 kV 3.0 20000x TLD 5.0 090310C_InAs_MEE_500C_D2

10.0 kV 3.0 35000x TLD 5.3 090326C_regrowth_Mo_edge
Subthreshold characteristics

$L_g = 1.0 \, \mu m$

$I_d (A)$ vs. $V_{gs} (V)$ for $V_{ds} = 0.1 V$ and $V_{ds} = 1.0 V$

$L_g = 0.35 \, \mu m$

$I_d (A)$ vs. $V_{gs} (V)$ for $V_{ds} = 0.1 V$ and $V_{ds} = 1.0 V$

290 mV/decade

325 mV/decade
10-30 nm Process Development

Excellent structural yield in sub-100nm process flow
27 nm Self-Aligned InGaAs MOSFET

Self-aligned N+ S/D regrowth
shallow, high doping, low sheet $\rho$

Self-aligned Mo in-situ S/D contacts:
low $\rho$, refractory $\rightarrow$ shallow
HAADF TEM
STEM is chemical contrast imaging -> Is the regrowth sinking?
Conclusion
**III-V MOS**

With appropriate design, III-V channels can provide > current than Si ...even for highly scaled devices

But present III-V device structures are also unsuitable for 10 nm MOS
large access regions, low current densities, deep junctions

Raised S/D regrowth process is a path towards a nm VLSI III-V device