100-1000 GHz Bipolar ICs: Device and Circuit Design Principles

Part II: Design / Testing of 300 GHz ICs in InP HBT Technology

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  — Cleanroom Staff
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  — Professor Mark Rodwell and his Device Team.

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  — Dr. Anders Skalare, Alejandro Peralta, Robert Lin

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Outline

- Overview / General Considerations in > 300 GHz IC Design
- Transceiver Building Blocks
  - 350 GHz Differential LNA
  - 300 GHz Differential Oscillator
  - 300 GHz Dynamic Frequency Divider
- 350 GHz Single-Chip Receiver IC
- 300 GHz Single-Chip PLL IC
- Conclusion
Challenges in > 300 GHz IC Design & Characterization

- **Low transistor gain / high passive loss**
  - Diff. topology removes AC-ground loss

- **Modeling (Device / EM) uncertainties**
  - Diff. topology removes AC-ground impedance
  - Inverted Microstrip → Guaranteed *solid* ground plane
    * Normal microstrip → Many holes due to HBT conn.
    * CPW → Not suitable for complex / feedback c Ikts

- **Many CKT-EM cycles**

- **Testing**
  - Everything is $$$ (money / delivery time) : VNA / mixer / source / probe…
  - Exploit on-chip self-testing:
    - Integrated OSC+Mixer / OSC+Divider / LNA+Mixer
Differential Topology for mm-wave ICs

- **Differential topology eliminates**
  - (1) Gain reduction due to $R_{AC-GND}$
  - (2) BW reduction due to $L_{AC-GND}$
  - (3) Detuning due to MIM cap model errors → Robust design
  - (4) Detuning due to bias ckt & via (→ 3D) model errors → Robust design
- **Differential topology decouples RF from DC BIAS** → Flexible design
  ...at the cost of $P_{DC}$↑, Area↑, # device↑
- **Caution: Common-mode Stability**

\[
\begin{bmatrix}
S_{11} & S_{12} & S_{13} & S_{14} \\
S_{21} & S_{22} & S_{23} & S_{24} \\
S_{31} & S_{32} & S_{33} & S_{34} \\
S_{41} & S_{42} & S_{43} & S_{44}
\end{bmatrix} \rightarrow \begin{bmatrix}
S_{DM} & S_{DM} & 0 & 0 \\
S_{DM} & S_{DM} & 0 & 0 \\
0 & 0 & S_{CM} & S_{CM} \\
0 & 0 & S_{CM} & S_{CM}
\end{bmatrix}
\]

- AC ground
  - (MIM cap, $\frac{1}{2}\lambda$ line, radial stub)
  - Lossy, finite BW

- Virtual ground
  - Lossless, $\infty$ BW

- Gain drop per stage
  \[
  \frac{Q_{L1,\text{eff}}}{Q_{L1,\text{eff}} + Q_{11}} \cdot \frac{Q_{L2,\text{eff}}}{Q_{L2,\text{eff}} + Q_{22}}
  \]
  
- BW reduction per stage
  \[
  \frac{L_1}{L_1 + L_{AC-GND}} \cdot \frac{L_2}{L_2 + L_{AC-GND}}
  \]

$L_1, L_2$ input/output matching inductance

$R_{AC-GND}$ ac-ground resistance at resonance

$L_{AC-GND}$ ac-ground series inductance

$Q_{L1,\text{eff}} = \omega L_1 / (R_{L1} + R_{AC-GND})$

$Q_{11} = \text{Im}(y_{11}) / \text{Re}(y_{11})$

$[y_{ij}]$ Transistor $y$ parameter

$Q_{L2,\text{eff}}$, $Q_{22}$ similarly defined.
Teledyne 0.25µm InP HBT Process: Overview

- Two process generations: THzIC1 \( (f_{\text{max}} \sim 600\text{GHz}) \), THzIC2 \( (f_{\text{max}} \sim 800\text{GHz}) \)
- 3-Metal (Au) back-end: M1, M2, M3 (all 1µm thick)
- Thin-film resistor (50Ω/sq), MIM cap (0.3fF/µm²), B-C junction varactor
- Optional wafer thinning & Thru-wafer vias
- Packaging in a silicon micromachined waveguide block.
0.25μm InP HBT RF Performance

At 300 GHz, MAG\textsubscript{CE} = 5 dB, MSG\textsubscript{CB} = 10.8 dB, MSG\textsubscript{cascode} = 20 dB

In actual circuits, operating gain will be further limited by: (1) stabilization (if unstable), (2) matching network losses, and (3) large-signal operation (e.g. oscillators or power amplifiers)
Passive Device Modeling

Thin-Film Resistors (TFR)

- 10μ × 20μ (100Ω @dc)
- 10μ × 50μ (250Ω @dc)

MIM Capacitors

- 10μ × 10μ
- 10μ × 13μ
- 13μ × 13μ

Inverted Microstrip Line

Loss of 50Ω line (W=10μ): 3-4 dB/mm @300-500 GHz

B-C junction varactor

- Aspect ratio optimized for high-Q
- Capacitance ratio = 1.6 @V_{CB} = 0-1V
Design Flow

(1) Build passive device library
   Transmission lines: \((Z_0, \beta)\) – compact model from EM sim
   MIM caps, Thin-film resistors: 2-port S-param from EM sim

(2) Initial schematic design using the library

(3) Core circuit layout (i.e. w/o common-mode bias)

(4) EM-sim. \(\rightarrow\) Multi-port S-param

(5) Re-simulation w/ S-param blocks (core + bias)

(6) Complete top-level layout w/ bias, interconnects, RF / DC pads, etc.

(7) Final Design Verification
   DRC (Design-Rule Check)
   LVS (Layout-versus-Schematic)

CKT-EM cycle
- \(\sim 300 \text{ GHz}: 1\sim 2\) cycles
- \(> 500 \text{ GHz}: > 5\) cycles
Waveguide Packaging of InP Chips

- InP chips after backside singulation
- Amplifier ICs after backside release
- Silicon micromachined waveguide

THRU-line test chip in a silicon WG block

- Through-wafer vias, wafer thinning → backside metallization → dry etch chip singulation → mount in silicon micromachined waveguide block
- WR3 THRU test chip: < 4 dB measured insertion loss @300 GHz, < 1 dB per transition
Design of 300 GHz Building Blocks

- 350 GHz Differential LNA
- 300 GHz Differential Oscillator
- 300 GHz Dynamic Frequency Divider
350 GHz Differential Cascode Amplifier

- Topology: Differential Cascode
- RF operation in diff. mode (blue line), DC biasing in common mode (black line)
- Make sure no common-mode oscillation (dc-$f_{max}$)

**Layout / EM model**
- Inverted-Microstrip (Continuous M3 ground plane)
- Total 21 ports (16 device, 4 RF, 1 bias) → 21-port S-parameter

Size: $60 \times 180 \, \mu m^2$

- Output matching
- Stability control

1. Suppress common-mode gain
2. Bypass thermal noise from $R_E$
### 350 GHz Differential Cascode Amplifier

#### Three modes of operation of interest: \textit{DIFF}, \textit{COMM}, \textit{SE} modes

- If \textit{DIFF} gain is sufficiently higher than \textit{COMM}-mode gain, \textit{SE}-mode performance approaches \textit{DIFF}-mode
  - i.e. input common-mode will diminish, yielding $|S_{21,\text{SE}}| \approx |S_{31,\text{SE}}| \approx |S_{21,\text{DIFF}}| - 3\text{dB}$, $\text{NF}_{\text{SE}} \approx \text{NF}_{\text{DIFF}}$.
  - \textit{SE} mode operation (1) facilitates testing, and (2) obviates lossy input balun, thus most useful in the receiver front-end.

- $S_{21,\text{diff}} = 10 \text{ dB/stage}$, noise figure = 13.8 dB @ $P_{\text{DC}} = 50 \text{ mW/stage}$

- Amplifier must be stable in all three modes.
SE Mode Operation: What About Output Balance?

‘Single-Ended’ (SE) Mode

P1 P2 P3

Question: In SE mode, are the amplifier outputs (P2, P3) well balanced?

Average Gain = dB((S_{21} + S_{31})/2)

Magnitude Error = dB(S_{21} / S_{31})

Phase Error = phase(S_{21} / S_{31}) \cdot 180

- For a 3-stage differential configuration, amplitude and phase imbalances are less than 0.1 dB and 0.5 deg, respectively.
Effects of AC-ground Impedance: Single-Ended Amplifier Example

- Amplifier in a single-ended topology, but otherwise, equivalent to the previous 3-stage differential 350 GHz design (e.g. same matching network, same bias)
- Effects of AC-ground resistance / inductance are clearly seen: Even $R_{AC-GND} = 1 \, \Omega$ degrades circuit gain by 4-5 dB (= 1.5 dB reduction per stage).
- $L_{AC-GND} = 10 \, \text{pH}$ reduces amplifier 3-dB bandwidth by half !!
350 GHz Differential Cascode Amplifier: Layout & Hierarchy

Single-stage cell

Core circuit block
(mostly diff.)
→ Full EM model
(multi-port S-param)

Bias circuitry (SE)
→ EM or compact model

Multi-Stage Cell

Final on-wafer testing structure

- General layout hierarchy: core_half → core → single_stage → multi_stage → top_cell
- Note M3 top ground plane covers entire circuit.
3-D Top View

Top M3 ground plane set to partially transparent
M1 / M2 Signal, M3 GND (inverted microstrip)
Inverted MSL-to-Pad Transition

- On-wafer testing of inverted-MSL-based circuits requires a transition to a co-planar GSG pad.
- Distance from M3 GND plane to signal pad ($L_1, L_2$) was adjusted for broadband low-loss transition.
- Simulated $S_{21} = -0.5$dB @300 GHz, -1.4dB @550 GHz ($S_{11} < -12$ dB)
2-port Vector Network Analyzer (VNA) Setup

- 220-325 GHz (WR3) OML VNA Extenders
  - Interfaced with HP8510C
- 500-750 GHz (WR1.5) VDI VNA Extenders
  - Interfaced with Agilent PNA-X

- mm-wave extenders interface with main VNA module via IF / LO
- VNA setup for 325-500 GHz (WR2.2) band available at JPL
- A VNA extender can also be used as a Up/Down conversion harmonic mixer
  —e.g. oscillator frequency measurement (Watch out for image responses!!)
350 GHz 3-Stage Differential Cascode Amplifier: Measurement Results

- Peak $S_{21,SE} = 27$ dB @350 GHz, @ $P_{DC}=150$ mW
- Testing in 2-port SE mode, with unused output port (P3) terminated on-chip.
- Noise figure of receiver chain (3-stage LNA + down-mixer) was measured to be 13 dB (will be shown later)
450 GHz 3-Stage Differential Cascode Amplifier: Measurement Results

- Peak $S_{21,SE} = 9 \text{ dB} \ @ 440 \text{ GHz, } @ P_{DC} = 150 \text{ mW}$
- Testing in 2-port SE mode, with unused output port (P3) terminated on-chip.
300 GHz Oscillator: Schematic

- **Topology:** Differential series-tuned oscillator w/ stacked common-base buffer
  - Fixed-frequency designs (FFO) and voltage-controlled designs (VCO)
- RF operation in diff. mode (blue line), DC biasing in common mode (black line)
- Make sure no common-mode oscillation \( (\text{dc-f}_{\text{max}}) \)

“π” feedback

“T” feedback

Less discontinuities
More predictable
More scalable

Output matching

Common-base buffer (gain, isolation)

Load coupling

OSC core

Tuning range control

Improves Common-mode stability

Defines \( V_{CB} \) of \( Q_1-Q_4 \)

Provides \( V_{BE} \) of \( Q_1-Q_4 \)

\( V_{EE} \) can be tuned for an optimum \( J_E \)

\( V_{BB} \) can be tuned for an optimum \( V_{CB} \)
300 GHz VCO: Core Layout / EM Model

Inverted-Microstrip: M1/M2 Signal, M3 GND
Line width = 5 μm (except for 50Ω output line)
Layout: 300 GHz versus 570 GHz

(1) Stronger line coupling
(2) Mostly “discontinuous”
→ More CKT-EM cycles
Freq. Testing with an External Mixer

OSC under test → WR3 probe (GGB) → WR-3 VNA Extender → Down-converter → IF < 100 MHz → HP8565 Spectrum Analyzer

3-4dB loss

Test chip size: 740×550 μm²

VCO Cell (Core+Bias)
Size: 400×200 μm²

RF OUT
V

V TUNE

V BB

VEE

HBT $J_E = 7-10 \text{ mA/μm}^2$

$P_{DC} = 70-110 \text{ mW}$

Fixed-frequency & voltage-controlled designs from 250 to > 600 GHz

300 GHz VCO in waveguide package

Typical IF Spectrum

Typical VCO tuning curve

Oscillation frequency (GHz)

Vtune [V]
OSC Freq. Testing: Integrated OSC+MIX

- Integrated mixer facilitates spectrum measurement.
  - No > 300 GHz mm-wave interface
- Sub-harmonic operation
  - \( f_{LO} \approx 20 \text{ GHz} \) (\( BW_{IF} > 25 \text{ GHz} \))
  - \( N=21-31 \) for 400-600 GHz RF input
  - Conv. Loss = 30-40 dB
- Mixer consumes 60 mW.
**OSC Freq. Testing: Integrated OSC+MIX**

**Signal Generator**
- **HP8341B**
- Output: $f_{LO} \sim 20\, \text{GHz}$
- **30~40dB loss**
- Output: $f_{IF} < 20\, \text{GHz}$

**OSC+Mixer under test**

**Spectrum Analyzer**
- **HP8565**

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**Power (dBm)**

**$f_{LO} = 19.8\, \text{GHz}$**
- **Power ($-40$ dBm)**
- **Center:** 2.897 GHz
- **Span:** 2 GHz
- **$\Delta f_{LO} = 0.2\, \text{GHz}$**

**$f_{IF} = 2.893\, \text{GHz}$**
- **Power ($-40$ dBm)**
- **Center:** 2.893 GHz
- **Span:** 2 GHz

**Power (dBm)**

**$f_{LO} = 20.0\, \text{GHz}$**
- **Power ($-40$ dBm)**
- **Center:** 7.100 GHz
- **Span:** 2 GHz

**$f_{IF} = 7.100\, \text{GHz}$**
- **Power ($-40$ dBm)**
- **Center:** 7.100 GHz
- **Span:** 2 GHz

---

**$f_{IF}$**

\[ f_{IF} = \left| Nf_{LO} - f_{OSC} \right| \]

\[ \frac{\Delta f_{IF}}{\Delta f_{LO}} > 0 \quad \Rightarrow \quad f_{IF} = Nf_{LO} - f_{OSC} \]

\[ N = \text{Round} \left( \frac{\Delta f_{IF}}{\Delta f_{LO}} \right) = \text{Round} \left( \frac{7.1 - 2.893}{0.2} \right) = \text{Round}[21.035] = 21 \]

**Small**
300 GHz VCO Tuning Bandwidth

- Theoretical max. tuning range = $\sqrt{C_{RATIO}} = \sqrt{1.4} \approx 1.2$ (20%)
- Varactors lightly coupled ($Q_{VAR} \sim 8$, $Q_{TL} \sim 25$)
Measured Phase Noise

- **Approximately follow -20 dB/dec curve**
  - 1/f noise corner < 1 MHz
- **IF noise floor limits measurement for offsets > 20 MHz**
- **Drifts in oscillation frequency must be minimized for accurate phase noise testing**
  - Stable, low-noise power supplies

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**Oscillation frequency (GHz)**

- Voltage-controlled designs (VCO)
- Fixed-frequency designs (FFO)

**Initial spectrum**

**After 10-min**

\[ \Delta \text{freq} \approx 7 \text{MHz} \]
Oscillator Power Testing

WR3 (220-330G)
WR2.2 (330-500G)

WR3 probe (3-4dB loss)
WR2.2 probe (5-8dB loss)

OSC under test → Waveguide taper → WR-10 → Erikson Inst. Power meter

WR1.5 (500-750G)

DC supply → OSC → Waveguide transition → Waveguide taper → WR-10 → Erikson Inst. Power meter → software

Problem: Tiny raw power → Lowest full-scale → Long settling time → Subject to drift
Solution: Modulated sensing

dc supply
Modulation
(3 s ON, 3 s OFF)
digitized readout
de-modulation
WR-1.5 Power Testing Setup (JPL)

# Oscillator Measurement Summary / Performance Comparison

<table>
<thead>
<tr>
<th>Process Technology</th>
<th>Oscillation Frequency</th>
<th>Single-ended output power(^1) (dBm)</th>
<th>Phase noise @ 10 MHz offset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Design</td>
<td>Measured</td>
<td>Simulation w/ revised HBT model</td>
</tr>
<tr>
<td>THzIC1</td>
<td>292.4 GHz</td>
<td>267.4 GHz</td>
<td>261.5 GHz</td>
</tr>
<tr>
<td>THzIC1</td>
<td>315.4 GHz</td>
<td>286.8 GHz</td>
<td>280.6 GHz</td>
</tr>
<tr>
<td>THzIC1</td>
<td>336.5 GHz</td>
<td>310.2 GHz</td>
<td>303.7 GHz</td>
</tr>
<tr>
<td>THzIC1</td>
<td>387.8 GHz</td>
<td>346.2 GHz</td>
<td>346.0 GHz</td>
</tr>
<tr>
<td>THzIC2</td>
<td>397.0 GHz</td>
<td>412.9 GHz</td>
<td>394.5 GHz</td>
</tr>
<tr>
<td>THzIC2</td>
<td>508.0 GHz</td>
<td>487.7 GHz</td>
<td>505.9 GHz</td>
</tr>
<tr>
<td>THzIC2</td>
<td>587.9 GHz</td>
<td>573.1 GHz</td>
<td>586.3 GHz</td>
</tr>
</tbody>
</table>

1. Inverted-microstrip-to-GSG-pad transition loss included.
2. Probe and/or waveguide transition loss is deembedded.

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**Oscillation frequency (GHz)**

**Output power (dBm)**
mm-wave OSC beyond 250 GHz: References


300 GHz Dynamic Frequency Divider: Schematic

“Regenerative” frequency divider

Many implementations possible

- Single-TR circuit
  w/ implicit feedback

- Multi-TR circuit
  w/ explicit feedback

Topologies:
- Double-balanced mixer with emitter follower (EF) feedback and inductive loading (Adapted from H. M. Rein’s original design)
- Compared to a traditional resistive / trans-impedance loading, inductive loading significantly extends divider bandwidth.
- Beyond ~400 GHz, divider operation is ultimately limited by the EF stage.

Traditional R-loading: < 220 GHz
Inductive loading: < 360 GHz

Emitter-follow feedback

Improves sensitivity by ~3dB
Divider Layout / EM Model

Divider Core (also EM Model)

Size: 140×90 μm²

Upper
diff. pairs

M1

M2

M3

DIVOUT(+)

DIVOUT(-)

Bias

Lower
diff. pair

RFIN+

RFIN-

Total 29 ports (24 device, 4 RF, 1 bias) → 29-port S-parameter

Test Chip (880×470 μm²)
Divider Simulation Results

Typical output waveform

Voltage (V)

Power (dBm)

Divider Input Freq. (GHz)

Input Sensitivity (dBm)

Divider Output Power (dBm)

VCO output

Minimum input power (S.E)

Input Sensitivity (dBm)

BW margin

P\textsubscript{DC} = 90 mW

P\textsubscript{IN,SE} = -3 dBm

Typical output power

Typical output spectrum
Divider Testing using External 300 GHz Source (UCSB)

- Divider operating bandwidth: 305-330 GHz ($P_{DC} = 100$ mW)
- Testing @ < 300 GHz limited by insufficient source power
- Sub-harm. mixer produces multiple image responses → Use “Signal Identification” (spectrum analyzer built-in function) for correct output tone identification.

**Graphical Elements**
- Signal Source: Virginia Diodes
- X24 Freq. Mult.: WR3 probe (3dB loss) 300 GHz
- Divider: WR5 probe (2.1dB loss) 150 GHz
- Harmonic Mixer: OML Inc.
- Spectrum Analyzer: HP-70000

**Graphical Data**
- $P_{IN}$ (meas): 300 GHz VDI Source
- $P_{OUT}$ (meas)
- $P_{OUT}$ (sim)
- Insufficient $P_{IN}$

**Image Descriptions**
- WR3 mixer
- 320GHz VDI multiplier
- Input = 314.24 GHz
- Output = 157.12 GHz

**Graph Details**
- Power (dBm) vs. Divider Input Frequency (GHz)
- Range: 300 to 340 GHz
- Y-axis: -35 to 15 dBm
Divider Testing: Integrated VCO+DIV

- Each divider design is integrated w/ VCO for on-chip self-testing
  — 4 VCO designs centered at 275 GHz, 300 GHz, 325 GHz, and 350 GHz, w/ 5-10 GHz tuning bandwidth.

- Confirms divider operation from 278 GHz to 350 GHz.

Chip Size: 1,100×600 μm²
# Divider: Performance Comparison

<table>
<thead>
<tr>
<th>Ref. (year)</th>
<th>Type</th>
<th>Technology</th>
<th>Div. Ratio</th>
<th>Max. operating freq. [GHz]</th>
<th>Min. operating freq. [GHz]</th>
<th>Power Supply [V]</th>
<th>DC power [mW]</th>
<th>Die area [mm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] (2003)</td>
<td>Regenerative</td>
<td>SiGe ($f_t = 207\text{GHz}$)</td>
<td>2</td>
<td>100</td>
<td>14</td>
<td>-3.8</td>
<td>285</td>
<td>-</td>
</tr>
<tr>
<td>[2] (2006)</td>
<td>Regenerative</td>
<td>SiGe:C ($f_t = 200\text{GHz}$)</td>
<td>2</td>
<td>103</td>
<td>24</td>
<td>+5.2</td>
<td>195</td>
<td>1×0.5</td>
</tr>
<tr>
<td>[3] (2003)</td>
<td>Regenerative</td>
<td>mHEMT ($f_t = 220\text{GHz}$)</td>
<td>2</td>
<td>108</td>
<td>86</td>
<td>-</td>
<td>360</td>
<td>1×0.75</td>
</tr>
<tr>
<td>[4] (2003)</td>
<td>Regenerative</td>
<td>SiGe ($f_t = 200\text{GHz}$)</td>
<td>2</td>
<td>110*</td>
<td>35</td>
<td>-5</td>
<td>310</td>
<td>0.55×0.45</td>
</tr>
<tr>
<td>[5] (2009)</td>
<td>Regenerative</td>
<td>SiGe ($f_t = 210\text{GHz}$)</td>
<td>2</td>
<td>136*</td>
<td>74</td>
<td>-3.3</td>
<td>118.8</td>
<td>1.78×0.63</td>
</tr>
<tr>
<td>[6] (2009)</td>
<td>Injection locking</td>
<td>65 nm CMOS</td>
<td>2</td>
<td>137</td>
<td>128.24</td>
<td>+1.1</td>
<td>5.5¹</td>
<td>0.6×0.5</td>
</tr>
<tr>
<td>[7] (2003)</td>
<td>Clocked inverter</td>
<td>InP HBT ($f_t = 245\text{GHz}$)</td>
<td>2</td>
<td>150*</td>
<td>120</td>
<td>-5.5</td>
<td>357</td>
<td>1.5×1.5</td>
</tr>
<tr>
<td>[8] (2006)</td>
<td>Regenerative</td>
<td>SiGe ($f_t = 225\text{GHz}$)</td>
<td>4</td>
<td>160</td>
<td>80</td>
<td>-5.5</td>
<td>650</td>
<td>0.55×0.45</td>
</tr>
<tr>
<td>[9] (2009)</td>
<td>Regenerative</td>
<td>SiGe:C ($f_t = 215\text{GHz}$)</td>
<td>2</td>
<td>168</td>
<td>51</td>
<td>+4</td>
<td>105²</td>
<td>0.58×0.48</td>
</tr>
<tr>
<td>[10] (2010)</td>
<td>Regenerative</td>
<td>InP HBT ($f_t = 375\text{GHz}$)</td>
<td>2</td>
<td>331.2</td>
<td>304.8¹</td>
<td>-4.1 / -3.3</td>
<td>85.5</td>
<td>0.64×0.62</td>
</tr>
</tbody>
</table>

¹ Including power consumption of the output buffer.  
² Including pads.  
³ Measurement limited by available test setup

**References**


350 GHz Single-Chip Receiver

300 GHz Single-Chip PLL
300 GHz / 350 GHz Integrated Differential Receiver

**Receiver Layout**

- Includes LNA, double-balanced mixer, and VCO
- Receiver designs at 300 GHz and 350 GHz
- RF input is single-ended, IF output is differential
- On-wafer noise figure (NF) testing performed at JPL
  - Hot/Cold noise source coupled to receiver w/ horn-antenna
  - NF derived using Y-factor method
  - IF frequency: 2.18 GHz, 320 MHz bandwidth

**Measured Receiver Gain and Noise Figure**

<table>
<thead>
<tr>
<th>VCO Freq.</th>
<th>DC Power</th>
<th>Input Probe Loss</th>
<th>Receiver Gain</th>
<th>Receiver NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>305 GHz</td>
<td>222 mW</td>
<td>3 dB</td>
<td>32 dB</td>
<td>10 dB</td>
</tr>
<tr>
<td>345 GHz</td>
<td>303 mW</td>
<td>5.5 dB</td>
<td>27 dB</td>
<td>13 dB</td>
</tr>
</tbody>
</table>

**Chip photograph** (1,300×570 μm²)

- 2-stage LNA
- Mixer
- 300 / 350 GHz VCO

**On-wafer NF testing setup at JPL**

- Horn antenna
Phase-Locked Source @ 300 GHz

→ Critical, power hungry, building block for THz imager / instrumentation

Commercially available source

Product: 330 GHz FEM

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<table>
<thead>
<tr>
<th>Technology</th>
<th>GaAs Shottky diodes (modules)</th>
<th>0.25μ InP HBT (one-chip)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>~1000 cm³</td>
<td>~1 mm² (unpackaged)</td>
</tr>
<tr>
<td>Weight</td>
<td>~1 kg</td>
<td>~1 g (unpackaged)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>~ 10 W</td>
<td>0.3 W</td>
</tr>
<tr>
<td>Output power</td>
<td>0 ~ 13 dBm</td>
<td>-23 dBm</td>
</tr>
<tr>
<td>Tunable range</td>
<td>20 GHz (320-340 GHz)</td>
<td>0.36 GHz (300.76-301.12 GHz)</td>
</tr>
</tbody>
</table>

Low-power / Portable / Handheld
300 GHz InP PLL: Overview

Phase detector ($\times 5$ sub-harmonic)

Active loop filter

300 GHz VCO

Critical path

REF CLK (30 GHz)

2:1 Dynamic Frequency Divider

300 GHz PLL OUT

150 GHz

300 GHz VCO

Static 2:1 DIV

Static 2:1 DIV

Static 2:1 DIV

37.5 GHz

PD

Static Div NOT fast enough

>100 HBTs, 2W $P_{DC}$

300 GHz VCO

Dynamic 2:1 DIV

Static 2:1 DIV

Static 2:1 DIV

37.5 GHz

PD

50 HBTs, 0.3 W $P_{DC}$

300 GHz VCO

Dynamic 2:1 DIV

150 GHz

Sub-harmonic PD

REF (30 GHz)
Phase Detector: 5\textsuperscript{th}-order Sub-harmonic

**Gilbert Cell as a Odd-sub-harmonic PD**

- Gilbert Cell can operate as a phase detector in odd-order sub-harm. mode
- Useful detection gain up to 5\textsuperscript{th}-order (N=5) sub-harmonic operation
- Operation at N > 5 may suffer from increased sensitivity of active loop filter offset voltages (phase noise may also degrade).
300 GHz PLL: Layout

- Total 51 HBTs
- $P_{DC} = 302 \, mW$
  - VCO: 96 mW,
  - DIV: 90 mW,
  - PD: 26 mW,
  - LF: 90 mW.

Size: 1,380 $\times$ 610 $\mu m^2$
PLL: Measured Spectrum

Measurement Setup

15 GHz
Signal generator
HP83752B

x2 Freq. Multiplier
HP83554A
HP8349B

REF clock (30 GHz)
300 GHz PLL IC

PLL output (WR3)
WR-3 VNA extender
OML Inc.

Spectrum analyzer
HP-8565E

PLL Output (dBm) Readout
m1
freq=
PLL_output_dBm=-52.667 260.02MHz

Narrowband Spectrum
Center: 260MHz
Span: 500 KHz
RBW 3KHz
VBW 100Hz

Wideband Spectrum
Center: 260MHz
Span: 500 MHz
RBW 100KHz
VBW 3KHz

- PLL output power = -23 dBm @ P_Dc = 302 mW
  - Most of VCO output power goes to the dynamic frequency divider
PLL: Measured Phase Noise

Measurement by HP8565E Built-in Phase-Noise Meas. Utility

Freq. mult. factor = \(20 \log_{10} \left( \frac{300}{30} \right) = 20 \, \text{dB}\)

-78 dBc/Hz @100 KHz

PLL OUT (300.96 GHz)

REF CLK (30.096 GHz)
PLL: Measured Tuning Bandwidth

m2
freq=101.61MHz
PLL_output_dBm=-49.667

m3
ind Delta=3.588E8
dep Delta=-4.167
Delta Mode ON

360 MHz
f_{ref} = 15.038 \sim 15.056 \text{ GHz (1 MHz step)}
f_{vco} = 300.76 \sim 301.12 \text{ GHz}
220 GHz PLL (CSICS-2011)

- Improved locking range (increased loop filter gain) and output power (2-stage cascode output amplifier) compared to the previous 300 GHz PLL.
- Measured locking range: 220-225.9 GHz (BW = 5.9 GHz)
- PLL output power = -1 dBm (estimated) @ P_{DC} = 465 mW
- Phase noise: -83 dB/Hz @100 KHz
## PLL: Performance Comparison

<table>
<thead>
<tr>
<th>Published mm-Wave PLLs beyond 70 GHz</th>
</tr>
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<tbody>
<tr>
<td></td>
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<tr>
<td><strong>Frequency [GHz]</strong></td>
</tr>
<tr>
<td>InP 300 GHz (IMS-2011)</td>
</tr>
<tr>
<td>InP 220 GHz (CSICS-2011)</td>
</tr>
<tr>
<td>RFIC-2010</td>
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<tr>
<td>JSSC-2007</td>
</tr>
<tr>
<td>ISSCC-2009</td>
</tr>
<tr>
<td>MTT-2006</td>
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<tr>
<td>JSSC-2008</td>
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<tr>
<td>300.76–301.12</td>
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<tr>
<td>220–225.9</td>
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<tr>
<td>162–164*</td>
</tr>
<tr>
<td>86–92</td>
</tr>
<tr>
<td>81–82</td>
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<tr>
<td>91.8–101*</td>
</tr>
<tr>
<td>45.9–50.5</td>
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<tr>
<td>95.1–96.5</td>
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<tr>
<td>79.4</td>
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<tr>
<td>73.4–73.72</td>
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</tr>
<tr>
<td><strong>Technology</strong></td>
</tr>
<tr>
<td>InP HBT</td>
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<tr>
<td>InP HBT</td>
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<tr>
<td>0.13µm BiCMOS</td>
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<tr>
<td>0.13µm CMOS</td>
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<tr>
<td>65nm CMOS</td>
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<tr>
<td>SiGe</td>
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<tr>
<td>90nm CMOS</td>
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<tr>
<td></td>
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<tr>
<td><strong>Divide ratio [f_vco/f_ref]</strong></td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>16,32, 64, 128</td>
</tr>
<tr>
<td>512</td>
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<tr>
<td>256</td>
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<tr>
<td>64</td>
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<tr>
<td>32</td>
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<tr>
<td><strong>Phase noise @100KHz [dBC/Hz]</strong></td>
</tr>
<tr>
<td>-78</td>
</tr>
<tr>
<td>-83</td>
</tr>
<tr>
<td>-78.9 @163GHz</td>
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<tr>
<td>-93.8 @90GHz</td>
</tr>
<tr>
<td>-63.5</td>
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<tr>
<td>(50KHz offset)</td>
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<tr>
<td>-75.2 to -75.86</td>
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<tr>
<td>(1MHz offset)</td>
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<tr>
<td>-81</td>
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<tr>
<td>-88</td>
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<td></td>
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<tr>
<td><strong>Supply voltage [V]</strong></td>
</tr>
<tr>
<td>-4.3, -5.0</td>
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<tr>
<td>-4.3, -5.0</td>
</tr>
<tr>
<td>1.8, 2.5, 3.3</td>
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<tr>
<td>1.5, 0.8</td>
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<tr>
<td>1.2, 1.3</td>
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<tr>
<td>5.5</td>
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<tr>
<td>1.45</td>
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<td></td>
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<tr>
<td><strong>P_{OUT} [dBm]</strong></td>
</tr>
<tr>
<td>-23</td>
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<tr>
<td>-1 (estimated)</td>
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<tr>
<td>-25 @163GHz</td>
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<tr>
<td>-3 @90GHz</td>
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<tr>
<td>-10 @50GHz</td>
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<tr>
<td>-31 to -22 @100GHz</td>
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<td>-</td>
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<td>-</td>
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<td></td>
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<tr>
<td><strong>P_{DC} [mW]</strong></td>
</tr>
<tr>
<td>301.6</td>
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<tr>
<td>465.3</td>
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<tr>
<td>1,150 to 1,250</td>
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<tr>
<td>57</td>
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<tr>
<td>43.7</td>
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<tr>
<td>-</td>
</tr>
<tr>
<td>88*</td>
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<tr>
<td><strong>Chip area [mm^2]</strong></td>
</tr>
<tr>
<td>1.38×0.61</td>
</tr>
<tr>
<td>1.57×0.7</td>
</tr>
<tr>
<td>1.1×1.7</td>
</tr>
<tr>
<td>1.16×0.75</td>
</tr>
<tr>
<td>1×0.7</td>
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<tr>
<td>-</td>
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<tr>
<td>1×0.8</td>
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</tbody>
</table>

*Using the second order harmonic  
# Excluding the output buffer

### References


