InGaAs/InP DHBTs demonstrating simultaneous $f_t/f_{max} \sim 460/850$ GHz in a refractory emitter process

Vibhor Jain, Evan Lobisser, Ashish Baraskar, Brian J Thibeault, Mark Rodwell
ECE Department, University of California, Santa Barbara, CA 93106-9560

Miguel Urteaga
Teledyne Scientific & Imaging, Thousand Oaks, CA 91360

D Loubychev, A Snyder, Y Wu, J M Fastenau, W K Liu
IQE Inc., 119 Technology Drive, Bethlehem, PA 18015

vibhor@ece.ucsb.edu, 805-893-3273
Outline

• Need for high speed HBTs
• HBT Scaling Laws
• Fabrication
  – Challenges
  – Process Development
• DHBT
  – Epitaxial Design
  – Results
• Summary
Why THz Transistors?

- High gain at microwave frequencies → precision analog design, high resolution ADC & DAC, high performance receivers
- THz amplifiers for imaging, sensing, communications
- Digital Logic for Optical fiber circuits
Bipolar transistor scaling laws

\[
\frac{1}{2\pi f_r} = \tau_{tr} + RC
\]

\[
f_{\text{max}} = \sqrt{\frac{f_r}{8\pi R_{bb,\text{eff}} C_{cb,\text{eff}}}}
\]

To double cutoff frequencies of a mesa HBT, must:

Keep constant all resistances and currents

Reduce all capacitances and transit delays by 2

\[
\tau_b \approx T_b^2 / 2D_n + T_b / v_{\text{exit}}
\]

\[
\tau_c = T_c / 2v_{\text{sat}}
\]

\[
C_{cb} = \frac{\varepsilon A_c}{T_c}
\]

\[
I_{c,\text{max}} \propto v_{\text{eff}} A_e (V_{cb} + \phi_{bi}) / T_c^2
\]

\[
R_{ex} = \rho_{\text{contact}} / A_e
\]

\[
R_{bb} = \rho_{\text{sheet}} \left( \frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e} \right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}
\]

(emitter length \(L_e\))
Base Access Resistance

\[ f_{\text{max}} = \sqrt{\frac{f_{\tau}}{8\pi R_{bb} C_{cb}}} \]

\[ R_{bb} = \rho_{sh,e} \cdot \frac{W_e}{12L_e} + \rho_{sh,bc} \cdot \frac{W_{bc}}{6L_e} + \rho_{sh,gap} \cdot \frac{W_{gap}}{2L_e} + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}} \]

\[ \rho_{sh,gap} \gg \rho_{sh,e}, \rho_{sh,bc} \]

• Surface Depletion
• Process Damage

\[ \rightarrow \text{Need for very small } W_{gap} \]

• Small undercut in InP emitter
• Self-aligned base contact
Base-Emitter Short

Undercut in thick emitter semiconductor

Helps in Self Aligned Base Liftoff

For controlled semiconductor undercut

→ Thin semiconductor

To prevent base – emitter short

→ Vertical emitter profile and line of sight metal deposition

→ Shadowing effect due to high emitter aspect ratio
Composite Emitter Metal Stack

- W/TiW metal stack
- Low stress
- Refractory metal emitters
- Vertical dry etch profile

W emitter

TiW emitter

Erik Lind

Evan Lobisser
Vertical Emitter

Vertical etch profile
Low stress
High emitter yield
Scalable emitter process

100nm

BCB

TiW

Base Metal

SiN_x
Narrow Emitter Undercut

- InGaAs cap
- Mo contact
- InP emitter

Controlled InP undercut

Narrow BE gap

Dual SiN sidewall

Mo contact InGaAs cap
InP emitter

50nm
**Process flow**

**Mo contact to n- InGaAs for emitter**

- W/TiW/SiO$_2$/Cr dep
- SF$_6$/Ar etch
- SiN$_x$ Sidewall

**SiO$_2$/Cr removal**

- InGaAs Wet Etch

**Second SiN$_x$ Sidewall**

- InP Wet Etch

**Base Contact Lift-off**

*Base and collector* formed via *lift off* and *wet etch*

**BCB** used to passivate and planarize devices

**Self-aligned process flow for DHBTs**
Epitaxial Design

<table>
<thead>
<tr>
<th>T(nm)</th>
<th>Material</th>
<th>Doping (cm⁻³)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>In₀.₅₃Ga₀.₄₇As</td>
<td>8·10¹⁹ : Si</td>
<td>Emitter Cap</td>
</tr>
<tr>
<td>20</td>
<td>InP</td>
<td>5·10¹⁹ : Si</td>
<td>Emitter</td>
</tr>
<tr>
<td>15</td>
<td>InP</td>
<td>2·10¹⁸ : Si</td>
<td>Emitter</td>
</tr>
<tr>
<td>30</td>
<td>InGaAs</td>
<td>9·5·10¹⁹ : C</td>
<td>Base</td>
</tr>
<tr>
<td>13.5</td>
<td>In₀.₅₃Ga₀.₄₇As</td>
<td>5·10¹⁶ : Si</td>
<td>Setback</td>
</tr>
<tr>
<td>16.5</td>
<td>InGaAs / InAlAs</td>
<td>5·10¹⁶ : Si</td>
<td>B-C Grade</td>
</tr>
<tr>
<td>3</td>
<td>InP</td>
<td>3.6·10¹⁸ : Si</td>
<td>Pulse doping</td>
</tr>
<tr>
<td>67</td>
<td>InP</td>
<td>5·10¹⁶ : Si</td>
<td>Collector</td>
</tr>
<tr>
<td>7.5</td>
<td>InP</td>
<td>1·10¹⁹ : Si</td>
<td>Sub Collector</td>
</tr>
<tr>
<td>5</td>
<td>In₀.₅₃Ga₀.₄₇As</td>
<td>4·10¹⁹ : Si</td>
<td>Sub Collector</td>
</tr>
<tr>
<td>300</td>
<td>InP</td>
<td>2·10¹⁹ : Si</td>
<td>Sub Collector</td>
</tr>
<tr>
<td></td>
<td>SI : InP</td>
<td></td>
<td>Substrate</td>
</tr>
</tbody>
</table>

\[ V_{be} = 1 \text{ V}, \ V_{cb} = 0.7 \text{ V}, \ J_e = 24 \text{ mA/\mu m}^2 \]

Thin emitter semiconductor

→ Enables wet etching
Results - DC Measurements

$\text{BV}_{ceo} = 3.7 \text{ V} @ J_e = 10 \text{ kA/cm}^2$

$\beta = 20$

Base $\rho_{sh} = 710 \Omega/\text{sq}, \rho_c < 5 \Omega\cdot \mu\text{m}^2$

Collector $\rho_{sh} = 15 \Omega/\text{sq}, \rho_c = 22 \Omega\cdot \mu\text{m}^2$

@Peak $f_\tau, f_{\text{max}}$

$J_e = 19.4 \text{ mA/}\mu\text{m}^2$

$P = 32 \text{ mW/}\mu\text{m}^2$

Common emitter I-V

Solid line: $V_{cb} = 0.7\text{V}$

Dashed: $V_{cb} = 0\text{V}$

$n_c = 1.17$

$n_b = 1.98$

Gummel plot
1-67 GHz RF Data

- \( I_c = 11.5 \text{ mA} \)
- \( V_{ce} = 1.66 \text{ V} \)
- \( J_e = 19.4 \text{ mA/\mu m}^2 \)
- \( V_{cb} = 0.7 \text{ V} \)

- Single-pole fit to obtain cut-off frequencies

- \( f_{\text{max}} = 850 \text{ GHz} \)
- \( f_{\tau} = 460 \text{ GHz} \)

- \( A_{je} = 0.22 \times 2.7 \text{ \mu m}^2 \)
Parameter Extraction

$J_{kirk} = 23 \text{ mA/}\mu\text{m}^2 \text{ (@} V_{cb} = 0.7\text{V)}$
**Equivalent Circuit**

\[ R_{\text{ex}} < 4 \ \Omega \cdot \mu \text{m}^2 \]

**Hybrid-\( \pi \) equivalent circuit from measured RF data**

\[ C_{\text{cb,x}} = 3.71 \ \text{fF} \]
\[ C_{\text{cb,i}} = 0.81 \ \text{fF} \]
\[ R_{\text{cb}} = 34 \ \text{k}\Omega \]
\[ R_{\text{c}} = 4.7 \ \Omega \]
\[ R_{\text{bb}} = 30 \ \Omega \]
\[ R_{\text{be}} = 121 \ \Omega \]
\[ C_{\text{cg}} = 3.6 \ \text{fF} \]

**S-parameters**

- **S(1,1)**
- **S(2,2)**
- **S(1,2)**
- **S(2,1)**

**Frequencies**

- **freq (1.000GHz to 67.00GHz)**
- **freq (100.0MHz to 67.00GHz)**

---

: Measured

x : Simulated
TEM – Wide base mesa

High $A_c/A_e$ ratio (>5)
High $R_{ex} \cdot C_{cb}$ delay
Low $f_\tau$

0.2 μm

220 nm
Summary

- Demonstrated DHBTs with peak $f_{\tau} / f_{\text{max}} = 460/850$ GHz
- Small $W_{\text{gap}}$ for reduced base access resistance $\rightarrow$ High $f_{\text{max}}$
- Narrow sidewalls, smaller base mesa and better base ohmics needed to enable higher bandwidth devices
Thank You

Questions?

This work was supported by the DARPA THETA program under HR0011-09-C-006.

A portion of this work was done in the UCSB nanofabrication facility, part of NSF funded NNIN network and MRL Central Facilities supported by the MRSEC Program of the NSF under award No. MR05-20415