40Gbit/s Coherent Optical Receiver Using a Costas Loop

University of California at Santa Barbara
Introductions

Motivations

- Higher Spectral Efficiency – QPSK / multi-level QAMs
- Higher Data Rates – 40Gbit/s, 100Gbit/s, and even higher
- Higher Receiving Sensitivity

Recent Coherent Optical Communication

- Coherent detection based on DSP
  - Local oscillator (LO) laser
  - Polarization diversity 90° optical hybrid
  - Balanced detectors
  - High speed analog to digital convertor (ADC)
  - High speed digital signal processing (DSP)
Coherent Optical Communications

Coherent Optical Receiver – I

Advantages:
• Multi-level constellations
• High data rate
• Phase managements
• Polarization managements

Dis-advantages:
• Electrical circuit complexity
• Speed limitations
• Cost issues
• Power consumptions
Coherent Optical Communications

Coherent Optical Receiver – II

- Homodyne OPLL based coherent receiver – **Costas Loop**
- Optical carrier recovering technique

**Requiring Stable OPLL**
Coherent Optical Communications

Coherent Optical Receiver – II

• Challenges:
  • Long loop delays (*1ns)
  • Narrow loop bandwidth (*100MHz)
  • Transmitting and LO lasers’ linewidth
  • Sensitive by external variations

• Solutions:
  • Integrated circuits (photonic IC, electrical IC)
  • Feed-forward loop filter topology
  • Minimizing Interconnection delays
  • Digitally operating feedback system
Phase Locked Coherent BPSK Receiver

Homodyne OPLL + Costas Loop

- Three blocks: photonic IC, electrical IC, and hybrid loop filter
- High speed BPSK data demodulations
Phase Locked Coherent BPSK Receiver

Photonic IC

- SG-DBR laser – 40nm tunable ranges
- 90° optical hybrid
- 4 un-balance photodiodes – 30GHz bandwidth
Phase Locked Coherent BPSK Receiver

Diagram of a Phase Locked Coherent BPSK Receiver with components labeled:
- BPSK Mod. IN
- LO
- Optical Hybrid
- Photonic IC
- Electrical IC
- Limiting Amps
- Binary PFD
- BPSK Outputs
- Hybrid Loop Filter
Phase Locked Coherent BPSK Receiver

Electrical IC

- Limiting amplifiers
- Phase / frequency detector (PFD) – XOR + delay line

Teledyne’s 500nm InP HBT 300GHz $f_t / f_{max}$
Phase Locked Coherent BPSK Receiver
Phase Locked Coherent BPSK Receiver

Loop Filter

*Challenges:
1. OP amp has lots of delays
2. OP amps bandwidth is limited (100MHz)

- Main path by integrator – high gain at DC and low frequencies
- Feed-forward path – passive capacitor component

**Open Loop Responses**

- Conventional Loop Filter
- Passive Path for Wide Bandwidth
- Integrator Path for High DC gain

![Diagram of Loop Filter and Open Loop Responses](image-url)
Phase Locked Coherent BPSK Receiver

Integration on a Single Carrier board

- Compact chip size of 10 x 10mm²
- Total delay (120ps)=PIC (40ps)+EIC (50ps)+Interconnection (30ps)

1GHz Loop Bandwidth is feasible
Test Results – Homodyne OPLL

Beating spectrum: locked SG-DBR + Ref. with 100MHz mod.

1.1GHz closed loop bandwidth

Beating laser tones at 100MHz

0 500M 1G 1.5G 2G

Frequency (Hz)

PSD (dBm/RBW)

Left peak

Right peak

1.1GHz LBW
Cross correlation between SG-DBR and reference lasers

-100dBc/Hz @ above 50kHz
Test Results – Homodyne OPLL

Linewidth using self-heterodyne with 25km optical fiber

10MHz linewidth for free-running SG-DBR

![Graph showing linewidth results](image)

- 50MHz Span
- 50kHz RBW
- 10MHz
Reference laser (Koshin) linewidth 100kHz

100kHz linewidth for locked SG-DBR laser

![Graph showing PSD vs. Frequency with labels: Locked SGDBR only, Locked SGDBR w/ BPSK, Free Running SGDBR, Reference Laser. The graph highlights a 100kHz span with 3kHz RBW.](image-url)
Test Results – Homodyne OPLL

400MHz/512bits ON-OFF laser

*Locking conditions: EIC output – DC, External PD output – 100MHz*
Test Results – Homodyne OPLL

* Frequency pull-in time $\sim 600\text{ns}$

* Phase lock time $< 10\text{ns}$

* Worst conditions
Test Results – BPSK Receiver

**PRBS $2^{31}-1$ signals – up to 40Gb/s BPSK data**

*Open eye diagrams for 25Gb/s and 40Gb/s*

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**Diagram Description**

- **Homodyne OPLL Costas Loop**
- **OSA**
- **Optical Oscilloscope**
- **Pattern Generator**
- **ECL**
- **OSA**
- **ESA**

**Equipment and Devices**

- **50Gb/s BERT**
- **XOR 50Gb/s**
- **70GHz Oscilloscope**
- **PIC**
- **Loop Filter**
- **Carrier**
- **PC**
- **BPF**
- **EDFA**
- **VOA**
- **MZM**
- **AOM**
- **PD**
- **Amps**

**Test Conditions**

- **25Gb/s**
- **40Gb/s**

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**Additional Information**

- BPSK Receiver
- PRBS 2^{31}-1 signals
- Up to 40Gb/s BPSK data
- Open eye diagrams for 25Gb/s and 40Gb/s
Test Results – BPSK Receiver

BER vs. OSNR (20Gb/s to 40Gb/s)

Error-free up to 35Gb/s, < 1.0E-7 @ 40Gb/s
Conclusions

- The first demonstration highly integrated optical Costas loop receiver
- Integrated PIC, integrated EIC, and feed-forward loop filter
- The receiver is integrated within 10x10mm²
- A stable homodyne OPLL by 120ps delay and 1.1GHz loop bandwidth
- 40Gbit/s BPSK coherent optical receiver (BER < 1.0e-7)
- Error-free (BER < 1.0e-12) up to 35Gbit/s

Future works: QPSK receivers / long haul tests / dispersion compensations / polarization managements

Thank you for your attention!