High-Speed Track-and-Hold Circuit Design

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Outline

• 250 nm InP HBT technology review
• Applications and Motivation
• Key design features and contributions
• Review of circuit design and layout
• Measurement results and comparison
TSC 250nm InP HBT Process

- Four metal interconnect stack
- Peak bandwidth of $f_{\text{max}} = 700$ GHz & $f_{t} = 400$ GHz
- MIM caps of 0.3 fF/μm²
- Thin-film resistors 50 Ω/square

Plot courtesy Zach Griffith, UCSB 250nm InP HBT, 2007
Wideband Sample & Hold Applications

- **Sub-sampling applications:** automated test equipment (ATE), oscilloscope, jitter measurement ...

  ![Sampling Clock](image1)
  ![Signal Under Test](image2)
  ![Sampled Signal](image3)

- **Undersampling applications:** undersampling receivers

  Direct conversion receiver:
  - Problems such as DC offset, noise, distortion, I/Q mismatch, etc

  Undersampling receiver:
  - T/H replaces downconversion mixer
  - Eliminates IF filter, IF gain stages, mixer and high frequency LO
  - DC offset, IQ mismatch problem goes away
  - Noise folding is a problem

Slide courtesy MJC Teledyne
Motivation: Sample & Hold vs Track & Hold
High Frequency Sampling Techniques

Diode bridge: [1]

- ☀ Wide bandwidth
- ☀ Linearity
- ☀ Dynamic Range

Switched Emitter Follower (SEF): [2]

- ☀ Good linearity
- ☀ Better dynamic range
- ☋ Stability issues with EF

Base-collector diode:

- ☀ Widest bandwidth
- ☀ Good linearity
- ☀ Highest dynamic range
- ☀ No stability issues
- ☀ Flat AC response

Key Design Features

Track & hold switch: base-collector diode
- lower $R_{on}$, lower $C_{off}$ than HBT e-b junction
- minority carrier storage time approximately equal to base transit time

Common reports in the literature:
- switch voltage swings set very small and fast,
  but high IP3 only for $f_{\text{signal}} << f_{\text{Nyquist}}$

Real-world design requires:
- switch voltages set for high IP3 with Nyquist-frequency input

Linearization of input buffer for high IP3
- cubic feedforward path cancels IM3 from differential pair
Input Buffer & TH Switch
Input Buffer & TH Switch

T&H Switch (in Hold mode)  Input Buffer  T&H Switch (in Track mode)
\[ v_o(t) \approx \alpha_0 + \alpha_1 v_i(t) + \alpha_2 v_i^2(t) + \alpha_3 v_i^3(t), \quad (1) \]

\[ v_i(t) = V_p \sin \omega t \]

\[ HD_3 = \frac{1}{4} \frac{\alpha_3}{\alpha_1} V_p^2 \]

\[ \alpha_1 = \frac{v_o}{v_i} = \frac{-Z_L}{Z_L + r_{ex2} + 1/g_{m2}} \left[ \frac{r_{ex2} + 1/g_{m2}}{R_{EE1} + 1/g_{m1}} + \frac{R_L}{R_{EE3} + 1/g_{m3}} \right] \]

Nonlinearity Derivation-II

\[
\begin{align*}
\delta i_{c1} &= \frac{1}{g_{m1}} \frac{1}{R_{EE1} + 1/g_{m1}} \delta v_i, \\
\delta i_{c3} &= \frac{1}{g_{m3}} \frac{1}{R_{EE3} + 1/g_{m3}} \delta v_i, \\
\delta i_o &= \frac{-1}{Z_L + r_{ex2} + 1/g_{m2}} \left[ \frac{r_{ex2} + 1/g_{m2}}{R_{EE1} + 1/g_{m1}} + \frac{R_L}{R_{EE3} + 1/g_{m3}} \right] \delta v_i, \\
\delta i_{r2} &= \delta i_{r1} + \delta i_n. \\
\delta v_{be1} &= \left( \frac{V_T}{I_{DC1}} \right) \delta i_{C1} - \left( \frac{V_T}{2I_{DC1}^2} \right) \delta i_{C1}^2 + \left( \frac{V_T}{3I_{DC1}^3} \right) \delta i_{C1}^3 \\
\delta v_{be2} &= \left( \frac{V_T}{I_{DC2}} \right) \delta i_{C2} - \left( \frac{V_T}{2I_{DC2}^2} \right) \delta i_{C2}^2 + \left( \frac{V_T}{3I_{DC2}^3} \right) \delta i_{C2}^3 \\
\delta v_{be3} &= \left( \frac{V_T}{I_{DC3}} \right) \delta i_{C3} - \left( \frac{V_T}{2I_{DC3}^2} \right) \delta i_{C3}^2 + \left( \frac{V_T}{3I_{DC3}^3} \right) \delta i_{C3}^3 \\
\delta v_{be1\Theta} &= \left( \frac{V_T}{3I_{DC1}^3} \right) \left( \frac{1}{g_{m1}} \right) \frac{1}{R_{EE1} + 1/g_{m1}} \delta v_i^3 \\
\delta v_{be2\Theta} &= \left( \frac{V_T}{3I_{DC2}^3} \right) \left[ \frac{1}{g_{m1}} \frac{1}{R_{EE1} + 1/g_{m1}} - \frac{1}{Z_L + r_{ex2} + 1/g_{m2}} \times \left( \frac{r_{ex2} + 1/g_{m2}}{R_{EE1} + 1/g_{m1}} + \frac{R_L}{R_{EE3} + 1/g_{m3}} \right) \right] \delta v_i^3 \\
\delta v_{be3\Theta} &= \left( \frac{V_T}{3I_{DC3}^3} \right) \left( \frac{1}{g_{m3}} \right) \frac{1}{R_{EE3} + 1/g_{m3}} \delta v_i^3
\end{align*}
\]
Nonlinearity Derivation - III

\[
\delta v_o = \frac{Z_L}{\delta v_{be1} \left( r_{ex2} + \frac{1}{g_m2} \right)} \times \frac{1}{\delta v_{be1} \left( r_{ex2} + \frac{1}{g_m2} \right)}
\]

\[
\delta v_o = \frac{Z_{IP3}}{\delta v_{be1}}
\]

\[
\delta v_o = \frac{Z_{IP3}}{\delta v_{be1}}
\]

\[
\delta v_o = \frac{Z_{IP3}}{\delta v_{be1}}
\]

\[
R_{EE} = R_L + r_{ex2} + 1/g_m
\]

\[
k_1 = k_2 = k_3 = 1
\]

\[
IM_3 \approx \frac{-V_T^4V_P^2}{4I_{DC}^3R_{EE}^3 \left( r_{ex2} + \frac{1}{k_2g_m} + \frac{R_L}{k_1} \right)} \times \left[ \frac{R_{EE}}{k_2^2} \left( \frac{g_m \left( \frac{R_L}{k_1} + r_{ex2} + \frac{1}{k_2g_m} \right)}{Z_L + r_{ex2} + \frac{1}{k_2g_m}} - 1 \right)^3 + \frac{R_L}{k_3^2k_1^4 + r_{ex2} + \frac{1}{k_2g_m}} \right]
\]
Output Buffer & Output Driver
Output Buffer & Output Driver

- Output buffer should always be **on** in Sample & Hold circuit.

- Output stage needs to be designed linear enough not to affect total nonlinearity of the circuit.
Layout (Signal path)
S-parameters measurement

![Diagram of a circuit with T&H Switches and buffers, and a graph showing S-parameters (S21, S22, S11) vs. Frequency (GHz).]
Clock Distribution Circuit
Clock Distribution Circuit

$I_{tail} = 6 \text{ mA}$

$I_{tail} = 12 \text{ mA}$
Clock Distribution Circuit - layout
Transient and Linearity Measurements

10 GHz RF input signal with a 50 GHz clock

IIP3 & OIP3 vs Fin for Fclk = 50GHz
THD and Beat test Measurements

Measured HD$_2$ and HD$_3$

40.002 GHz input signal is being sampled by 40 GSamples/s sampling rate.
## Comparison with the State of the Art Works

<table>
<thead>
<tr>
<th>Reference</th>
<th>Sample Rate (GS/s)</th>
<th>BW (GHz)</th>
<th>Input Range Output Range</th>
<th>IIP3 @ $f_{in}/f_s$ (dBm @ GHz/GHz)</th>
<th>Power (mW)</th>
<th>$V_{Supply}$ (V)</th>
<th>Die-Size (mm$^2$)</th>
<th>Process</th>
<th>$f_t$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>30</td>
<td>7</td>
<td>$&lt;-12$ dBm $&lt;150$ mV$_{pp}$</td>
<td>1@5/30 0@9/30</td>
<td>270</td>
<td>1.8</td>
<td>1.0</td>
<td>CMOS</td>
<td></td>
</tr>
<tr>
<td>[2]</td>
<td>40</td>
<td>43</td>
<td>$&lt;-8$ dBm $&lt;500$ mV$_{pp}$</td>
<td>8@6/40 0@19/40</td>
<td>540</td>
<td>3.6</td>
<td>1.0 $\times$ 1.1</td>
<td>SiGe HBT 160 GHz</td>
<td></td>
</tr>
<tr>
<td>[3]</td>
<td>50</td>
<td>42</td>
<td>0 dBm N.A.</td>
<td>21@30/50</td>
<td>640</td>
<td>4.3</td>
<td>1.28 $\times$ 1.15</td>
<td>SiGe BiCMOS</td>
<td></td>
</tr>
<tr>
<td>[4]</td>
<td>20</td>
<td>20</td>
<td>500 mV$_{pp}$</td>
<td>16@2/20</td>
<td>1990</td>
<td>-6</td>
<td>1.6 $\times$ 1.4</td>
<td>InP HBT 210 GHz</td>
<td></td>
</tr>
<tr>
<td>[5]</td>
<td>40</td>
<td>16</td>
<td>1000 mV$<em>{pp}$ $&lt;100$ mV$</em>{pp}$</td>
<td>15.6@10/40</td>
<td>560</td>
<td>5.5</td>
<td>1.8 $\times$ 1.0</td>
<td>SiGe HBT 200 GHz</td>
<td></td>
</tr>
<tr>
<td>[6]</td>
<td>40</td>
<td>27</td>
<td>7 dBm N.A.</td>
<td>N.A.</td>
<td>1900</td>
<td>-6</td>
<td>1.4 $\times$ 1.6</td>
<td>InP DHBT 210 GHz</td>
<td></td>
</tr>
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</table>

**This work**

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<th>$f_t$</th>
</tr>
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<tbody>
<tr>
<td>50</td>
<td>40</td>
<td>9 dBm 800 mV$_{pp}$</td>
<td>20.7@6/40 19.7@10/40 17.4@18/40 16.7@22/40</td>
<td>1200</td>
<td>-5, -2.5</td>
<td>0.875 $\times$ 1.075</td>
<td>InP HBT 400 GHz</td>
<td></td>
</tr>
</tbody>
</table>

**References**


Questions?
T&H Chip layout
S&H Chip layout
Sample & Hold Transient waveforms

- 10 GHz RF input signal is being sampled by a 50 GHz clock

**Differential**

**Single-ended**
Sample & Hold Beat frequency test

**Simulation**

Fin=20.5 GHz, Fclk=20 GHz

**Experiment**

Fin=20.5 GHz, Fclk=10 GHz
Sample & Hold Linearity Measurements

Calculated ENOB using simulated noise figure of 20dB is more than 6bits.
Base-Collector Diode modeling - I

\[ W = 0.6\mu m, \quad L_B = 2.4\mu m \]
\[ \text{Area} = 1.6\mu m \times 1.6\mu m + W \times L_B \]

\[ D_1: \quad I_{S1} = \frac{2.45e-10}{\text{Area}}, \quad N = 1.9, \quad T_t = 50 \text{ fsec} \]

\[ D_2: \quad I_{S2} = \frac{1.47e-12}{\text{Area}}, \quad N = 1.3 \]

\[ D_3: \quad I_{S3} = \frac{2.38e-9}{\text{Area}}, \quad N = 20.7 \]

\[ R_1 = \frac{\rho_{cp}}{\text{Area}} = \frac{6e-12}{\text{Area}} \]

\[ R_2 = \frac{78e-12}{\text{Area}}, \quad R_1 + R_2 = 21\Omega. \]

\[ C = \frac{a_5 V_C^5 + a_4 V_C^4 + a_3 V_C^3 + a_2 V_C^2 + a_1 V_C + a_0}{\text{Area}} \]

- \( a_5 = -0.007 \text{ fF} \)
- \( a_4 = 0.209 \text{ fF} \)
- \( a_3 = 2.345 \text{ fF} \)
- \( a_2 = 7.705 \text{ fF} \)
- \( a_1 = 9.557 \text{ fF} \)
- \( a_0 = 7.637 \text{ fF} \)
Base Collector Diode modeling - II

I-V Characteristic
Forward biased

I-V Characteristic
Reverse biased