A DC-100 GHz Bandwidth and 20.5 dB Gain Limiting Amplifier in 0.25μm InP DHBT Technology

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Outline

• Application and Motivation of the work
• TSC 250nm HBT process overview
• Block diagram & schematic of the circuit
• Layout & EM modeling
• Measurement results and comparison table
Motivation - I

50 GSample/sec Sample & Hold circuit
Motivation - II

50 GHz clock circuit

CSICS 2013 Monterey, California
Applications - I

• **High speed optoelectronic** signal conversion requires broadband receivers

• **Limiting amplifiers** are the key components in these receivers in order to:

  ✓ Provide a **low input sensitivity** and **sufficient gain** to achieve saturated output levels from small-signal inputs which enables **reliable decision making**

  ✓ Provide a **wide bandwidth** to achieve **short rise and fall times** in order to provide an output signal with minimum distortion
TSC 250nm InP HBT process

- Four metal interconnect stack
- Peak bandwidth of $f_t = 400 \text{ GHz}$ & $f_{\text{max}} = 700 \text{ GHz}$
- MIM caps of 0.3 fF/μm²
- Thin-film resistors 50 Ω/square

Plot courtesy Zach Griffith, UCSB 250nm InP HBT, 2007

Representative cross-section of TSC250 IC technology. Drawing is not to scale.
Modified Cherry-Hooper stage [1-3]

Large signal behavior:

\[ V_{o1} - V_{o2} \approx (R_1 + R_2)I_{EE2} \cdot \tanh \left( \frac{V_2 - V_1}{2V_T} \right) \]

Conventional C-H amp. gain \( \approx g_{m1-2} R_F \)

Modified C-H amp. provides gain enhancement by a factor of \( 1 + \frac{R_2}{R_1} \) while \( 0 < \frac{R_2}{R_1} < 2.5 \)


Single-ended gain and BW measurements have been chosen due to unavailability of 4-port s-param measurement for frequencies > 67 GHz

→ ~6dB gain has been added to get the differential equivalent
R_1 = 30 \, \Omega

R_2 = 50 \, \Omega

R_F = 40 \, \Omega

Q_{1-8} = 3 \times 0.25 \, \mu m
Compact layout
Symmetric layout
EM Simulation

Whole chip has been modeled using ADS momentum EM simulator
S-parameter measurement results - I

Single-ended insertion loss

- $S_{21} = 14.5$ dB, 3dB BW = 100 GHz
- $S_{21}$ gain ripple < ±0.5 dB

Single-ended input and output return loss

- $S_{11} < -20$ dB, $S_{22} < -15$ dB
S-parameter measurement results - II

Rollet Stability factor

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \]
\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \]

Group Delay

\[ \tau_{\text{Group Delay}} = -\frac{d\phi}{d\omega} = -\frac{d\theta}{df \cdot 360^\circ} \]

Group delay \(\approx 9\) psec
Group delay variation = 11 psec
Eye diagrams @ 30 Gb/s

Input eye @ 30 Gb/s
- 47 mVpp
- 12 mV
- 5.5 psec

Output eye @ 30 Gb/s
- 221 mVpp
- 50 mV
- 5.7 psec

Input eye @ 30 Gb/s
- 436 mVpp
- 100 mV
- 6.1 psec

Output eye @ 30 Gb/s
- 260 mVpp
- 60 mV
- 5.3 psec

Small Signal

Large Signal
Eye diagrams @ 40 Gb/s

Small Signal
- Input eye @ 40 Gb/s: 47 mVpp
- Output eye @ 40 Gb/s: 219 mVpp

Large Signal
- Input eye @ 40 Gb/s: 433 mVpp
- Output eye @ 40 Gb/s: 257 mVpp
Comparison table

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Gain(^s) (dB)</th>
<th>Gain(^D)(^s) (dB)</th>
<th>BW(^\dagger) (GHz)</th>
<th>GBW(^\dagger) (GHz)</th>
<th>IRL(^\dagger) (dB)</th>
<th>ORL(^\dagger) (dB)</th>
<th>GR(^\diamond) (dB)</th>
<th>GD(^\diamond) (ps)</th>
<th>Supply (V)</th>
<th>Power (mW)</th>
<th>Area (mm(^2))</th>
<th>GBW/P(_{DC}) (GHz/mW)</th>
<th>Architecture</th>
<th>Process</th>
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<tbody>
<tr>
<td>[1]</td>
<td>11</td>
<td>-</td>
<td>90</td>
<td>320</td>
<td>&gt; 5</td>
<td>&gt; 7</td>
<td>2.4</td>
<td>2.5</td>
<td>210</td>
<td>1.28</td>
<td>1.52</td>
<td>DA(^1)</td>
<td>0.12(\mu)m SOI CMOS</td>
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<tr>
<td>[4]</td>
<td>7</td>
<td>13</td>
<td>81</td>
<td>362</td>
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<td>&gt; 7</td>
<td>5.5</td>
<td>-</td>
<td>495</td>
<td>1.17</td>
<td>0.73</td>
<td>DA(^1)</td>
<td>SiGe (f_T=200) GHz</td>
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<tr>
<td>[5]</td>
<td>10</td>
<td>16</td>
<td>62</td>
<td>391</td>
<td>&gt; 11</td>
<td>&gt; 3</td>
<td>&gt; 3</td>
<td>-</td>
<td>775</td>
<td>0.3</td>
<td>0.51</td>
<td>EF &amp; DP(^2)</td>
<td>SiGe (f_T=200) GHz</td>
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<tr>
<td>[6]</td>
<td>14</td>
<td>20</td>
<td>84</td>
<td>840</td>
<td>&gt; 7</td>
<td>&gt; 7</td>
<td>4</td>
<td>(\pm 32)</td>
<td>-5.5</td>
<td>990</td>
<td>0.63</td>
<td>EF &amp; CA(^3)</td>
<td>0.18(\mu)m SiGe</td>
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<tr>
<td>[7]</td>
<td>-1</td>
<td>5</td>
<td>62</td>
<td>110</td>
<td>&gt; 14</td>
<td>-</td>
<td>&gt; 3</td>
<td>-</td>
<td>125</td>
<td>-</td>
<td>0.88</td>
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<td>[8]</td>
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<td>&gt; 9</td>
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<td>(\pm 6)</td>
<td>2</td>
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<td>[9]</td>
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<td>43</td>
<td>1360</td>
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<td>&gt; 7</td>
<td>&gt; 2</td>
<td>(\pm 10)</td>
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<td>500</td>
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<td>EF &amp; CH(^4)</td>
<td>1(\mu)m InP SHBT</td>
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<tr>
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<td>EF &amp; CH(^4)</td>
<td>InGaAs-InP HBT</td>
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<td>67</td>
<td>729</td>
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<td>(\pm 10)</td>
<td>3.5</td>
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<td>0.09</td>
<td>EF &amp; CH(^4)</td>
<td>0.5(\mu)m InP DHBT</td>
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<tr>
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<td>-</td>
<td>120</td>
<td>1350</td>
<td>-10</td>
<td>-10</td>
<td>3</td>
<td>(\pm 15)</td>
<td>610</td>
<td>2</td>
<td>2.21</td>
<td>DA(^1)</td>
<td>InP DHBT</td>
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<td>110</td>
<td>694</td>
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<td>&gt; 5</td>
<td>&gt; 3</td>
<td>-4</td>
<td>304</td>
<td>0.95</td>
<td>2.28</td>
<td>EF &amp; CH(^4)</td>
<td>0.25(\mu)m InP DHBT</td>
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</tr>
</tbody>
</table>

This work: 14.5 20.5 100 1060 > 20 > 15 1 ±5.5 > 15 7.31 EF & CH\(^4\) 0.25\(\mu\)m InP DHBT

\(^s\) Measured single-ended \(S_{21}\) gain, \(^D\) Inferred differential \(S_{21}\) gain, \(^\dagger\) 3-dB bandwidth of \(S_{21}\), \(^\diamond\) Inferred differential \(S_{21}\) gain \(\times\) its 3-dB bandwidth, \(^\dagger\) Input return loss, \(^\dagger\) Output return loss, \(^\diamond\) Total \(S_{21}\) gain ripple, \(^\diamond\) Group delay variation of \(S_{21}\), \(^1\) Distributed amplifier, \(^2\) Emitter follower & differential pair, \(^3\) Emitter follower & cascode stage, \(^4\) Emitter follower & Cherry-Hooper stage, \(^5\) Darlington feedback amplifier & constructive wave amplifier.
Thank you for your listening