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Reduction of leakage current in In$_{0.53}$Ga$_{0.47}$As channel metal-oxide-semiconductor field-effect-transistors using AlAs$_{0.56}$Sb$_{0.44}$ confinement layers


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We compare the DC characteristics of planar In$_{0.53}$Ga$_{0.47}$As channel MOSFETs using AlAs$_{0.56}$Sb$_{0.44}$ barriers to similar MOSFETs using In$_{0.52}$Al$_{0.48}$As barriers. AlAs$_{0.56}$Sb$_{0.44}$, with ~1.0 eV conduction-band offset to In$_{0.53}$Ga$_{0.47}$As, improves electron confinement within the channel. At gate lengths below 100 nm and $V_{DS}$ = 0.5 V, the MOSFETs with AlAs$_{0.56}$Sb$_{0.44}$ barriers show steeper subthreshold swing (SS) and reduced drain-source leakage current. We attribute the greater leakage observed with the In$_{0.52}$Al$_{0.48}$As barrier to thermionic emission from the N$^+$ In$_{0.53}$Ga$_{0.47}$As source over the In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As heterointerface. A 56 nm gate length device with the AlAs$_{0.56}$Sb$_{0.44}$ barrier exhibits 1.96 mS/μm peak transconductance and SS = 134 mV/dec at $V_{DS}$ = 0.5 V. © 2013 AIP Publishing LLC.

Driven by the potential for improved on-current over Si, InAs/In$_{0.53}$Ga$_{0.47}$As and In$_{0.53}$Ga$_{0.47}$As channel materials are being investigated to replace Si in future generations of CMOS VLSI. To date, most reported III-V MOSFETs grown lattice-matched to InP use In$_{0.52}$Al$_{0.48}$As lower electron confinement (barrier) layers. For this barrier layer, the In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As conduction-band offset is approximately 0.52 eV. In the heavily doped source and drain regions, at ~4 × 10$^{19}$ cm$^{-3}$ doping, the electron Fermi level, $E_f$, is ~0.3–0.4 eV above the conduction band edge of In$_{0.53}$Ga$_{0.47}$As, leaving the In$_{0.52}$Al$_{0.48}$As conduction band energy, $E_c$, only ~0.1–0.2 eV above this Fermi level. This small barrier energy is insufficient to fully confine electrons in the channel; the thermionic emission current density over the barrier can be approximated by

$$J_{th} \approx q(kT/m^*)^{1/2}N_e \exp((E_f - E_c)/kT),$$

where $N_e = 2 \times 10^{17}$/cm$^3$ effective density of states of In$_{0.53}$Ga$_{0.47}$As and $m^*$ is the electron effective mass. Given a 0.2 eV barrier, this thermionic current is approximately 5 μA/μm$^2$. Given both small (<100 nm) separations between the N$^+$ source and drain, and significant (~500 mV) drain-source bias voltage, the drain-source field is large, and electrons thermally emitted from the N$^+$ source into the In$_{0.52}$Al$_{0.48}$As barrier layer are then carried under high field to the drain.

We here show that barrier leakage can be the dominant source of off-state leakage current in short-channel InGaAs MOSFETs with In$_{0.52}$Al$_{0.48}$As barriers and small separations between the N$^+$ source and drain. The magnitude of barrier leakage will depend in detail upon the MOSFET's source-drain structure; presence of an In$_{0.52}$Al$_{0.48}$As upper barrier layer between the In$_{0.53}$Ga$_{0.47}$As channel and the N$^+$ In$_{0.53}$Ga$_{0.47}$As source and drain will reduce the electron density within the channel, increasing ($E_c - E_f$) and thereby reducing the thermionic leakage. While in other reported III-V MOSFETs the separation between the N$^+$ source and drain is significantly greater than the gate length.

In this letter, we demonstrate In$_{0.53}$Ga$_{0.47}$As MOSFETs with an AlAs$_{0.56}$Sb$_{0.44}$ barrier layer, grown lattice-matched to an InP substrate, and compare its DC characteristics to that of similar MOSFETs using In$_{0.52}$Al$_{0.48}$As confinement layers. The In$_{0.53}$Ga$_{0.47}$As/AlAs$_{0.56}$Sb$_{0.44}$ conduction-band offset is ~1.0 eV, providing much greater suppression of barrier leakage current than provided by an In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As heterointerface. At gate lengths below 100 nm, and for 0.5 V drain-source bias voltage, the MOSFETs with AlAs$_{0.56}$Sb$_{0.44}$ barriers show steeper subthreshold swing and reduced off-state drain-source leakage current. A 56 nm gate length device shows 1.96 mS/μm peak transconductance and 134 mV/dec subthreshold swing, both measured at $V_{DS}$ = 0.5 V.

The epitaxial layer structures (Figure 1) were grown on semi-insulating InP substrates using solid-source molecular beam epitaxy. Sample A consists of a 400 nm non-intentionally doped (N.I.D.) In$_{0.53}$Ga$_{0.47}$As buffer layer, a 3 μm Si-doped (1.3 × 10$^{19}$ cm$^{-3}$) In$_{0.52}$Al$_{0.48}$As pulse doping layer, and a 10 nm In$_{0.53}$Ga$_{0.47}$As channel. Sample B consists of a 375 nm N.I.D. In$_{0.53}$Ga$_{0.47}$As buffer layer, a 25 nm N.I.D AlAs$_{0.56}$Sb$_{0.44}$ bottom barrier layer, a 3 μm Si-doped (1.3 × 10$^{19}$ cm$^{-3}$) In$_{0.52}$Al$_{0.48}$As pulse doping layer, a 3 nm N.I.D AlAs$_{0.56}$Sb$_{0.44}$ spacer layer, and a 10 nm In$_{0.53}$Ga$_{0.47}$As channel, with details of AlAs$_{0.56}$Sb$_{0.44}$ growth as described in Ref. 8. To characterize the interface quality of In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As/AlAs$_{0.56}$Sb$_{0.44}$ heterojunctions, InGaAs single quantum well double heterostructures (DH) with 5 nm and 10 nm well thickness were grown and investigated. The detailed structures were presented in Ref. 8. The measured Hall...
The electron mobility for a 10 nm InGaAs quantum well is about $9500 \text{ cm}^2/\text{V} \cdot \text{s}$ at room temperature for both DHs with InAlAs barriers and AlAsSb barriers. As reducing the well thickness from 10 nm to 5 nm, the electron mobility significantly decreased and was lower for InGaAs/AlAsSb DHs than for InGaAs/InAlAs DHs. The decrease in mobility could be the result of stronger interface scattering associated with the higher conduction band offset of AlAsSb barriers, or a rougher interface for InGaAs grown on a higher aluminum content barrier layer.

To fabricate MOSFETs, hydrogen silsesquioxane (HSQ) dummy gates were patterned by e-beam lithography, and $50 \text{ nm}$ thick, $n$-type In$_{0.53}$Ga$_{0.47}$As (Si: $4 \times 10^{19} \text{ cm}^{-3}$) source-drain layers were regrown by metal organic chemical vapor deposition (MOCVD). After MOCVD regrowth, the dummy gates were removed in buffered HF. Channel surface damage caused by regrowth was then removed by two cycles of digital etching. The final In$_{0.53}$Ga$_{0.47}$As channel thickness is $7.5 \text{ nm}$ for both samples. Transistors were then mesa-isolated, were cleaned in buffered HF for 2 min and then in-situ cleaned in an atomic layer deposition (ALD) reactor using alternating cycle of nitrogen plasma and trimethylaluminum pretreatment. Approximately $3.9 \text{ nm}$ HfO$_2$ gate dielectric was then blanket-deposited. Samples were then annealed in forming gas (5% H$_2$/95% N$_2$) at $400^\circ \text{C}$ for 15 min. $35 \text{ nm}$/$120 \text{ nm}$ thermally evaporated Ni/Au gate metal and $20 \text{ nm}$/$50 \text{ nm}$/$100 \text{ nm}$ Ti/Pd/Au source/drain metal were then deposited and patterned by liftoff. Because AlAs$_{0.56}$Sb$_{0.44}$ is readily oxidized by air exposure and is etched during the mesa isolation, $0.75 \mu\text{m}$ mesa etch undercut is observed at the edge of the bottom barrier in the final devices. The final gate width determined by scanning electron microscope is $\sim 23.5 \mu\text{m}$ (25 $\mu\text{m}$ as drawn) for sample B.

Figure 2 shows the transfer characteristic of sample A and sample B, at 58 nm and 56 nm gate lengths ($L_g$) respectively. At $V_{DS} = 0.5 \text{ V}$, sample A shows 2.2 mS/$\mu\text{m}$ peak transconductance and 242 mV/dec subthreshold swing (SS), while sample B shows 1.96 mS/$\mu\text{m}$ peak transconductance and 134 mV/dec SS. The drain-source leakage current ($I_{DS}$ at, e.g., $V_{GS} = -0.2$ to $-0.4 \text{ V}$) is significantly reduced in sample B. The slightly reduced transconductance of sample B may be due to reduced mobility arising from stronger interface roughness scattering of InGaAs/AlAsSb heterojunction. As a function of gate lengths, threshold voltages are $0.1$–$0.15 \text{ V}$ more positive for sample B, possibly a result of the increased eigenstate energy in the InGaAs channel, also due to stronger quantum confinement.

Figures 3(a) and 3(b) compare the subthreshold characteristics of samples A and B as a function of gate lengths. With sample A (InAlAs barrier), the off-state drain leakage current ($I_{DS}$ at, e.g., $V_{GS} = -0.2$ to $-0.4 \text{ V}$) increases rapidly as $L_g$ is reduced from $558 \text{ nm}$ to $131 \text{ nm}$ and $58 \text{ nm}$, particularly for $V_{DS} = 0.5 \text{ V}$. At short gate lengths, $130 \text{ nm}$ and $56 \text{ nm}$ $L_g$, sample B (AlAsSb barrier) exhibits much smaller off-state leakage than sample A. For $L_g < 200 \text{ nm}$, sample B shows considerably smaller subthreshold swing as shown in Figure 3(c). Sample B shows a residual off-state leakage of

![Figure 1](image1.png)

**FIG. 1.** Structure of sample B (AlAs$_{0.56}$Sb$_{0.44}$ barrier). The pulse doping layer is $3 \text{ nm}$, $1.3 \times 10^{19} \text{ cm}^{-3}$ Si-doped In$_{0.52}$Al$_{0.48}$As. In sample A, the two AlAs$_{0.56}$Sb$_{0.44}$ layers are omitted and the In$_{0.52}$Al$_{0.48}$As buffer layer is $400 \text{ nm}$ thick. (N.I.D. = non-intentionally doped).

**TABLE I.** Comparison of Hall mobility between InGaAs/InAlAs and InGaAs/AlAsSb double heterostructures (detailed structures depicted in Ref. 8).

<table>
<thead>
<tr>
<th>Well thickness (nm)</th>
<th>Barrier layer</th>
<th>$N_s$, 300 K ($10^{12} \text{ cm}^{-2}$)</th>
<th>$\mu$, 300 K ($\text{cm}^2/\text{V} \cdot \text{s}$)</th>
</tr>
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<td>10</td>
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<td>9530</td>
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<tr>
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<td>AlAsSb</td>
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<td>9541</td>
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<td>6785</td>
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<tr>
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<td>AlAsSb</td>
<td>2.13</td>
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</table>

![Figure 2](image2.png)

**FIG. 2.** Transfer characteristics of (a) sample A with $L_g = 58 \text{ nm}$ and (b) sample B with $L_g = 56 \text{ nm}$ at $V_{DS}$ of 0.1, 0.3, and 0.5 V.
3–4 × 10⁻⁵ mA/µm at V_DS = 0.1 V and 2–3 × 10⁻⁴ mA/µm at V_DS = 0.5 V. This background leakage has an approximately linear (Ohmic) variation with V_DS, and is only weakly dependent upon the gate length; on other experimental samples, we have observed similar background leakage when the isolation mesa etch depth is insufficient.

Off-state drain leakage current arising from simple electrostatics (excessive channel or gate dielectric thickness) or from source-drain or band-band tunneling would not show the strong observed dependence upon the energy offset of the lower barrier. Leakage by thermal emission from the N+ source over the channel-barrier interface should however show a strong dependence upon the barrier energy, consistent with Figures 2 and 3.

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