THz Technologies:
Transistors, ICs, Systems

Mark Rodwell, UCSB
rodwell@ece.ucsb.edu

Co-Authors and Collaborators:
Teledyne HBT Team:
M. Urteaga, R. Pierson, P. Rowell, B. Brar, Teledyne Scientific Company

Teledyne IC Design Team:
M. Seo, J. Hacker, Z. Griffith, A. Young, M. J. Choe, Teledyne Scientific Company

UCSB HBT Team:
Recent Graduates: V. Jain, E. Lobisser, A. Baraskar,

UCSB IC Design Team:
S. Danesgar, T. Reed, H-C Park, Eli Bloch
DC to Daylight. Far-Infrared Electronics

**How high in frequency can we push electronics?**

1982: ~20 GHz   
2012: 820 GHz   
~2030: 3THz

- **microwave** SHF*  
  3-30 GHz  
  10-1 cm

- **mm-wave** EHF*  
  30-300 GHz  
  10-1 mm

- **sub-mm-wave** THF*  
  0.3-3THz  
  1-0.1 mm

- **mid-IR**  
  6-100 THz  
  50-3 μm

- **near-IR**  
  100-385 THz  
  3.078 μm

- **optical**  
  385-790 THz

**...and what we would be do with it?**

- **100+ Gb/s wireless networks**

- **Video-resolution radar**  
  → fly & drive through fog & rain

- **near-Terabit optical fiber links**

*ITU band designations  
** IR bands as per ISO 20473
100-1000 GHz Wireless Has High Capacity

very large bandwidths available

short wavelengths $\rightarrow$ many parallel channels

\[
\text{angular resolution} \approx \frac{\text{wavelength}}{\text{array width}}
\]

\[
N = \frac{B^2}{\lambda R} + 1
\]

\[
B = ND
\]

\[
\text{#channels} \propto \left( \frac{\text{aperture area}}{\text{wavelength} \cdot \text{distance}} \right)^2
\]
100-1000 GHz Wireless Needs Phased Arrays

isotropic antenna \rightarrow weak signal \rightarrow short range

\begin{equation}
\frac{P_{\text{received}}}{P_{\text{transmitted}}} \propto \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\end{equation}

highly directional antenna \rightarrow strong signal, but must be aimed

\begin{equation}
\frac{P_{\text{received}}}{P_{\text{transmitted}}} \propto D_t D_r \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\end{equation}

no good for mobile

must be precisely aimed \rightarrow too expensive for telecom operators

beam steering arrays \rightarrow strong signal, steerable

\begin{equation}
\frac{P_{\text{received}}}{P_{\text{transmit}}} \propto N_{\text{receive}} N_{\text{transmit}} \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\end{equation}

32-element array \rightarrow 30 (45?) dB increased SNR
100-1000 GHz Wireless Needs Mesh Networks

Object having area $\sim \lambda R$ will block beam.

...high-frequency signals are easily blocked.

Blockage is avoided using beamsteering and mesh networks.

...this is easier at high frequencies.
100-1000 GHz Wireless Has Low Attenuation?

Low attenuation on a sunny day

Wiltse, 1997
IEEE Int. APS Symposium, July
100-1000 GHz Wireless Has **High Attenuation**

**High Rain Attenuation**

Rain Attenuation, dB/km

- 30 dB/km
- 50 mm/Hr
- 100 mm/Hr

Rain Attenuation, dB/km vs Frequency, Hz

- Five-9's rain @ 50-1000 GHz: → 30 dB/km
- \( \lambda^{-4} \) @ 50 GHz

**High Fog Attenuation**

\( \alpha(f) \)

- Very heavy fog

\( \sim (25 \text{ dB/km}) \times \text{frequency/500 GHz} \)

50-500 GHz links must tolerate \( \sim 30 \text{ dB/km attenuation} \)

---


140 GHz, 10 Gb/s Adaptive Picocell Backhaul

array: 2x32

4 units

90° (h) by 10° (v) scan

individual antennas 1.4x12 mm

25mm

44mm
140 GHz, 10 Gb/s Adaptive Picocell Backhaul

350 meters range in five-9's rain

Realistic packaging loss, operating & design margins

PAs: 24 dBm $P_{sat}$ (per element) $\rightarrow$ GaN or InP

LNAs: 4 dB noise figure $\rightarrow$ InP HEMT
340 GHz, 160 Gb/s MIMO Backhaul Link

Eight 20 Gb/s MIMO units: each an 8x8 array

individual antennas: 6x6 mm

→ 1° beamwidth; 8° beamsteering
340 GHz, 160 Gb/s MIMO Backhaul Link

Eight 20 Gb/s MIMO units: each an 8x8 array

1° beamwidth; 8° beamsteering

600 meters range in five-9's rain

Realistic packaging loss, operating & design margins

PAs: 21 dBm $P_{\text{sat}}$ (per element) $\rightarrow$ InP

LNAs: 7 dB noise figure $\rightarrow$ InP HEMT
400 GHz frequency-scanned imaging radar

What your eyes see-- in fog

What you see with X-band radar

What you would like to see
400 GHz frequency-scanned imaging car radar

Eight 1x8 modules

1x64 endfire array

30 cm x 30 cm diffraction grating

Cylindrical lens: 30 cm aperture

Frequency-scanned beam

Individual antennas: 0.4 mm x 5.0 mm
400 GHz frequency-scanned imaging car radar

Range: see a basketball at 300 meters (10 seconds warning) in heavy fog
(10 dB SNR, 28 dB/km, 1 foot diameter target, 65 MPH)

Image refresh rate: 60 Hz

Resolution 64×512=32,800 pixels

Angular resolution: 0.10 degrees

Angular field of view: 9 by 97 degrees

Aperture: 12" by 12"

Component requirements:
10 mW peak power/element,
3% pulse duty factor
6.5 dB noise figure,
5 dB package losses
5 dB manufacturing/aging margin
100-1000 GHz Wireless Transceiver Architecture

III-V LNAs, III-V PAs → power, efficiency, noise
Si CMOS beamformer → integration scale

...similar to today's cell phones.
RADAR / Imaging Needs Watts of Power, Low Noise Figure

220 GHz video-rate synthetic aperture radar

As a function of range, weather, and data rate, effective sub-mm-wave technologies must low noise figure, high transmit power, and/or moderate to large phased arrays

Azimuthal resolution $\delta_a = \frac{\lambda R_{\text{image}}}{v_{\text{aircraft}}}$

SNR = $\frac{P_{\text{trans}}}{kT f_{\text{image}}} \frac{1}{4\pi R^2} \frac{LH}{\lambda^2} \cdot \delta_a \cdot \delta_r \cdot \sin \psi \cdot \rho \cdot \frac{LH}{4\pi R^2} e^{-\alpha R}$

10 Hz video rate. 1 km range
570 x 500 pixel image 100 mm x 44 mm total aperture, 16 dB SNR
5.5 cm resolution. 32 receive elements.
@ 10% reflectivity. 250 m/s aircraft velocity
7 dB/km attenuation

50 W transmitted power. 6 dB noise figure.

...to reach such levels with a solid-state source:

Present 220 GHz, 66 mW PA
Develop 200 mW PA
8-element array tile IC: 1.6 W
32 tiles/array $\rightarrow$ 51 W

As a function of range, weather, and data rate, effective sub-mm-wave technologies must low noise figure, high transmit power, and/or moderate to large phased arrays
On-wafer antennas
substantial die area, have high losses

For useful directivity, aperture areas are ~ 25 cm².
→ vastly too large for an IC
0.1-1 THz Comms Links: Discrete LNAs & PAs

Monolithic PAs & LNAs
long lines to antennas
many dB losses on transmit
many dB losses on transmit
degraded noise, degraded power

Discrete LNAs and PAs
LNAs & PAs: adjacent to antennas
losses no longer impair link

Given that we should not integrate the LNA and PA on the beamformer, it is to our benefit to use high-performance GaN & InP LNAs and PAs.
0.1-1 THz Comms Links: Array Design Concepts

Concepts: Robert York, UCSB
Effects of array size, Transmitter PAE, Receiver $F_{\text{min}}$

Low transmitter PAE & high receiver noise are partially offset using arrays,

but DC power, system complexity still suffer

Large arrays: more directivity, more complex ICs
Small arrays: less directivity, less complex ICs

→ Proper array size minimizes DC power
III-V PAs and LNAs in today's wireless systems...

http://www.chipworks.com/blog/recentteardowns/2012/10/02/apple-iphone-5-the-rf/
Devices for 100-1000 GHz systems: $F_{\text{min}}$, $P_{\text{sat}}$, PAE

LNA noise figure, Power amplifier power & efficiency: All critically important in radio and radar

**InP HBTs**: strong THz MSI technology
- efficient, high-power PAs,
- up/down converters (VCOs, synthesizers, mixers)

**InP HEMTs**: best THz LNA technology
- 3 dB more noise $\rightarrow$ 2:1 more transmit power

**GaN HEMTs vs. InP HBTs** for power:
- breakdown vs. gain $\rightarrow$ power vs. PAE.

**CMOS VLSI**:
- high bandwidth, high integration scales $\rightarrow$ bulk of signal processing
- poor $P_{\text{sat}}$, PAE, $F_{\text{min}}$.

**Harmonic techniques**:
- multiplication: low power, inefficient, nonlinear (16QAM ?, OFDM ?)
- harmonic mixing: high noise figure
Transistors for 100-1000 GHz systems
Transistor scaling laws: $\left( V, I, R, C, \tau \right)$ vs. geometry

**Depletion Layers**

\[ C = \varepsilon \cdot \frac{A}{T} \]

\[ \tau = \frac{T}{2v} \]

\[ I_{\text{max}} = \frac{4\varepsilon v_{\text{sat}}(V_{\text{appl}} + \phi)}{A} \]

**Bulk and Contact Resistances**

\[ R \approx \rho_{\text{contact}} / A \]

**Fringing Capacitances**

\[ C_{\text{fing}} / L \sim \varepsilon \]

1) FET fringing capacitances
2) IC interconnect capacitances

**Thermal Resistance**

\[ \Delta T_{\text{IC}} \propto \frac{P_{\text{IC}}}{K_{th} L} \]

\[ \Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L \ln \left( \frac{L}{W} \right)} \]

**Available quantum states to carry current**

$\rightarrow$ capacitance, transconductance contact resistance
Changes required to double transistor bandwidth

<table>
<thead>
<tr>
<th>FET parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/µm), ( g_m ) (mS/µm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport effective mass</td>
<td>constant</td>
</tr>
<tr>
<td>channel 2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel density of states</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>source &amp; drain contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

fringing capacitance does not scale → linewidths scale as \( \frac{1}{\text{bandwidth}} \)

<table>
<thead>
<tr>
<th>HBT parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter &amp; collector junction widths</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density (mA/µm²)</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>current density (mA/µm)</td>
<td>constant</td>
</tr>
<tr>
<td>collector depletion thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.4:1</td>
</tr>
<tr>
<td>emitter &amp; base contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

nearly constant junction temperature → linewidths vary as \( \frac{1}{\text{bandwidth}^2} \)
THz Bipolar Transistors

Gain (dB) vs Frequency (Hz)

- $f_{\tau} = 480$ GHz
- $f_{\text{max}} = 1.0$ THz

$V_{T,\text{useful}} \approx 2 \text{ THz} \cdot V$

$\tau \cdot (\text{useful } \Delta V) \approx 1.0 \text{ THz} \cdot V$

#### Performance Parameters

- **Emitter**
  - $f_{\tau} = 370$
  - $f_{\text{max}} = 490$
- **Base**
  - $f_{\tau} = 520$
  - $f_{\text{max}} = 850$
- **Collector**
  - $f_{\tau} = 730$
  - $f_{\text{max}} = 1300$
- **Power Amplifiers**
  - $f_{\tau} = 1000$
  - $f_{\text{max}} = 2000$
- **2:1 Divider**
  - $f_{\tau} = 480$
  - $f_{\text{max}} = 660$

#### Additional Information

- **Width**
  - 32 nm
  - 1 $\Omega \cdot \mu m^2$ contact $\rho$
- **Contact Width**
  - 30 nm
  - 1.25 $\Omega \cdot \mu m^2$ contact $\rho$
- **Thickness**
  - 37.5 nm
  - 72 mA/$\mu$A current density
- **Breakdown**
  - 2-2.5 V, breakdown

#### Electrical Parameters

- $f_{\tau} \cdot V_{br} \approx 2 \text{ THz} \cdot V$
-

- $I_{b,\text{step}} = 200 \mu A$
- $A_{je} = 0.22 \times 2.7 \mu m^2$
- $J_e = 20.4$ mA/$\mu m^2$
- $V_{cb} = 0.7$ V
InP HBT: Key Features

512 nm node:
  high-yield "pilot-line" process, ~4000 HBTs/IC

256 nm node:
  Power Amplifiers: >0.5 W/mm @ 220 GHz
  highly competitive mm-wave / THz power technology

128 nm node:
  >500 GHz $f_t$, >1.1 THz $f_{\text{max}}$, ~3.5 V breakdown
  breakdown* $f_t = 1.75 \text{ THz*Volts}$
  highly competitive mm-wave / THz power technology

64 nm (2 THz) & 32 nm (2.8 THz) nodes:
  Development needs major effort, but no serious scaling barriers

1.5 THz monolithic ICs are feasible.
InP Bipolar Transistor Scaling Roadmap

3-4 THz Bipolar Transistors are Feasible.

4 THz HBTs realized by:
Extremely low resistivity contacts
Extreme current densities
Processes scaled to 16 nm junctions

Impact:
efficient power amplifiers and complex signal processing from 100-1000 GHz.

<table>
<thead>
<tr>
<th>Scaling Node</th>
<th>64</th>
<th>32</th>
<th>16</th>
<th>nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Width</td>
<td>64</td>
<td>32</td>
<td>16</td>
<td>nm</td>
</tr>
<tr>
<td>Resistivity</td>
<td>2</td>
<td>1</td>
<td>0.5</td>
<td>Ω-μm²</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>18</td>
<td>15</td>
<td>13</td>
<td>nm</td>
</tr>
<tr>
<td>Contact width</td>
<td>60</td>
<td>30</td>
<td>15</td>
<td>nm</td>
</tr>
<tr>
<td>Contact ρ</td>
<td>2.5</td>
<td>1.25</td>
<td>0.63</td>
<td>Ω-μm²</td>
</tr>
<tr>
<td>Collector Width</td>
<td>180</td>
<td>90</td>
<td>45</td>
<td>nm</td>
</tr>
<tr>
<td>Thickness</td>
<td>53</td>
<td>37.5</td>
<td>26</td>
<td>nm</td>
</tr>
<tr>
<td>Current Density</td>
<td>36</td>
<td>72</td>
<td>140</td>
<td>mA/μm²</td>
</tr>
<tr>
<td>( f_t )</td>
<td>1.0</td>
<td>1.4</td>
<td>2.0</td>
<td>THz</td>
</tr>
<tr>
<td>( f_{max} )</td>
<td>2.0</td>
<td>2.8</td>
<td>4.0</td>
<td>THz</td>
</tr>
</tbody>
</table>
2-3 THz InP HEMTs are Feasible.

2 THz FETs realized by:
- Ultra low resistivity source/drain
- High operating current densities
- Very thin barriers & dielectrics
- Gates scaled to 9 nm junctions

Impact:
- Sensitive, low-noise receivers from 100-1000 GHz.

3 dB less noise → need 3 dB less transmit power.
Can we make a 1 THz SiGe Bipolar Transistor?

Simple physics clearly drives scaling
- transit times, $C_{cb}/I_c$
  - thinner layers, higher current density
- high power density → narrow junctions
- small junctions → low resistance contacts

Key challenge: Breakdown
- 15 nm collector → very low breakdown

Also required:
- low resistivity Ohmic contacts to Si
- very high current densities: heat

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions

<table>
<thead>
<tr>
<th></th>
<th>InP</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter</td>
<td>64</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.6</td>
</tr>
<tr>
<td>nm width</td>
<td></td>
<td></td>
</tr>
<tr>
<td>base</td>
<td>64</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td>0.7</td>
</tr>
<tr>
<td>nm contact width</td>
<td></td>
<td></td>
</tr>
<tr>
<td>collector</td>
<td>53</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>36</td>
<td>125</td>
</tr>
<tr>
<td>nm thick</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.75</td>
<td>1.3?</td>
</tr>
<tr>
<td>mA/μm²</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_\tau$</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>2000</td>
<td>2000</td>
</tr>
<tr>
<td>GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PAs</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>digital</td>
<td>480</td>
<td>480</td>
</tr>
<tr>
<td>GHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(2:1 static divider metric)
III-V vs. CMOS: A false comparison?

III-V MOS has a reasonable chance of future use in VLSI

The real THz / VLSI distinction:
Device geometry optimized for high-frequency gain vs. optimized for small footprint and high DC on/off ratio.
0.1-1THz IC Design
Challenges: 100-1000 GHz IC design

Given: we must use scaled, high-bandwidth transistors

Reduced breakdown is significant, but is not the main problem:

- breakdown does not vary as (bandwidth)^{-1}
- low breakdown is not the only problem

Interconnects and their parasitics

- interconnect length should vary as (frequency)^{-1}
- scaled device footprint: \( (g_m / \text{area}) \propto (\text{current} / \text{area}) \propto (\text{frequency})^2 \)
- scaled interconnect pitch: \( \propto (\text{frequency})^{-1} \)

Interconnects, footprints not scaled

\rightarrow \text{large interconnect LC parasitics}

Interconnects, footprints scaled

\rightarrow \text{large interconnect resistance & skin loss}
\rightarrow \text{small interconnect burnout current}
\rightarrow \text{high IC power density}
III-V MIMIC Interconnects  -- Classic Substrate Microstrip

Thick Substrate  → low skin loss

Zero ground inductance in package

No ground plane breaks in IC

High via inductance

TM substrate mode coupling

12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

Strong coupling when substrate approaches ~λ_d/4 thickness

lines must be widely spaced

ground vias must be widely spaced

Line spacings must be ~3*(substrate thickness)

all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

$\alpha_{skin} \propto \frac{1}{\varepsilon_r^{1/2} H}$

Brass carrier and assembly ground interconnect substrate
IC with backside ground plane & vias
near-zero ground-ground inductance
IC vias eliminate on-wafer ground loops
Coplanar Waveguide

No ground vias
No need (???) to thin substrate

Parasitic slot mode

Hard to ground IC
to package

Parasitic microstrip mode

ground plane breaks → loss of ground integrity

-\( V \) 0V +\( V \)

0V

Parasitic slot mode

substrate mode coupling
or substrate losses

-\( V \) 0V +\( V \)

\( k_z \)

Repairing ground plane with ground straps is effective only in simple ICs. In more complex CPW ICs, ground plane rapidly vanishes → common-lead inductance → strong circuit-circuit coupling

poor ground integrity

loss of impedance control

ground bounce

coupling, EMI, oscillation

III-V: semi-insulating substrate → substrate mode coupling
Silicon conducting substrate → substrate conductivity losses

40 Gb/s differential TWA modulator driver note CPW lines, fragmented ground plane
35 GHz master-slave latch in CPW note fragmented ground plane
175 GHz tuned amplifier in CPW note fragmented ground plane
If It Has Breaks, It Is Not A Ground Plane!

coupling / EMI due to poor ground system integrity is common in high-frequency systems whether on PC boards ...or on ICs.
III-V MIMIC Interconnects -- Thin-Film Microstrip

- narrow line spacing → IC density
- no substrate radiation, no substrate losses
- fewer breaks in ground plane than CPW
- ... but ground breaks at device placements
- still have problem with package grounding
- ...need to flip-chip bond

thin dielectrics → narrow lines → high line losses → low current capability → no high-$Z_0$ lines

$Z_0 \sim \frac{\eta_0}{\varepsilon_r^{1/2}} \left( \frac{H}{W + H} \right)$
III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

- **narrow line spacing → IC density**
  - Smiley face

- **Some substrate radiation / substrate losses**
  - Sad face

- **No breaks in ground plane**
  - Smiley face

- **... no ground breaks at device placements**
  - Smiley face

- **still have problem with package grounding**
  - Sad face

- ...need to flip-chip bond

- **thin dielectrics → narrow lines**
  - High line losses

- **low current capability**

- **no high-$Z_0$ lines**

---

InP 150 GHz master-slave latch

InP 8 GHz clock rate delta-sigma ADC
VLSI mm-wave interconnects with ground integrity

- Narrow line spacing → IC density
- No substrate radiation, no substrate losses
- Negligible breaks in ground plane
- Negligible ground breaks @ device placements
- Still have problem with package grounding
  ...need to flip-chip bond

- Thin dielectrics → narrow lines
  → High line losses
  → Low current capability
  → No high-\(Z_0\) lines

Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling.
(critical signal line is placed above ground, other lines and supplies are placed below ground)
1: (over)stabilize at the design frequency guided by stability circles

2: Tune input for $F_{\text{min}}$ (LNAs) or output for $P_{\text{sat}}$ (PAs)

3: Tune remaining port for maximum gain

4: Add out-of-band stabilization.

There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers. Choice guided by tuning losses. No particular preferences.

For BJT's, MAG/MSG usually highest for common-base. → preferred topology.

Common-base gain is however reduced by:
- base (layout) inductance
- emitter-collector layout capacitance.
longer interconnects: lines terminated in Zo → no reflections.

Shorter interconnects: lines NOT terminated in Zo. But they are *still* transmission-lines. Ignore their effect at your peril!

If length << wavelength, or line delay << risetime, short interconnects behave as lumped L and C.

\[
L = Z_0 \tau, \quad C = \tau / Z_0, \quad \tau = l / v
\]
Design Flow: Digital & Mixed-Signal IC's

All interconnects: thin-film microstrip environment. 
Continuous ground on one plane.

2.5-D simulations run on representative lines. 
various widths, various planes 
same reference (ground) plane.

Simulation data manually fit to CAD line model 
effective substrate $\varepsilon_r$, effective line-ground spacing.

Width, length, substrate of each line 
entered on CAD schematic. 
rapid data entry, rapid simulation.

Resistors and capacitors: 
2.5-D simulation $\rightarrow$ RLC fit 
RLC model ---or simulation S-parameters --used in simulation.
High Speed ECL Design

Followers associated with inputs, not outputs
Emitters never drive long wires.
(instability with capacitive load)

Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.

Current mirror biasing is more compact.
Mirror capacitance → ringing, instability.
Resistors provide follower damping.
High Speed ECL Design

**Layout:** short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

**Key:** transistors in on-state operate at Kirk limited-current. → minimizes $C_{cb}/I_c$ delay.

**Key:** transistors designed for minimum ECL gate delay*, not peak ($f_r$, $f_{max}$).

*hand expression, charge-control analysis

**Example:** 8:1 205 GHz static divider in 256 nm InP HBT.

205 GHz divider, Griffith et al., IEEE CSIC, Oct. 2010
ICs in Thin-Film (Not Inverted) Microstrip

Note breaks in ground plane at transistors, resistors, capacitors
ICs in Thin-Film (Not Inverted) Microstrip

Note breaks in ground plane at transistors, resistors, capacitors
ICs in Thin-Film Inverted Microstrip

100 GHz differential TASTIS Amp.  512nm InP HBT
Digital, mixed-signal, RF-IC (tuned) IC designs----at very high frequencies

Even at 670 GHz, design procedures differ little from that at lower frequencies:

Classic IC design extends readily to the far-infrared.

Key considerations: Tuned ("RF") ICs
Rigorous E&M modeling of all interconnects & passive elements
Continuous ground plane → required for predicable interconnect models.
Higher frequencies→ close conductor planes→ higher loss, lower current

Key considerations: digital & mixed-signal :
Transmission-line modeling of all interconnects
Continuous ground plane → required for predicable interconnect models.
Unterminated lines within blocks; terminated lines interconnecting blocks.
Analog & digital blocks design to naturally interface to 50 or 75Ω.
Design Examples, IC Results
InP HBT Integrated Circuits: 600 GHz & Beyond

614 GHz fundamental VCO
M. Seo, TSC / UCSB

565 GHz, 34 dB, 0.4 mW output power amplifier
J. Hacker, TSC

340 GHz dynamic frequency divider
M. Seo, UCSB/TSC IMS 2010

204 GHz static frequency divider (ECL master-slave latch)
Z. Griffith, TSC CSIC 2010

300 GHz fundamental PLL
M. Seo, TSC IMS 2011

600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC

Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC

220 GHz 90 mW power amplifier
T. Reed, UCSB
Digital Logic: 30 GHz to 204 GHz in 12 Years

1998: 30 GHz → 48 GHz

2000: 66 GHz

2001: 75 GHz

2002: 87 GHz

2004: 118 GHz

2004: 142 GHz, 150 GHz

2010: 204 GHz (with Teledyne)
Other InP HBT ICs in Inverted Microstrip

- **InP 8 GHz clock rate delta-sigma ADC** (Krishnan, IMS 2003)
- **30 GHz digital SSB mixer / PFD for optical PLL** (Bloch, IMS 2012)
- **10 Gb/s x 6-channel (+/- 12.5, +/- 37.5, +/- 62.5 GHz)** WDM receiver IC for coherent optical links (H. Park, being tested)
- **40 Gb/s coherent optically-phase-locked BSPK optical receiver** (Bloch, Park, ECOC 2012)
- **40 Gb/s coherent optically-phase-locked QPSK optical receiver** (E. Bloch, being tested)
- **50 GS/s Track/hold and sample/hold amplifiers** Daneshgar, IEEE CSICS Oct. 2012
Teledyne: 600 GHz Common-Base Amplifier IC

- 12-Stage Common-base using inverted CPW-G architecture
- 2.8 dBm saturated output power
- >20 dB gain up to 620 GHz

M. Seo et al, Teledyne Scientific: IMS2013
90 mW, 220 GHz Power Amplifier

Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT

Amplifier gains (dBi)
frequency (GHz)
3dB bandwidth = 240GHz
S\textsubscript{21,mid-band} = 15.4dB
P\textsubscript{DC} = 4.46W

P\textsubscript{out}, mW
P\textsubscript{in}, mW
8-cell, 2-stage PA
220GHz operation

active area, 1.02 x 0.85 mm
die: 2.42 x 1.22 mm
90 mW, 220 GHz Power Amplifier

RF output power densities up to 0.5 W/mm @ 220 GHz.

→ InP HBT is a competitive mm-wave / sub-mm-wave power technology.
220 GHz 330mW Power Amplifier Design

Operating Frequency = 220 GHz
Pdc = 12 W

Gain (dB), Pout (dBm)
Pin (dBm)

S-parameters (dB)
Frequency (GHz)

2.3 mm x 2.5 mm

T. Reed, UCSB
Z. Griffith, Teledyne
Teledyne 250 nm InP HBT
**84 GHz Power Amplifier Design #1: 250 nm InP HBT**

**Simulations:**

**HBT:** 16 fingers x 6um x 0.25um = 96 um x 0.25 um

**Gain:** 9.2dB

**PAE:** 35%

**$P_{out}$:** 22.3 dBm (170 mW) $\rightarrow$ 1.75 W/mm

**Chip size:** 450 $\mu$m x 780 $\mu$m
84 GHz Power Amplifier Design #2: 250 nm InP HBT

Simulations:

HBT: 96 fingers x 6μm x 0.25μm = 576 μm x 0.25 μm

Gain: 16.5dB

PAE: 24%

$P_{\text{out}}$: 28.8 dBm (760 mW) → 1.3 W/mm

Chip size: 1100 μm x 980 μm
220 GHz Vector Modulator / Phase Shifter Design
220 GHz Vector Modulator / Phase Shifter Design
220 GHz Vector Modulator / Phase Shifter Design

Technology: 256nm InP HBT
9/2012 tapeout; ICs expected 12/2012

intended operating range
THz Electronics for Terabit fiber optics

Bandwidth of optical fiber: ~5 THz.
Bandwidth of modern ICs: ~800GHz.

→ With THz transistors, and new IC topologies, electrical ICs can access over 1 THz of the optical fiber spectrum
Closing
Where Next? → 2 THz Transistors, 1 THz Radios.

transmitter

receiver

interconnects

circuits
**THz and Far-Infrared Electronics**

*IR today → lasers & bolometers → generate & detect*

**Far-infrared ICs: classic device physics, classic circuit design**

Power, power-added efficiency, noise figure are all very important.

*fundamental-mode operation, not harmonic generation*

The transistors will scale to at least 2 THz bandwidths.

**Even 1-3 THz ICs will be feasible**