Transistors for THz Systems

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UCSB IC Design Team:
S. Danesgar, T. Reed, H-C Park, Eli Bloch
**DC to Daylight. Far-Infrared Electronics**

**How high in frequency can we push electronics?**

<table>
<thead>
<tr>
<th>Year</th>
<th>Frequency (GHz)</th>
<th>Bandwidth (THz)</th>
<th>Transmission</th>
</tr>
</thead>
<tbody>
<tr>
<td>1982</td>
<td>~20</td>
<td>~20</td>
<td>Microwave</td>
</tr>
<tr>
<td>2012</td>
<td>820</td>
<td>820</td>
<td>mm-wave</td>
</tr>
<tr>
<td>~2030</td>
<td>300</td>
<td>300</td>
<td>sub-mm-wave</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>mid-IR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>near-IR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Optical</td>
</tr>
</tbody>
</table>

...and what we would be do with it?

- **100+ Gb/s wireless networks**
- **Video-resolution radar**
  - fly & drive through fog & rain
- **near-Terabit optical fiber links**

**Graphical Elements:**
- Frequency spectrum with bands labeled:
  - Microwave: 3-30 GHz, 10-1 cm
  - MM-wave: 30-300 GHz, 10-1 mm
  - Sub-mm-wave: 0.3-3 THz, 1-0.1 mm
  - Mid-IR: 6-100 THz, 50-3 µm
  - Near-IR: 100-385 THz, 3.0-0.78 µm
  - Optical: 385-790 THz

*ITU band designations
**IR bands as per ISO 20473
THz Transistors: Not Just For THz Circuits

- Precision analog design at microwave frequencies → high-performance receivers
- Higher-resolution microwave ADCs, DACs, DDSs
- THz amplifiers → THz radios → imaging, communications

Graph showing the relationship between frequency and transistor power gain.
THz Communications Needs High Power, Low Noise

140 GHz, 10 Gb/s spatially scanned network node

340 GHz, 160 Gb/s spatially multiplexed (MIMO) backhaul

Real systems with real-world weather & design margins, 500-1000m range:

Will require:

3-7 dB Noise figure, 50mW-1W output/element, 64-256 element arrays
→ InP or GaN PAs and LNAs, Silicon beamformer ICs
THz Communications Needs High Power, Low Noise

140 GHz, 10 Gb/s spatially scanned network node

array: 2x32 total
four modules
each 1x16

individual antennas
1.4x12 mm

25 mm

THz TRX module

multi-mode modulation

Si VLSI beamformer

InP or GaN PAs

antenna array

THz RCVR module

antenna array

InP LNAs

multitone demod.

equalization

340 GHz, 160 Gb/s spatially multiplexed (MIMO) backhaul

eight 20 Gb/s MIMO units

50 mm

1x8 array

TRX module

Si VLSI beamformer

GaN or InP PAs

antenna array

RCVR module

Si VLSI beamformer

ΔΔΔΔ InP LNAs

MIMO channel separation

clock/data recovery

Real systems → LNAs with low Fmin, PAs with high Psat & high PAE

Comparing technologies

InP HEMTs give the best noise. InP HBT & GaN HEMT compete for the PA. CMOS is great for signal processing, but noise, power, PAE are poor. Harmonic generation is low power, inefficient. Harmonic mixing is noisy.
III-V PAs and LNAs in today's wireless systems...

http://www.chipworks.com/blog/recentteardowns/2012/10/02/apple-iphone-5-the-rf/
THz Device Scaling
nm Transistors, Far-Infrared Integrated Circuits

IR today → lasers & bolometers → generate & detect

Far-infrared ICs: classic device physics, classic circuit design

It's all about the interfaces: contact and gate dielectrics...
...wire resistance,...
...heat,...

...& charge density.

band structure and density of states!
### Transistor scaling laws: \( V, I, R, C, t \) vs. geometry

#### Depletion Layers

\[
C = \varepsilon \cdot \frac{A}{T}
\]

\[
\tau = \frac{T}{2v}
\]

\[
I_{\text{max}} = \frac{4\varepsilon v_{\text{sat}} (V_{\text{appl}} + \phi)}{A} T^2
\]

#### Bulk and Contact Resistances

\[
R \approx \rho_{\text{contact}} / A \quad \text{contact terms dominate}
\]

### Fringing Capacitances

\[
C_{\text{fing}} / L \sim \varepsilon
\]

1) FET fringing capacitances
2) IC interconnect capacitances

### Thermal Resistance

\[
\Delta T_{IC} \propto \frac{P_{IC}}{K_{th}L} \quad \Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th}L} \ln \left( \frac{L}{W} \right)
\]

### Available quantum states to carry current

→ capacitance, transconductance contact resistance
# THz & nm Transistors: State Density Limits

<table>
<thead>
<tr>
<th></th>
<th>2-D: FET</th>
<th>3-D: BJT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>capacitance</strong></td>
<td>$C_{DOS} = \frac{q^2 m^*}{2\pi \hbar^2}$</td>
<td></td>
</tr>
<tr>
<td><strong>current</strong></td>
<td>$J_{\text{sheet}} = \frac{2^{3/2} q^{5/2} (m^*)^{1/2} V^{3/2}}{3\pi^2 \hbar^2}$</td>
<td>$J = \frac{q^3 m^* V^2}{4\pi^2 \hbar^3}$</td>
</tr>
<tr>
<td><strong>conductivity</strong></td>
<td>$\sigma_c = \left(\frac{q^2}{\hbar}\right) \cdot \left(\frac{2}{\pi^3}\right)^{1/2} \cdot n^{1/2}$</td>
<td>$\sigma_c = \left(\frac{q^2}{\hbar}\right) \cdot \left(\frac{3}{8\pi}\right)^{2/3} \cdot n^{2/3}$</td>
</tr>
</tbody>
</table>

# of available quantum states / energy determines FET channel capacitance
FET and bipolar transistor current access resistance of Ohmic contact
Bipolar Transistor Design

\[ \tau_b \approx T_b^2 / 2D_n \]

\[ \tau_c = T_c / 2v_{sat} \]

\[ C_{cb} = eA_c / T_c \]

\[ I_{c,\text{max}} \propto v_{sat} A_e (V_{ce,\text{operating}} + V_{ce,\text{punch-through}}) / T_c^2 \]

\[ \Delta T \propto \frac{P}{L_E} \left[ 1 + \ln \left( \frac{L_e}{W_e} \right) \right] \]

\[ R_{ex} = \rho_{contact} / A_e \]

\[ R_{bb} = \rho_{\text{sheet}} \left( \frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e} \right) + \frac{\rho_{contact}}{A_{\text{contacts}}} \]
Bipolar Transistor Design: Scaling

\[ \tau_b \approx \frac{T_b^2}{2D_n} \]

\[ \tau_c = \frac{T_c}{2\nu_{sat}} \]

\[ C_{cb} = \varepsilon A_c / T_c \]

\[ I_{c,\text{max}} \propto \nu_{sat} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2 \]

\[ \Delta T \propto \frac{P}{L_E} \left[ 1 + \ln \left( \frac{L_e}{W_e} \right) \right] \]

\[ R_{ex} = \rho_{\text{contact}} / A_e \]

\[ R_{bb} = \rho_{\text{sheet}} \left( \frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e} \right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}} \]
Breakdown: Never Less than the Bandgap

$E_{\text{gap,base}}$  
$E_{\text{gap,collector}}$

emitter  
base  
collector

band-band tunneling: base bandgap  
impact ionization: collector bandgap
FET Design

\[ C_{gd} \approx C_{gs,f} \approx \varepsilon W_g \]

\[ g_m = C_{g-ch} \cdot \left( \frac{v}{L_g} \right) \]

\[ C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{well}/2\varepsilon_{well} + (q^2/\text{well statedensity})} \]

\[ v \propto \left( \text{voltage division ratio between the above three capacitors} \right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}} \]

\[ R_{DS} \approx L_g / (W_g \sqrt{\varepsilon}) \quad R_S = R_D = \frac{\rho_{\text{contact}}}{L_{S/D} W_g} \]
FET Design: Scaling

\[ C_{gd} \approx C_{gs,f} \approx \varepsilon W_g \]

\[ g_m = C_{g-ch} \cdot \left( \frac{v}{L_g} \right) \]

\[ C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{well}/2\varepsilon_{well} + (q^2/\text{well state density})} \]

\[ v \propto \left( \text{voltage division ratio between the above three capacitors} \right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}} \]

\[ R_{DS} \approx \frac{L_g}{(W_g v \varepsilon)} \quad R_S = R_D = \frac{\rho_{\text{contact}}}{L_{S/D} W_g} \]
FET Design: Scaling

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\[ R_{DS} \approx \frac{L_g}{(W_g v \varepsilon)} \]

\[ R_S = R_D = \frac{\rho_{\text{contact}}}{L_{S/D} W_g} \]
Changes required to double transistor bandwidth

**FET parameter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/µm), $g_m$ (mS/µm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport effective mass</td>
<td>constant</td>
</tr>
<tr>
<td>channel 2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel density of states</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>source &amp; drain contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

(fringing capacitance does not scale $\rightarrow$ linewidths scale as $(1 / \text{bandwidth})$)

**HBT parameter**

<table>
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<tr>
<th>Parameter</th>
<th>Change</th>
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<tbody>
<tr>
<td>emitter &amp; collector junction widths</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density (mA/µm²)</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>current density (mA/µm)</td>
<td>constant</td>
</tr>
<tr>
<td>collector depletion thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.4:1</td>
</tr>
<tr>
<td>emitter &amp; base contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

(nearly constant junction temperature $\rightarrow$ linewidths vary as $(1 / \text{bandwidth})^2$)
THz & nm Transistors: what needs to be done

**Metal-semiconductor interfaces (Ohmic contacts): very low resistivity**

**Dielectric-semiconductor interfaces (Gate dielectrics---FETs only): thin!**

**Ultra-low-resistivity (~0.25 $\Omega \cdot \mu m^2$), ultra shallow (1 nm), ultra-robust (0.2 A/\mu m^2) contacts**

**Heat**

$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th}L}$$

$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th}L} \ln\left(\frac{L}{W}\right)$$

**Available quantum states to carry current**

→ capacitance, transconductance, contact resistance
THz InP HBTs
Scaling Laws, Scaling Roadmap

Scaling laws: to double bandwidth

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<tr>
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<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>emitter</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>32 nm width</td>
<td>1 Ω·µm² access ρ</td>
</tr>
<tr>
<td>base</td>
<td>120</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>30 nm contact width,</td>
<td>1.25 Ω·µm² contact ρ</td>
</tr>
<tr>
<td>collector</td>
<td>75</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>37.5 nm thick,</td>
<td>72 mA/µm² current density</td>
</tr>
<tr>
<td></td>
<td>3.3</td>
<td>2.75</td>
</tr>
<tr>
<td></td>
<td>2-2.5 V, breakdown</td>
<td></td>
</tr>
<tr>
<td>$f_t$</td>
<td>730</td>
<td>1000</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>1300</td>
<td>2000</td>
</tr>
<tr>
<td>RF-ICs</td>
<td>660</td>
<td>1000</td>
</tr>
<tr>
<td>digital divider</td>
<td>330</td>
<td>480</td>
</tr>
<tr>
<td></td>
<td>1400 GHz</td>
<td>2800 GHz</td>
</tr>
<tr>
<td></td>
<td>1400 GHz</td>
<td>660 GHz</td>
</tr>
</tbody>
</table>
HBT Fabrication Process Must Change... Greatly

32 nm width base & emitter contacts...self-aligned
32 nm width emitter semiconductor junctions

Contacts:
1 $\Omega \mu m^2$ resistivities
70 mA/$\mu m^2$ current density
~1 nm penetration depths
$\rightarrow$ refractory contacts

nm III-V FET, Si FET processes have similar requirements
Needed: Greatly Improved Ohmic Contacts

Pt/Ti/Pd/Au

\(~5 \text{ nm} \) Pt contact penetration (into 25 nm base)
Ultra Low-Resistivity Refractory Contacts

In-situ: avoids surface contaminants

Refractory: robust under high-current operation

Low penetration depth, ~ 1 nm

Contact performance sufficient for 32 nm /2.8 THz node.
Ultra Low-Resistivity Refractory Contacts

Schottky Barrier is about one lattice constant

what is setting contact resistivity?
what resistivity should we expect?
Ultra Low-Resistivity Refractory Contacts

Zero-barrier contact resistivity:
(state density and quantum-reflectivity limit)

\[ \rho_c = \left( \frac{\hbar}{q^2} \right) \cdot \left( \frac{8\pi}{3} \right)^{2/3} \cdot \frac{1}{T^2} \cdot \frac{1}{n^{2/3}} \]

- \( n = \) carrier concentration
- \( T = \) transmission coefficient

\[ \rho_c \approx 0.1 \Omega - \mu m^2 \] at \( n = 7 \cdot 10^{19} \text{ cm}^{-3} \).
Refactory Emitter Contacts

negligible penetration
HBT Fabrication Process Must Change... Greatly

tall, narrow contacts: liftoff fails!

control undercut → thinner emitter
→ thinner emitter
→ thinner base metal

thinner base metal → excess base metal resistance

Undercutting of emitter ends

\{101\}A planes: fast

\{111\}A planes: slow
Sub-200-nm Emitter Contact & Post

Refractory contact, refractory post $\rightarrow$ high-J operation

Sputter+dry etch $\rightarrow$ 50-200nm contacts

Liftoff aided by TiW/W interface undercut

Dielectric sidewalls
RF Data: 25 nm thick base, 75 nm Thick Collector

Required dimensions obtained but poor base contacts on this run

E. Lobisser, ISCS 2012, August, Santa Barbara
DC, RF Data: 100 nm Thick Collector

\[ f_{\text{max}} = 1.0 \text{ THz} \]
\[ f = 480 \text{ GHz} \]

\[ A_{je} = 0.22 \times 2.7 \mu m^2 \]
\[ I_c = 12.1 \text{ mA} \]
\[ J_e = 20.4 \text{ mA/\mu m}^2 \]
\[ P = 33.5 \text{ mW/\mu m}^2 \]
\[ V_{cb} = 0.7 \text{ V} \]

Solid line: \( V_{cb} = 0.7\text{V} \)
Dashed: \( V_{cb} = 0\text{V} \)
\[ n_c = 1.19 \]
\[ n_b = 1.87 \]

Solid line: \( V_{cb} = 0.7\text{V} \)
Dashed: \( V_{cb} = 0\text{V} \)
\[ n_c = 1.19 \]
\[ n_b = 1.87 \]
THz InP HBTs From Teledyne

Fig. 3 RF gains of 0.13x2μm² HBT

130nm InP DHBTs with $f_t > 0.52$THz and $f_{max} > 1.1$THz

M. Urteaga¹, R. Pierson¹, P. Rowell¹, V. Jain¹, E. Lobisser¹, M.J.W. Rodwell²

¹Teledyne Scientific Company, Thousand Oaks, CA 93160. ²Department of ECE, University of California, Santa Barbara, CA 93106. E-mail: muretega@teledyne-si.com

Fig. 2 Common-emitter IV characteristics of 130nm HBT normalized to emitter area

Fig. 4 $f_t$ and $f_{max}$ versus collector current at varying values of $V_{CE}$ for 0.13x2μm² HBT

Urteaga et al, DRC 2011, June
Base contact process:
Present contacts too resistive (4Ω·μm²)
Present contacts sink too deep (5 nm) for target 15 nm base
→ refractory base contacts

Emitter Degeneracy:
Target current density is almost 0.1 Amp/μm² (!)
Injected electron density becomes degenerate.
transconductance is reduced.
→ Increased electron mass in emitter
Base Ohmic Contact Penetration

~5 nm Pt contact penetration (into 25 nm base)
Refractory Base Process (1)

Blanket liftoff; refractory base metal

Patterned liftoff; Thick Ti/Au

Blanket liftoff; refractory base metal

Patterned liftoff; Thick Ti/Au

base surface not exposed to photoresist chemistry: no contamination

low contact resistivity, shallow contacts

low penetration depth allows thin base, pulsed-doped base contacts
Increased surface doping:
reduced contact resistivity,
but increased Auger recombination.

→ Surface doping spike at most 2-5 thick.

Refractory contacts do not penetrate;
compatible with pulse doping.
Degenerate Injection $\rightarrow$ Reduced Transconductance

Current varies exponentially with $V_{be}$

$$J = J_s \exp\left(\frac{qV_{be}}{kT}\right).$$

Transconductance is high

$$g_m / A_E \propto J$$
Degenerate Injection → Reduced Transconductance

Current varies exponentially with $V_{be}$

$$J = J_s \exp \left( \frac{qV_{be}}{kT} \right).$$

Transconductance is reduced

Fermi-Dirac Boltzmann

$(\phi-V_{be}) >> kT/q$
Degenerate Injection $\rightarrow$ Reduced Transconductance

Highly degenerate limit:

Current varies as the square of bias

$$J \propto m^*_E (V_{be} - \phi)^2$$

Fermi-Dirac

Boltzmann

$$(\phi - V_{be}) \gg kT/q$$

Highly degenerate

$$(V_{be} - \phi) \gg kT/q$$

$$J \approx \frac{q^3 m^*}{8\pi^2 \hbar^3} (V_{be} - \phi)^2$$
Degenerate Injection $\rightarrow$ Reduced Transconductance

**Highly degenerate limit:**

*current varies as the square of bias*

$$J \propto m^* (V_{be} - \phi)^2$$

**Transconductance varies as $J^{1/2}$**

$$g_m / A_E \propto \sqrt{m^* J}$$

...and as $(m^*)^{1/2}$

At & beyond 32 nm, we must increase the emitter effective mass.
Degenerate Injection → Solutions

At & beyond 32 nm, we must **increase** the emitter (transverse) effective mass.

Other emitter semiconductors:

*no obvious good choices (band offsets, etc.).*

Emitter-base superlattice:

*increases transverse mass in junction*  
evidence that InAlAs/InGaAs grades are beneficial

**Extreme solution (10 years from now):**

*partition the emitter into small sub-junctions, ~ 5 nm x 5 nm.*  
*parasitic resistivity is reduced progressively as sub-junction areas are reduced.*

![Diagram of emitter and base superlattice](image-url)
3-4 THz Bipolar Transistors are Feasible.

4 THz HBTs realized by:
- Extremely low resistivity contacts
- Extreme current densities
- Processes scaled to 16 nm junctions

Impact:
- Efficient power amplifiers and complex signal processing from 100-1000 GHz.
InP HBT: Key Features

512 nm node:
high-yield "pilot-line" process, ~4000 HBTs/IC

256 nm node:
Power Amplifiers: >0.5 W/mm @ 220 GHz
highly competitive mm-wave / THz power technology

128 nm node:
>500 GHz $f_\tau$, >1.1 THz $f_{\text{max}}$, ~3.5 V breakdown
breakdown* $f_\tau = 1.75 \text{ THz*Volts}$
highly competitive mm-wave / THz power technology

64 nm (2 THz) & 32 nm (2.8 THz) nodes:
Development needs major effort, but no serious scaling barriers

1.5 THz monolithic ICs are feasible.
Can we make a 1 THz SiGe Bipolar Transistor?

Simple physics clearly drives scaling
transit times, $C_{cb}/I_c$
→ thinner layers, higher current density
high power density → narrow junctions
small junctions→ low resistance contacts

Key challenge: Breakdown
15 nm collector → very low breakdown

Also required:
low resistivity Ohmic contacts to Si
very high current densities: heat

<table>
<thead>
<tr>
<th></th>
<th>InP</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>emitter</strong></td>
<td>64</td>
<td>18</td>
</tr>
</tbody>
</table>
| width            | 2   | 0.6  | nm width
| **base**         | 64  | 18   |
| contact width,   | 2.5 | 0.7  | $\Omega \cdot \mu m^2$ contact $\rho$
| **collector**    | 53  | 15   |
| thickness        | 36  | 125  | mA/$\mu m^2$
|                 | 2.75| 1.3? | V, breakdown

- $f_\tau$ 1000 1000 GHz
- $f_{\text{max}}$ 2000 2000 GHz
- PAs 1000 1000 GHz
digital 480 480 GHz
(2:1 static divider metric)

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions.
**THz InP Bipolar Transistor Technology**

**Goal:**
extend the operation of electronics to the highest feasible frequencies

**THz InP Heterojunction Bipolar Transistors**
1 THz device

**Scaling roadmap through 3 THz**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>1982: ~13 GHz</th>
<th>2012: 820 GHz</th>
<th>~2027: 3THz</th>
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<tbody>
<tr>
<td>10^8</td>
<td>microwave</td>
<td>mm-wave</td>
<td>0.3-6 THz</td>
</tr>
<tr>
<td>10^9</td>
<td>far-IR</td>
<td>mid-IR</td>
<td>6-100 THz</td>
</tr>
<tr>
<td>10^10</td>
<td>3-30 GHz</td>
<td>near-IR</td>
<td>100-150 THz</td>
</tr>
<tr>
<td>10^11</td>
<td>optical</td>
<td>sub-THz</td>
<td>&gt;150 THz</td>
</tr>
</tbody>
</table>

**60-600 GHz IC examples; demonstrated & in fab**

- 220 GHz power amplifiers
- ultra-efficient 85 GHz power amplifiers
- 100 GHz ICs for *electronic* demultiplexing of WDM optical communications

**Enabling Technologies:**
~30 nm fabrication processes, extremely low resistivity (epitaxial, refractory) contacts, extreme current densities, doping at solubility limits, few-nm-thick junctions

**Teledyne Scientific: moving THz IC Technology towards aerospace applications**

1.1 THz pilot IC process
204 GHz digital logic (M/S latch)
670 GHz amplifier

**614 GHz fundamental oscillator (VCO)**

**182 mW**

**50 GHz sample/hold**

**40 GHz op-amp**

**40 Gb/s phase-locked coherent optical receivers**

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THz InP HEMTs and III-V MOSFETs
Changes required to double transistor bandwidth

<table>
<thead>
<tr>
<th>FET parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/μm), $g_m$ (mS/μm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport effective mass</td>
<td>constant</td>
</tr>
<tr>
<td>channel 2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel density of states</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>source &amp; drain contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

fringing capacitance does not scale → linewidths scale as $(1 / \text{bandwidth})$

<table>
<thead>
<tr>
<th>HBT parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter &amp; collector junction widths</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density (mA/μm$^2$)</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>current density (mA/μm)</td>
<td>constant</td>
</tr>
<tr>
<td>collector depletion thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.4:1</td>
</tr>
<tr>
<td>emitter &amp; base contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

constant voltage, constant velocity scaling

nearly constant junction temperature → linewidths vary as $(1 / \text{bandwidth})^2$
FET scaling challenges...and solutions

Gate barrier under S/D contacts $\rightarrow$ high S/D access resistance addressed by S/D regrowth

High gate leakage from thin barrier, high channel charge density (almost) eliminated by ALD high-K gate dielectric

Other scaling considerations:
- low InAs electron mass $\rightarrow$ low state density capacitance $\rightarrow g_m$ fails to scale
- increased $m^*$, hence reduced velocity in thin channels
- minimum feasible thickness of gate dielectric (tunneling) and channel
III-V MOS

Peak transconductance; VLSI-style FET: 2.5 mS/micron ~85% of best THz InAs HEMTs

**III-V MOS will soon surpass HEMTs in RF performance**

![Graph showing current density, gate bias, and peak transconductance](image)

*Gate length (µm) vs. Peak Transconductance (mS/µm)*

*Current Density (mA/µm) vs. Gate Bias (V)*

*40 nm devices are nearly ballistic*

Regrown S/D gate channel

Al₂O₃/HfO₂

Sanghoon Lee
FET Drain Current in the Ballistic Limit

\[ J = K_1 \cdot \left( \frac{84 \text{ mA}}{\mu \text{m}} \right) \cdot \left( \frac{V_{gs} - V_{th}}{1 \text{ V}} \right)^{3/2}, \quad \text{where} \quad K_1 = \frac{g \cdot (m^*/m_o)^{1/2}}{\left( 1 + (c_{dos,o} / c_{equiv}) \cdot g \cdot (m^*/m_o) \right)^{3/2}} \]

In ballistic limit, current and transconductance are set by:

channel & dielectric thickness, transport mass, state density
Low $m^*$ gives lowest transit time, lowest $C_{gs}$ at any EOT.

\[ \tau_{ch} \equiv \frac{Q_{ch}}{I_D} = K_2 \cdot \left( \frac{L_g}{2.52 \cdot 10^7 \text{ cm/s}} \right) \cdot \left( \frac{1 \text{ Volt}}{V_{gs} - V_{th}} \right)^{1/2} \quad \text{where} \quad K_2 = \left( \frac{m^*}{m_0} \right)^{1/2} \cdot \left( 1 + \frac{c_{dos,o}}{c_{eq}} \cdot g \cdot \frac{m^*}{m_0} \right)^{1/2} \]

$\tau_{ch}$ and $K_2$ are plotted against $m^*/m_0$ for various EOT values and material types (Si, GaN, InGaAs). The graph shows normalized transit delay $K_2$ versus $m^*/m_0$ for different EOT values (0.4 nm, 0.6 nm, 1.0 nm). It includes wavefunction depth term (mean wavefunction depth $\varepsilon_{SiO_2} / \varepsilon_{semiconductor}$).

EOT=1.0 nm
0.6 nm

1 nm
0.4 nm
0.6 nm
0.4 nm

$C_{equiv} = \left( \frac{1}{c_{ox}} + \frac{1}{c_{semi}} \right)^{-1} = \varepsilon_{SiO_2} / \text{EOT}$

---

Transit delay versus mass, # valleys, and EOT

$\varepsilon_{SiO_2}$ is the dielectric constant of silicon dioxide, and $\varepsilon_{semiconductor}$ is the dielectric constant of the semiconductor.
FET Scaling: fixed vs. increasing state density

- Canonical scaling
- Stepped # of bands
- \( \Gamma \) transport only

- \( f_\tau \)
- \( f_{\text{max}} \)

- Drain current density, m\(A/\mu m\) → VLSI metric
- SCFL static divider speed

- 200 mV gate overdrive

Need higher state density for ~10 nm node
2-3 THz Field-Effect Transistors are Feasible.

3 THz FETs realized by:
- Ultra low resistivity source/drain
- High operating current densities
- Very thin barriers & dielectrics
- Gates scaled to 9 nm junctions

Impact:
- Sensitive, low-noise receivers from 100-1000 GHz.

3 dB less noise → need 3 dB less transmit power.
4-nm / 5-THz FETs: Challenges

Gate dielectric
- 0.1 nm EOT: UTB
- 0.2 nm EOT: fin

Channel thickness
- 0.8 nm: UTB
- 1.6 nm: fin atomically flat

Gate tunneling current is just acceptable at 0.2 nm EOT.

How can we make a 1.6 nm thick fin, or a 0.8 nm thick body?
Thin wells have high scattering rate

Scattering probability $\propto 1/m_q^2 T_{well}^6$.

Sakaki

Need single-atomic-layer control of thickness
Need high *quantization* mass $m_q$. 
III-V vs. CMOS: A false comparison?

III-V MOS has a reasonable chance of future use in VLSI

The real THz / VLSI distinction:
Device geometry optimized for high-frequency gain
vs. optimized for small footprint and high DC on/off ratio.
Conclusion
THz and Far-Infrared Electronics

IR today → lasers & bolometers → generate & detect

Far-infrared ICs: **classic** device physics, **classic** circuit design

It's all about **classic** scaling:

- contact and gate dielectrics...
- wire resistance,...
- heat,...
- & charge density.

*band structure and density of quantum states (new!).*

Even 1-3 THz ICs will be feasible
Electron Plasma Resonance: Not a Dominant Limit

\[ L_{\text{kinetic}} = \frac{T}{A q^2 \nu m^*} \]

\[ R_{\text{bulk}} = \frac{T}{A q^2 \nu m^* \tau_m} \]

\[ C_{\text{displacement}} = \frac{\varepsilon A}{T} \]

dielectric relaxation frequency
\[ f_{\text{dielectric}} = \frac{1}{2\pi} \frac{1}{C_{\text{displacement}} R_{\text{bulk}}} = \frac{1}{2\pi} \frac{\sigma}{\varepsilon} \]

scattering frequency
\[ f_{\text{scatter}} = \frac{1}{2\pi} \frac{R_{\text{bulk}}}{L_{\text{kinetic}}} = \frac{1}{2\pi \tau_m} \]

plasma frequency
\[ f_{\text{plasma}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{kinetic}} C_{\text{displacement}}}} \]

<table>
<thead>
<tr>
<th></th>
<th>dielectric relaxation frequency</th>
<th>scattering frequency</th>
<th>plasma frequency</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>[ f_{\text{dielectric}} = \frac{1}{2\pi} \frac{1}{C_{\text{displacement}} R_{\text{bulk}}} = \frac{1}{2\pi} \frac{\sigma}{\varepsilon} ]</td>
<td>[ f_{\text{scatter}} = \frac{1}{2\pi} \frac{R_{\text{bulk}}}{L_{\text{kinetic}}} = \frac{1}{2\pi \tau_m} ]</td>
<td>[ f_{\text{plasma}} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{\text{kinetic}} C_{\text{displacement}}}} ]</td>
</tr>
<tr>
<td>n - InGaAs</td>
<td>800 THz</td>
<td>7 THz</td>
<td>74 THz</td>
</tr>
<tr>
<td>3.5 \cdot 10^{19} / cm^3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>p - InGaAs</td>
<td>80 THz</td>
<td>12 THz</td>
<td>31 THz</td>
</tr>
<tr>
<td>7 \cdot 10^{19} / cm^3</td>
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</table>