Performance Impact of Post-Regrowth Channel Etching on InGaAs MOSFETs Having MOCVD Source-Drain Regrowth

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Overview

Why III-V for VLSI?
Device Physics and Scaling
Process Flows
Measurements
Conclusions
Why III-V VLSI?

Higher electron velocities than Si MOS

For short $L_g$ FETs, $\frac{J_{\text{drain}}}{q} = \frac{n_{s,\text{channel}} \cdot v_{\text{sat}}}{C_{\text{g}}}$

Transconductance, $g_m = C_{\text{effective}} \cdot v_{\text{sat}}$

$J_d$ and $g_m$ are key figures of merit in VLSI

However:

$J_d$ and $g_m$ degraded by source large $R_{\text{access}}$

$J_d$ and $g_m$ degraded by interface trap density, $D_{it}$

Therefore, we must develop:

Low access resistance source/drain contacts

Thin, high-k, low $D_{it}$ dielectrics on InGaAs

Fully self-aligned process modules

MOSFETs have been, and always will be, a materials challenge.
**FET Device Physics**

\[ C_{ox} = \frac{\varepsilon_0 \varepsilon_r L_g W_g}{t_{ox}} \]

\[ C_{depth} \approx \frac{\varepsilon_0 \varepsilon_{channel} L_g W_g}{t_{channel}/2} \]

\[ C_{dos} = \frac{q^2 g_m}{2\pi \hbar^2} L_g W_g \]

\[ n_{channel} = \frac{C_{dos}}{q} (V_{dos}) \]

**D_{it} problem**

\[ \uparrow C_{it}, \downarrow V_{surface} \]

\[ V_{surface} \text{ supplies } C_{dos} \]

\[ \downarrow V_{surface} = \downarrow n_{dos} \text{ in } C_{dos} \]

**Electron band diagram: gate-insulator-channel**
Candidate III-V Planar Geometries

“Trench” MOSFET
Leverages HEMT tech.
Gate oxide $\rightarrow$ Low $I_g$
Small footprint
But
Will the $L_g$ scale?

Replacement Gate MOSFET
Easily defined $L_g$
Gate oxide
Small footprint
But
Is RG doping high enough?
## Gate Replacement FET Process Flow

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>MBE growth, deposit SiO₂</td>
</tr>
<tr>
<td>2.</td>
<td>InGaAs well, InAlAs barrier, S.I. substrate</td>
</tr>
<tr>
<td>3.</td>
<td>Pattern dummy gate.</td>
</tr>
<tr>
<td>4.</td>
<td>Regrow source/drain.</td>
</tr>
<tr>
<td>5.</td>
<td>Strip SiO₂, deposit gate dielectric.</td>
</tr>
<tr>
<td>6.</td>
<td>Lift off gate metal.</td>
</tr>
</tbody>
</table>

### MBE S/D Regrowth

- **Low-damage process**
- Thermal gate metal
- No/Low-damage plasma
- Dielectric post-regrowth

**STEM FET cross section, color-coded by chemistry**

*Figure courtesy Jeremy Law (UCSB)*

**Nickel Gate Metal**

100 nm $L_g$

10 nm Thick Well

InAlAs Back Barrier
Gate Replacement FET Challenges

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>InGaAs well</td>
<td>N⁺ S/D</td>
<td>InGaAs well</td>
<td>N⁺ S/D</td>
<td>InGaAs well</td>
</tr>
<tr>
<td>InAlAs barrier</td>
<td>InAlAs barrier</td>
<td>SiO₂</td>
<td>InAlAs barrier</td>
<td>SiO₂</td>
<td>InAlAs barrier</td>
</tr>
<tr>
<td>S.I. substrate</td>
<td>S.I. substrate</td>
<td></td>
<td>S.I. substrate</td>
<td></td>
<td>S.I. substrate</td>
</tr>
</tbody>
</table>

SEM of dummy gate

MBE regrowth is non-selective → requires photoresist planarization

DRC 2013
Gate Replacement FET Challenges

Short dummy gates are hard to planarize, aspect-ratio-limited gate length
Solution: MOCVD S/D Regrowth *

MBE InAs RG  MOCVD InGaAs RG

MBE is non-selective to the SiO₂ pillar, while MOCVD is selective!
→ PR planarization no longer necessary → short $L_g$ that will not fall over

* Terao et al, APEX 2011, and Egard et al, DRC 2011
81 nm \( L_g \), (1 nm Al\(_2\)O\(_3\)/ 4 nm HfO\(_2\)), 10 nm channel, MBE InGaAs Regrowth

\[ V_{GS} = -0.2 \text{ V to } 0.6 \text{ V} \]
\[ 0.2 \text{ V increment} \]

\[ V_{DS} = 0.1 \text{ V, 0.5 V, 0.7 V} \]
\[ SS=194 \text{ mV} \]
\[ at V_{DS}=0.1\text{V} \]

68 \( L_g \), (1 nm Al\(_2\)O\(_3\)/ 4 nm HfO\(_2\)), 10 nm channel, MOCVD InGaAs Regrowth

\[ V_{GS} = -0.6 \text{ V to } 0.6 \text{ V} \]
\[ 0.2 \text{ V increment} \]

\[ V_{DS} = 0.05 \text{ V to } 0.5 \text{ V} \]

**Similar on-state performance, but large Vth shift, poor SS, DIBL**

DRC 2013
Poor subthreshold: Channel Degradation

> 300 mV/dec subthreshold swing $\rightarrow D_{it}$? Channel degradation?

Experiment: SiO$_2$ capping + high temp anneal + strip $\rightarrow$ MOSCAP 5 nm Al$_2$O$_3$

InP channel capping for RG $\rightarrow$ large subthreshold swing for FETs 😞
Digital semiconductor etching*

Before ALD deposition:
Oxidize channel surface (UV O₃)
Etch oxide in HCl:DI

Repeat as needed
Etches ~ 1.2 nm per cycle

Top-down thin channels \(\rightarrow\) Increase \(C_{\text{depth}}\)
Simultaneous damage removal and body scaling

* S.Lee et al, IPRM 2013
MOCVD RG with Digital Channel Etching

68 nm actual $L_g$, (1 nm Al$_2$O$_3$ / 4 nm HfO$_2$), No digital etching (~ 10 nm channel)

65 nm actual $L_g$, (1 nm Al$_2$O$_3$ / 4 nm HfO$_2$), 2 cycles of digital etching (~ 6.5 nm channel)

result

All devices improve with channel etch $\rightarrow$ thinner channel, remove surface damage
MOCVD RG with Digital Channel Etching

Peak transconductance (mS/micron): 50 nm as drawn gate length, 0.5 V \( V_{gs} \)

<table>
<thead>
<tr>
<th>No Etching (10 nm ch.)</th>
<th>2 Cycle Etching (~6.5 nm ch.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.10</td>
</tr>
<tr>
<td>2</td>
<td>0.89</td>
</tr>
<tr>
<td>3</td>
<td>0.93</td>
</tr>
<tr>
<td>4</td>
<td>1.01</td>
</tr>
<tr>
<td>5</td>
<td>Open</td>
</tr>
<tr>
<td>6</td>
<td>0.99</td>
</tr>
</tbody>
</table>

Peak transconductance (mS/micron):

- 50 nm as drawn gate length, 0.5 V \( V_{gs} \)

**Result**

All devices improve with channel etch → thinner channel, remove surface damage
All devices improve with channel etch → thinner channel, remove surface damage
Lower performance for not etched channels not due to metal-RG contact
MOCVD RG: Recent Results

48 nm gate length, ~ 3.8 nm HfO$_2$, InGaAs with 2 cycle digital etching, p-doped back barrier

40 nm gate length, ~ 3.6 nm HfO$_2$, InAs/InGaAs channel, digitally etched *

High performance III-V MOS using aggressively scaled ALD dielectrics
Conclusions

65 nm gate last InGaAs MOSFET process flow using MOCVD

\[ J_{\text{drain}} = 0.78 \text{ mA/\mu m} \text{ at } 0.5 \text{ V} \ V_{gs} - V_{th}, 0.5 \text{ V} \ V_{ds} \]

Peak transconductance: 1.58 mS/micron at 0.5 V \( V_{ds} \)

Self-aligned process path for sub-50 nm III-V VLSI

Continued research areas
  Thinner gate dielectrics
  Body scaling (thin planar QW and/or FinFETs)
  Improved \( D_{it} \) passivation techniques
Thanks for your time!
Questions?

contact address: adc [at] ece.ucsb.edu

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BACK UP SLIDES
### Source-Drain Regrowth Data

<table>
<thead>
<tr>
<th>Name</th>
<th>Dopant (cm$^{-3}$)</th>
<th>Thickness (nm)</th>
<th>Contact Metal</th>
<th>$R_{\text{sheet}}$ (Ω/□)</th>
<th>$R_{\text{Access}}$ (Ω·μm)</th>
<th>$\rho_{\text{contact}}$ (Ω·μm$^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MBE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-InGaAs</td>
<td>Si, $\sim 5 \times 10^{19}$</td>
<td>$\sim 50$</td>
<td>Mo, In-Situ</td>
<td>29</td>
<td>12</td>
<td>5.5</td>
<td>[18]</td>
</tr>
<tr>
<td>n-InAs</td>
<td>Si, $\sim 4 \times 10^{19}$</td>
<td>$\sim 50$</td>
<td>Mo, In-Situ</td>
<td>23</td>
<td>8.5</td>
<td>3.5</td>
<td>[20]</td>
</tr>
<tr>
<td>n-InAs (1)</td>
<td>Si, $\sim 5 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>21.4</td>
<td>6.5</td>
<td>2</td>
<td>[24]</td>
</tr>
<tr>
<td>n-InAs (2)</td>
<td>Si, $\sim 5 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>25.3</td>
<td>9.9</td>
<td>3.9</td>
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<tr>
<td>n-InAs (3)</td>
<td>Si+Te, $\sim 6 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>17</td>
<td>4.7</td>
<td>1.29</td>
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<tr>
<td>n-InAs</td>
<td>Si+Te, $\sim 6 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>18.9</td>
<td>6.56</td>
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<tr>
<td>n-InAs</td>
<td>Si+Te, $\sim 6 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>17.8</td>
<td>10.6</td>
<td>6.32</td>
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<tr>
<td>n-InGaAs</td>
<td>Si+Te, $\sim 5 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ni/Pd/Au $^\dagger$, Ex-Situ</td>
<td>17.8</td>
<td>3.25</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td><strong>MOCVD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-InGaAs (1)</td>
<td>Si, $\sim 4.5 \times 10^{19}$</td>
<td>$\sim 30$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>41.8</td>
<td>32.44</td>
<td>25.2</td>
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<tr>
<td>n-InGaAs (2)</td>
<td>Si, $\sim 4.5 \times 10^{19}$</td>
<td>$\sim 30$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>39.4</td>
<td>16.97</td>
<td>7.29</td>
<td></td>
</tr>
<tr>
<td>n-InGaAs (3)</td>
<td>Si, $\sim 4.5 \times 10^{19}$</td>
<td>$\sim 30$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>46</td>
<td>19.8</td>
<td>8.5</td>
<td></td>
</tr>
<tr>
<td>n-InGaAs</td>
<td>Si, $\sim 4.5 \times 10^{19}$</td>
<td>$\sim 60$</td>
<td>Ti/Pd/Au, Ex-Situ</td>
<td>23.5</td>
<td>13.02</td>
<td>7.2</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1: Summary of MBE and MOCVD regrowth data. Dopant concentration is active carrier concentration. Electron beam evaporation for metal contacts, unless otherwise noted. $^\dagger$: thermal metal evaporation.
MOCVD RG: Recent Results

48 nm gate length, ~3.8 nm HfO₂, InGaAs with 2 cycle digital etching, p-doped back barrier

40 nm gate length, ~3.6 nm HfO₂, InAs/InGaAs channel, digitally etched *

High performance III-V MOS using aggressively scaled ALD dielectrics

* S. Lee et al, VLSI 2013
FET Device Physics

\[ C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \]

\[ C_{\text{depth}} \approx \frac{\varepsilon_o \varepsilon_{\text{channel}}}{t_{\text{channel}}/2} \]

\[ C_{\text{dos,2D}} = \frac{q^2 g_m^*}{\pi \hbar^2} \]

\[ n_{\text{channel}} = \frac{C_{\text{dos}}}{q} (V_{\text{dos}}) \]

\[ J_{\text{drain}} = q \cdot n_{s,\text{channel}} \cdot v_{\text{sat}} \]

\[ g_m = C_{\text{effective}} \cdot v_{\text{sat}} \]

*Effective includes \( C_{ox}, C_{\text{depth}}, C_{\text{dos}} \)

Electron band diagram of a quantum well FET
FET Device Scaling

Contacted Gate Pitch

Si CMOS scaling: Contacted gate pitch 4x the gate length\(^1\)

4:1 reduction of contact area\(^2\) → 4:1 reduction of \(\rho_{\text{contact}}\)

22 nm node → 33 nm \(L_{S/D}\) → For \(L_{S/D} = L_T\), requires \(5 \times 10^{-9}\) ohm-cm\(^2\) \(\rho_{\text{contact}}\)

\[
\text{Contact Transfer Length} = L_T = \sqrt{\frac{\rho_c}{R_{sh}}}
\]

Gate First FET Process Flow

Thick (10 nm) channel

- Process damage mitigation

Heavy (~ $9 \times 10^{12} \text{ cm}^{-2}$) $\delta$ doping

- Prevents ungated sidewall current choke

$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ heterobarrier

- Carrier confinement

Semi-insulating InP

- Device isolation
Gate First FET Process Flow

**Gate Stack Deposition**

- **mask**
- **SiO₂**
- **Cr**
- **W**
- **high-k**
- **InGaAs Channel**
- **InAlAs Heterobarrier**
- **Insulating Substrate**

**Gate Stack Etching**

- **SiO₂**
- **Cr**
- **W**
- **high-k**
- **InGaAs Channel**
- **InAlAs Heterobarrier**
- **Insulating Substrate**

Front End: Gate Stack Definition

*In-situ* hydrogen plasma / TMA treatment before Al₂O₃ growth
Mixed e-beam / optical lithography
Bi-layer gate (Sputtered W + e-beam evaporated Cr)
High selectivity, low power dry etch
FET Process Development

Use optical lithography to produce >0.5um gates
Use electron beam lithography to produce sub-100nm gates
Need to investigate possible e-beam damage to oxides

EBL Tests

Finished Gate Etch + Sidewall Deposition
FET Process Development

ICP dry etches calibrated to perform at sub-100nm scale

Increased ICP Power

Higher power dry etch → vertical gate stack

Undercutting leads to fallen gates, ungated access regions → Minimize Cr undercut by reducing thickness
Gate First FET Process Flow

Front End: Gate Stack Definition

Sidewall Deposition
Conformal, protects S/D short circuit to gate

Sidewall etch
Vertical gate stack → self aligned sidewall
FET Process Development

Low power etch $\rightarrow$ Isotropic etching + undercut $\rightarrow$ fallen gates
Large undercuts $\rightarrow$ ungated regions $\rightarrow$ high $R_{\text{access}}$

**Thick gate stack:**
- Small $L_g$
- Large sidewall foot
- Unreliable gates

**Thin Cr stack:**
- Small $L_g$
- Large sidewall foot
- Repeatable gate etch?

**ALD SiO$_2$ sidewall:**
- Small $L_g$
- Still sidewall foot!
- Unrepeatable gate undercut
Gate First FET Process Flow

**High-k Etch and Regrowth Prep**

- **SiO₂**
- **Cr**
- **W**
- high-k

**InGaAs Channel**

**InAlAs Heterobarrier**

**Insulating Substrate**

**Source and Drain Regrowth**

- **SiO₂**
- **Cr**
- **W**
- high-k

**InGaAs Channel**

**InAlAs Heterobarrier**

**Insulating Substrate**

**Contact Metalization, Device Isolation, and Passivation**

**Regrowth and Back End**

**Surface preparation**

- UV O₃ exposure to clean the source/drain, removed *ex-situ* before MBE load

**MBE InAs Regrowth**

- Low arsenic flux, high temperature → near gate fill in

**Metallization and Mesa Isolation**

- *In-situ*Mo in MBE optional for lower ρₑ
- Ti/Pd/Au liftoff
- Wet etch for mesa isolation
Gate First FET Process Flow

TEM micrographs of 60 nm $L_g$ device
Gate First FET Results

60 nm $L_g$

- $V_{gs}$: -2V to 3V in 1V steps
- $W_g$: 9 μm

- Increased leakage current:
  - Heavy $\delta$ doping leakage path
  - Drain induced barrier lowering

115 nm $L_g$

- $V_{gs}$: -2V to 3V in 1V steps
- $W_g$: 9 μm
Gate First FET Results

60 nm $L_g$

$V_{gs} : -2V$ to $3V$ in $1V$ steps
$W_g : 9 \mu m$

High $J_{\text{drain}}$ but depletion mode

Transconductance: Similar to previous results* ($\approx 0.3\text{mS/}\mu\text{m}$)

Low $R_{\text{on}}$ (371 ohm-$\mu$m) for InGaAs MOSFETs

Gate First FET Results

- $J_{\text{drain}}$ increases rapidly with gate length scaling
- Transconductance: Relatively flat with gate length scaling

$W_g = 9 \ \mu\text{m}$

FET: Access Resistance

MOSFET On Resistance

Gateless Transistor Resistance

Gateless transistor effective diagnostic of regrowth

$R_{\text{access}}$: 200 ohm-µm

$R_{\text{access}}$: 100 ohm-µm

$R_{\text{measured}} = \frac{R_{sh} L_{\text{gap}}}{W} + 2R_{\text{access}}$

$W_g = 25 \mu m$

$T_{\text{chan}} = 15 \text{ nm}$

$W_g = 9 \mu m$

$T_{\text{chan}} = 10 \text{ nm}$

$y = 400.46 + 795.01x$  \( R^2 = 0.98313 \)

$y = 337.87 + 658.51x$  \( R^2 = 0.9877 \)

$y = 304.7 + 608.65x$  \( R^2 = 0.98906 \)
Gate First FET: Metal-Regrowth TLM

\[ R_{\text{measured}} = \frac{R_{\text{sh}} L_{\text{gap}}}{W} + 2R_c \]

\[ R_c \approx \frac{\rho_c}{L_TW} \quad \text{for } L > 1.5L_T \]

\[ L_T = \sqrt{\frac{\rho_c}{R_{\text{sh}}}} \]

Metal-Regrowth access resistance is not a limiting factor in \( J_{\text{drain}} \)

*Ex-situ* Ti/Pd/Au / n-type InAs contacts: \( \rho_c = 2 \times 10^{-8} \text{ ohm-cm}^2 \)

*In-situ* Mo / n-type InAs contacts have shown \( \rho_c = 6 \times 10^{-9} \text{ ohm-cm}^2 \)

Gate First FET: Issues

Ungated region $\rightarrow$ potential current choke

Thinner sidewall can help…

… but hard to control with gate undercut

Electron band diagram of channel underneath sidewall
Gate First FET: Issues

Heavy $\delta$ doping $\rightarrow$ parallel conduction, poor $g_m$
Large leakage current in device
Decreases $C_{\text{depth}}$ $\rightarrow$ limits $g_m$

\[ 9 \cdot 10^{12} \text{ cm}^{-2} \delta \text{ doping} \quad \text{no } \delta \text{ doping} \]

Must reduce $\delta$ doping while maintaining low $R_{\text{access}}$
FET Device Physics

\[ C_{ox} = \frac{\varepsilon_o \varepsilon_r L_g W_g}{t_{ox}} \]

\[ C_{depth} \approx \frac{\varepsilon_o \varepsilon_{\text{channel}} L_g W_g}{t_{\text{channel}}/2} \]

\[ C_{dos} = \frac{q^2 g_m^*}{\pi \hbar^2} L_g W_g \]

\[ n_{\text{channel}} = \frac{C_{dos}}{q} (V_{dos}) \]

- **Dit problem**
  - \( \uparrow C_{it} \), \( \downarrow V_{surface} \)
  - \( V_{surface} \) also supplies \( C_{dos} \)
  - \( \downarrow V_{surface} = \downarrow ndos \) in \( C_{dos} \)
FET Device Scaling

<table>
<thead>
<tr>
<th>FET parameters</th>
<th>Scaling Rule</th>
<th>How?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Density $\left(\frac{mA}{\mu m}\right)$, $g_m \left(\frac{mS}{\mu m}\right)$</td>
<td>increase 2:1</td>
<td>Lithographic Scaling</td>
</tr>
<tr>
<td>Gate Length and Contact Spacing $\left(L_g, L_{S/D}\right)$</td>
<td>decrease 2:1</td>
<td>Channel Material and Orientation</td>
</tr>
<tr>
<td>Channel Electron Density</td>
<td>increase 2:1</td>
<td>Channel Material and Orientation</td>
</tr>
<tr>
<td>Electron Transport Mass $\left(m^*_{\text{transverse}}\right)$</td>
<td>constant</td>
<td>Channel Material and Orientation</td>
</tr>
<tr>
<td>Gate Capacitance</td>
<td>increase 2:1</td>
<td>Channel Material and Orientation</td>
</tr>
<tr>
<td>Channel Density of States</td>
<td>increase 2:1</td>
<td>Channel Material and Orientation</td>
</tr>
<tr>
<td>Channel Thickness $\left(T_{\text{inv}}\right)$</td>
<td>decrease 2:1</td>
<td>Materials Engineering</td>
</tr>
<tr>
<td>Effective Oxide Thickness $\left(T_{\text{ox}}\right)$</td>
<td>decrease 2:1</td>
<td>Materials Engineering</td>
</tr>
<tr>
<td>Source/Drain Contact Resistivity</td>
<td>decrease 4:1</td>
<td>Materials Engineering</td>
</tr>
</tbody>
</table>
FET Device Scaling

- 5 nm channel, 500 cm²/(V*s) mobility, 5E19 cm⁻³ carriers = 500 ohm/sq
- 5E-9 ohm cm² contact resistance
- \( L_{\text{transfer}} \approx 31 \) nm

\[
\text{Contact Transfer Length} = L_T = \sqrt{\frac{\rho_c}{R_{sh}}}
\]

FET Process Development

1) Poorly controlled dry etch undercut
   - Low power etch → Isotropic etching

**Thick gate stack:**
Small $L_g$ ☺
Large sidewall foot ☹
Unreliable gates ☹

**Thin Cr stack:**
Small $L_g$ ☺
Large sidewall foot ☹
Reliable gate etch?

**ALD SiO$_2$ sidewall:**
Small $L_g$ ☺
Still sidewall foot! ☹
Unreliable gate undercut ☹