Low Power III-V InGaAs MOSFETs Featuring InP Recessed Source/Drain Spacers with $I_{on}=120 \, \mu A/\mu m$ at $I_{off}=1 \, nA/\mu m$ and $V_{DS}=0.5 \, V$

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Outline

- Problem: III-V MOSFETs are very leaky
- Gate-last Process Flow
- Knob 1: Wide band-gap barrier
- Knob 2: Source/Drain vertical spacer
- Knob 3: Ultrathin channel
- Knob 4: Recessed InP S/D spacer
- Knob 5: Doping-graded InP spacer
- Summary
InGaAs/InAs FETs are leaky!

- **III-V channel**: low electron effective mass, high velocity, high mobility $\rightarrow$ higher current at lower $V_{DD}$ 😊

- Low band gap $\rightarrow$ band-to-band tunneling (BTBT) 😞

- High permittivity $\rightarrow$ worse electrostatics, large DIBL 😞

- Goal: reduce leakage current for low power logic!

### Table: Comparison of Materials

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InAs</th>
<th>In$<em>{0.53}$Ga$</em>{0.47}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_e^*$ (m$_e$/eV)</td>
<td>0.19</td>
<td>0.08</td>
<td>0.063</td>
<td>0.023</td>
<td>0.041</td>
</tr>
<tr>
<td>$\mu_e$ (cm$^2$/V·s)</td>
<td>1450</td>
<td>3900</td>
<td>9200</td>
<td>33000</td>
<td>12000</td>
</tr>
<tr>
<td>$\mu_h$ (cm$^2$/V·s)</td>
<td>370</td>
<td>1800</td>
<td>400</td>
<td>450</td>
<td>&lt;300</td>
</tr>
<tr>
<td>$E_g$ (eV)</td>
<td>1.12</td>
<td>0.664</td>
<td>1.424</td>
<td>0.354</td>
<td>0.75</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.7</td>
<td>16.2</td>
<td>12.9</td>
<td>15.2</td>
<td>13.9</td>
</tr>
<tr>
<td>$a$ (Å)</td>
<td>5.43</td>
<td>5.66</td>
<td>5.65</td>
<td>6.06</td>
<td>(InP)</td>
</tr>
</tbody>
</table>

![Graph showing current density vs. gate bias for different device thicknesses at $V_{DS}=0.5$ V and $0.05$ V]
UCSB Gate Last Process Flow

- Channel
- Barrier
- Substrate

MBE grown device epilayer

Pattern dummy gate

HSQ

MOCVD source/drain regrowth

N+ S/D

HSQ

ZrO₂

Isolation
Strip dummy gate
Digital etch
Deposit ALD dielectric
FGA anneal

N+ S/D

Channel
Barrier
Substrate

Lift-off gate metal

N+ S/D

Channel
Barrier
Substrate

Deposit S/D contacts

Ti/Pd/Au
Knob 1: Wide Band-gap Barrier

- Wide band-gap barriers or P-doped back barriers reduces bottom leakage path.
- **Solution 1**: AlAsSb barriers (Sample B) reduces subthreshold leakage.
- **Solution 2**: P-doped InAlAs barriers also work well.

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C. Y. Huang et al., APL., 103, 203502 (2013)
Knob 2: Source/Drain Vertical Spacer

Vertical spacers reduce the peak electric field, improve electrostatics, and reduce BTBT floor.

S. Lee et al., APL 103, 233503 (2013)
C. Y. Huang et al., DRC 2014.
Knob 3: Ultra-thin channel

S. Lee et al., VLSI 2014

2.7 nm InAs channel (strained)

2.5 nm ZrO₂

1 nm Al₂O₃Nₓ

![Graph](image)

\( I_{on} = 500 \, \mu A/\mu m \) at \( I_{off} = 100 \, nA/\mu m \)

and \( V_D = 0.5 V \)

SS ~ 72 mV/dec.

SS ~ 77 mV/dec.

\( V_{DS} = 0.5 \, V \)

\( I_{on} = 500 \, \mu A/\mu m \) at \( I_{off} = 100 \, nA/\mu m \)

Intel, IEDM 2009

J. Gu, IEDM 2012

D. Kim, IEDM 2012
Increasing band gap: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel

<table>
<thead>
<tr>
<th>Sample</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel (nm)</td>
<td>4.5</td>
<td>3</td>
</tr>
<tr>
<td>InGaAs spacer (nm)</td>
<td>11.5</td>
<td>13</td>
</tr>
</tbody>
</table>

Reduction in channel thickness improves electrostatics, increases confinement bandgap and reduces BTBT.
E-field and BTBT contour

- Concentrated electric field at the drain end of the channel next to the gate edge.

- **Solution:** Replace InGaAs with wide band-gap InP ($E_g \sim 1.35$ eV)

R. Chu et al., EDL 29, 974 (2008)

J. Lin et al., EDL 35, 1203 (2014)
Knob 4: Recessed InP S/D spacer

12 nm InGaAs spacer

5 nm Recessed InP spacer

$V_{DS} = 0.1$ to 0.7 V, 0.2 V step

SS $\approx 80.1$ mV

SS $\approx 72.5$ mV

$L_g = 60$ nm
Minimum spacer thickness is required to maintain good electrostatics.

Thicker spacer is desired at drain to smooth electric field.
- Thicker InP spacer increases $R_{on}$, and degrades $G_m$.
- Thinner spacer is desired at source to reduce $R_{S/D}$. 

![Graph showing the effect of InP spacer thickness on $g_m$ and $R_{on}$]
Knob 5: Doping-graded InP spacer

- Doping-graded InP spacer reduces parasitic source/drain resistance and improves $G_m$.
- Gate leakage limits $I_{\text{off}} \sim 300 \text{ pA/\mu m}$. 

$\L_g$ - 30 nm, 30Å ZrO$_2$

$V_{\text{DS}} = 0.1$ to $0.7 \text{ V}$
0.2 V increment

$I_D$, $|I_G|$(mA/\(\mu\)m)

$V_{\text{GS}}$(V)

$R_{\text{on}}$ at zero $L_g$ (\(\Omega \cdot \mu\)m)

<table>
<thead>
<tr>
<th>Layer</th>
<th>$5 \text{ nm UID InP}$</th>
<th>$13 \text{ nm UID InP}$</th>
<th>Doping graded InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{on}}$ at zero $L_g$ ((\Omega \cdot \mu)m)</td>
<td>$\sim 199$</td>
<td>$\sim 364$</td>
<td>$\sim 270$</td>
</tr>
</tbody>
</table>

S.I. InP substrate

50 nm N+InGaAs
10 nm N+InP
8 nm doping graded InP
5 nm U.I.D InP

ZrO$_2$

4.5 nm InGaAs
5 nm InAlAs U.I.D. spacer
2 nm 1E19 cm$^{-3}$ N+InAlAs
100 nm InAlAs U.I.D. buffer
250 nm 1E17 cm$^{-3}$ P-InAlAs
50 nm InAlAs U.I.D buffer
Doping-graded InP spacer + Thicker oxide

<table>
<thead>
<tr>
<th>$V_{DS}$ = 0.1 to 0.7 V</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0.2 V increment</td>
<td>0.2 V increment</td>
</tr>
</tbody>
</table>

### InP graded spacer

- 38Å ZrO$_2$
- $I_D$ ~ 60 pA/µm at $V_{D}$=0.5V for $L_g$-30 nm

| $V_{GS}$ (V) | $I_D$ (mA/µm) | $|I_G|$ (mA/µm) |
|--------------|---------------|---------------|
| -0.6         | 10^-9         | 10^-9         |
| -0.3         | 10^-8         | 10^-8         |
| 0            | 10^-7         | 10^-7         |
| 0.3          | 10^-6         | 10^-6         |
| 0.6          | 10^-5         | 10^-5         |

### InGaAs spacer

- 100:1 smaller $I_{off}$ compared to InGaAs spacer

| $V_{GS}$ (V) | $|I_D|$ (mA/µm) |
|--------------|----------------|
| -0.2         | 10^-9          |
| 0            | 10^-8          |
| 0.2          | 10^-7          |
| 0.4          | 10^-6          |
| 0.6          | 10^-5          |

- Minimum $I_{off}$ ~ 60 pA/µm at $V_{D}$=0.5V for $L_g$-30 nm
I_{on} vs L_g at I_{off} = 1 \text{nA/\mu m}

- Peak I_{on} = 150 \text{\mu A/\mu m} at V_{DS}=0.5\text{V} for L_g-45 nm devices.
$I_{on}$ vs $L_g$ at $I_{off} = 100$ nA/µm

- Peak $I_{on} = 415$ µA/µm at $V_{DS} = 0.5V$ for this work.
- Ultrathin InAs channel shows highest $I_{on}$. 

![Graph](image_url)
Barrier Leakage
Channel Leakage

I_{on} = 150 \mu A/\mu m
at I_{off} = 1 nA/\mu m

I_{on} = 500 \mu A/\mu m
at I_{off} = 100 nA/\mu m
Recessed InP source/drain spacers enable III-V MOSFETs for low power logic.

Thank you!

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