Nanometer InP Electron Devices for VLSI and THz Applications

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S. Lee, C.-Y. Huang, D. Elias, V. Chobpattanna, J. Rode, H.-W. Chiang, P. Choudhary, R. Maurer, , A.C. Gossard, S. Stemmer: UCSB

M. Urteaga, B. Brar: Teledyne Scientific
nm FETs & VLSI: how small can we go?

4 nm FET: an engineering grand challenge

Can we make even good 8nm FETs?

Can we manage $CV^2$ dissipation? Are tunnel FETs viable? Alternatives?

Will 2-D semiconductors scale better than bulk?

Perhaps bulk semiconductors can do very well.
High-frequency electronics: How high can it go?

820 GHz transistor ICs today

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^9</td>
</tr>
<tr>
<td>10^10</td>
</tr>
<tr>
<td>10^11</td>
</tr>
<tr>
<td>10^12</td>
</tr>
<tr>
<td>10^13</td>
</tr>
<tr>
<td>10^14</td>
</tr>
<tr>
<td>10^15</td>
</tr>
</tbody>
</table>

- microwave
  - SHF* 3-30 GHz
  - 10-1 cm

- mm-wave
  - EHF* 30-300 GHz
  - 10-1 mm

- sub-mm-wave
  - THF* 0.3-3 THz
  - 1-0.1 mm

- mid-IR
  - 6-100 THz
  - 50-3 μm

- far-IR: 0.3-6 THz

- near-IR
  - 100-385 THz
  - 3-0.78 μm

- mid-IR
  - 6-100 THz
  - 50-3 μm

- THF*
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  - 1-0.1 mm

- far-IR: 0.3-6 THz

- near-IR
  - 100-385 THz
  - 3-0.78 μm

- optical
  - 385-790 THz

Applications

- 100+ Gb/s wireless networks
- Video-resolution radar → fly & drive through fog & rain
- near-Terabit optical fiber links

Transistor Goal: < 3 dB noise, >1 W power, 10% efficiency, 50-500 GHz
nm

(III-V) MOSFETs
**Why III-V MOS?**

**III-V vs. Si:** Low $m^*$ $\rightarrow$ higher velocity. Fewer states $\rightarrow$ less scattering $\rightarrow$ higher current. Can then trade for lower voltage or smaller FETs.

Problems: Low $m^*$ $\rightarrow$ less charge. Low $m^*$ $\rightarrow$ more S/D tunneling. Narrow bandgap $\rightarrow$ more band-band tunneling, impact ionization.
nm/VLSI MOSFET Scaling: Targets

<table>
<thead>
<tr>
<th>FET parameter</th>
<th>?? nm Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>~10 nm</td>
</tr>
<tr>
<td>current density (mA/mm)</td>
<td>1 mA/μm @0.5V</td>
</tr>
<tr>
<td>transport mass</td>
<td></td>
</tr>
<tr>
<td>2DEG electron density</td>
<td>3*10^{12}/cm^2</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td></td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>0.5 nm (fin: 1.0 nm)</td>
</tr>
<tr>
<td>channel thickness</td>
<td>2.5 nm (fin: 5 nm)</td>
</tr>
<tr>
<td>channel state density</td>
<td></td>
</tr>
<tr>
<td>contact resistivities</td>
<td>0.4 Ω-μm^2</td>
</tr>
</tbody>
</table>
Research III-V MOS: Lateral Spacers & Tunneling

**Small S/D contact pitch**
- N+ source
- N+ drain
- channel
- barrier
- no lateral gate-drain space

**MOS-HEMT with large contact pitch**
- N+ source
- N+ drain
- channel
- barrier
- InP barrier
- ~70 nm gate-drain space

Lin, IEDM2013

Lin, IEDM2013

UCSB
We must build devices with small S/D pitch.

contact pitch ~ 3 times lithographic half-pitch (technology node dimension)

Small S/D pitch hard to realize if we require ~20-50nm lateral gate-drain spacers!
Vertical spacers: less leakage, small S/D pitch

Suppress band-band tunneling, S/D tunneling. Long gate length, small footprint.
MOSFET: 2.5nm ZrO$_2$ / 1nm Al$_2$O$_3$ / 2.5nm InAs

High-k(Al$_2$O$_x$N$_y$/ZrO$_2$)

Spacer/ N+ S/D
(In$_{0.53}$Ga$_{0.47}$As)

Channel (InAs)

Back Barrier (In$_{0.52}$Al$_{0.48}$As)

Gate metal (Ni/Au)

Substrate (InP)

2.7 nm InAs channel (strained)

2.5 nm ZrO$_2$

1 nm Al$_2$O$_x$N$_y$

Courtesy of S. Kraemer (UCSB)  *Heavy elements look brighter  Lee et al., 2014 VSLI Symposium
MOSFET: 2.5nm ZrO$_2$/1nm Al$_2$O$_3$/2.5nm InAs

Current Density ($mA/\mu m$)

Gate Bias (V)

$g_m$ (mS/\mu m)

DIBL = 76 mV/V

$V_f$ = -85 mV at 1 $\mu$A/\mu m

$SS_{min}$ ~ 72 mV/dec. (at $V_{DS}$ = 0.1 V)

$SS_{min}$ ~ 77 mV/dec. (at $V_{DS}$ = 0.5 V)

$V_{DS}$ = 0.1 to 0.7 V

0.2 V increment

Lee et al., 2014 VSLI Symposium

2.7 nm InAs channel (strained)
MOSFET: 2.5nm ZrO$_2$/ 1nm Al$_2$O$_3$ / 2.5nm InAs

Performance:
Equals Intel 22nm NMOS finFET (HP), surpasses 14nm FDSOI

Dielectrics: V. Chobpattana, et al., APL 2014
FETs: Lee et al., 2014 VLSI Symposium
Channel, Dielectric, and Spacer Design

**On-current:**

*Thin dielectrics, thin channels; too thin → scattering. high indium content (not clear why).*

**Subthreshold:**

*dielectrics, thin channels, thick spacers*

**Tunneling:**

*thin channels, low indium content, thick spacers*
Double Heterojunction MOSFETs: Low Leakage

**Meet GP (1nA/μm), LP (30pA/μm), ULP (10 pA/μm) specs?**

**InP spacer in highest-field region: BTBT**

**InGaAs spacer in lower-field regions: less added resistance**


Byeongkyu Cho: MS report
FinFETs by Atomic Layer Epitaxy: Why?

**FinFETs:**
body must be < 4 nm thick body for 8 nm $L_g$

Need smooth interfaces, precise fin thickness control

Is fin dry-etching feasible? Damage?
finFET by Sidewall Epitaxial Growth

**fin template**
- SiN mask
- etch stop layer
- InP template; (011) facet

**channel ALE**
- ALE InGaAs

**dummy gate**
- HSQ mask

**S/D regrowth**
- N+ InGaAs source/drain

**remove masks**

**release fins**
- transistor footprint width
- fin pitch
- height

Cohen-Elias et al., DRC 2013
finFET by Sidewall Epitaxial Growth

$HfO_2$  →  fin, $\sim 8$nm  →  TiN

50 nm fin pitch

100 nm fin pitch

10 nm thick fins, 100 nm tall

source
channel
drain

BTBT: need $< 5$nm fins

Cohen-Elias et al., DRC 2013
THz Transistors
### THz Transistor Scaling Laws (to double bandwidth)

#### FET parameter change

| Parameter                                      | Change  
|-----------------------------------------------|---------
| gate length                                   | decrease 2:1 |
| current density (mA/mm), $g_m$ (mS/mm)        | increase 2:1 |
| transport mass                                | constant |
| 2DEG electron density                         | increase 2:1 |
| gate-channel capacitance density              | increase 2:1 |
| dielectric equivalent thickness               | decrease 2:1 |
| channel thickness                             | decrease 2:1 |
| channel state density                         | increase 2:1 |
| contact resistivities                         | decrease 4:1 |

#### HBT parameter change

| Parameter                                      | Change  
|-----------------------------------------------|---------
| emitter & collector junction widths           | decrease 4:1 |
| current density (mA/mm$^2$)                   | increase 4:1 |
| current density (mA/mm)                       | constant |
| collector depletion thickness                 | decrease 2:1 |
| base thickness                                | decrease 1.4:1 |
| emitter & base contact resistivities          | decrease 4:1 |
2-3 THz Field-Effect Transistors are Feasible.

3 THz FETs realized by:
- Regrown low-resistivity source/drain
- Very thin channels, high-K dielectrics
- Gates scaled to 9 nm junctions

Impact:
- Sensitive, low-noise receivers from 100-1000 GHz.

3 dB less noise → need 3 dB less transmit power.
III-V MOS: Benefits THz HEMTs

**VLSI III-V MOS**

**THz III-V MOS**

- **Gm** (mS/μm)
- **Current Density** (mA/μm)
- **Gate Bias (V)**
- **Drain Bias (V)**

- **V_DS = 0.1 to 0.7 V**
- **0.2 V increment**

- **ALD HfO_2**
- **N+ S/D regrowth**

- **Pt/Au**
- **lateral drain offset**

- **InP barrier**
- **N+ S/D regrowth**

- **InAs channel barrier**

- **3mS/μm**

- **V_GS = -0.4 V to 1.0 V**
- **0.2 V increment**

- **R_on = 201 Ohm-μm**
- **at V_GS = 1.0 V**

S. Lee et al., EDL, June 2014
3 THz Bipolar Transistors are Feasible.

Needs

0.5 \( \Omega \cdot \mu \text{m}^2 \) resistivity contacts
ultra-shallow \( \rightarrow \) refractory

\(~100 \text{ mA/} \mu \text{m}^2\) current densities

16 nm junctions

Impact:

Efficient power amplifiers,
ADCs
complex mm-wave systems
from 100-1000 GHz.

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Scaling Node} & 64 & 32 & 16 & \text{nm} \\
\text{Emitter Width} & 64 & 32 & 16 & \text{nm} \\
\text{Resistivity} & 2 & 1 & 0.5 & \Omega \cdot \mu \text{m}^2 \\
\text{Base Thickness} & 18 & 15 & 13 & \text{nm} \\
\text{Contact width} & 60 & 30 & 15 & \text{nm} \\
\text{Contact } \rho & 2.5 & 1.25 & 0.63 & \Omega \cdot \mu \text{m}^2 \\
\text{Collector Width} & 180 & 90 & 45 & \text{nm} \\
\text{Thickness} & 53 & 37.5 & 26 & \text{nm} \\
\text{Current Density} & 36 & 72 & 140 & \text{mA/} \mu \text{m}^2 \\
\hline
\end{array}
\]

\[
\begin{array}{c|c|c|c|}
\text{ } & \text{ } & \text{ } & \text{THz} \\
\hline
f_c & 1.0 & 1.4 & 2.0 \\
\text{max} & 2.0 & 2.8 & 4.0 \\
\hline
\end{array}
\]
THz InP HBTs: Performance @ 128 nm Node

UCSB: V. Jain et al: 2011 DRC

Gain (dB) vs Frequency (Hz)

- $H_{21}$
- $U$
- $f_\tau = 480 \text{ GHz}$
- $f_{\text{max}} = 1.0 \text{ THz}$

$A_{je} = 0.22 \times 2.7 \mu m^2$

UCSB: J. Rode et al: unpublished

Teledyne: M. Urteaga et al: 2011 DRC

Gain (dB) vs Frequency (Hz)

- $f_i = 521 \text{ GHz}$
- $f_{\text{max}} = 1.15 \text{ THz}$

UCSB: J. Rode et al: unpublished

VCEO=4.3 V

$BVCEO=4.3 \text{ V}$

$V_{CE} = 1.6 \text{ V}$

$\text{IC}=6.9 \text{ mA}$
InP HBT Integrated Circuits: 600 GHz & Beyond

614 GHz fundamental VCO
M. Seo, TSC / UCSB

340 GHz dynamic frequency divider
M. Seo, UCSB/TSC
IMS 2010

620 GHz, 20 dB gain amplifier
M Seo, TSC
IMS 2013

Not shown: 670 GHz HBT amplifier
J. Hacker, TSC, IMS 2013

300 GHz fundamental PLL
M. Seo, TSC
IMS 2011

81 GHz 470 mW power amplifier
H-C Park UCSB
IMS 2014

204 GHz static frequency divider (ECL master-slave latch)
Z. Griffith, TSC
CSIC 2010

220 GHz 180 mW power amplifier
T. Reed, UCSB
CSICS 2013

600 GHz Integrated Transmitter
PLL + Mixer
M. Seo, TSC

Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC
**Extreme Currents: Quadratic I-V Characteristics**

**Boltzmann**

Energy diagram showing the Fermi level ($E_F$) with occupancy and emitter-base (base) labels.

**Fermi-Dirac**

Energy diagram showing the Fermi level ($E_F$) with occupancy and emitter-base (base) labels.

**Highly Degenerate**

Energy diagram showing the Fermi level ($E_F$) with occupancy and emitter-base (base) labels.

---

**Highly Degenerate limit → Transconductance varies as $J^{1/2}(m^*)^{1/2} → must increase m^*$**

**High currents → transconductance less than $qI/kT → bandwidth decreases**
Ultra Low-Resistivity Refractory Contacts

Refractory: robust under high-current operation.
Low penetration depth: \( \sim 1 \) nm.
Performance sufficient for 32 nm /2.8 THz node.

Landauer:

\[
\rho_c = \left( \frac{\hbar}{q^2} \right) \cdot \left( \frac{8\pi}{3} \right)^{2/3} \cdot \frac{1}{T} \cdot \frac{1}{n^{2/3}}
\]
Refractory Emitter Contact and Via

- Sputtered, dry-etched W/TiW via
- Low-resistivity Mo contact

Refractory metals → high currents
Needed: Much Better Base Ohmic Contacts

Pt/Ti/Pd/Au
(3.5/12/17/70 nm)

~5 nm deep Pt contact reaction
(into 25 nm base)
Two-Step Base Contact Process

1) Blanket deposit 1nm Pt
2) Blanket deposit 10nm Ru (refractory)
3) Pattern deposit Ti/Au

Surface not exposed to photoresist $\rightarrow$ less surface contamination
1 nm Pt layer: 2-3 nm surface penetration
Thick Au: low metal resistance
Two-Step Base Contact Process

- Increased surface doping: reduced contact resistivity, increased Auger recombination.
- Surface doping spike 2-5nm thick.
- Need limited-penetration metal.
"Near-Refractory" Base Ohmic Contacts

- base contact
- Au
- Ti
- Pt-InGaAs reaction
- emitter
- Ru
- 17 nm
- setback
- grade
- collector
- 14.1 nm
- 2.7 nm
THz InP HBTs

a few more things to fix ...
1-D, 30 THz diodes
1-D (nm) Diodes for 30THz mixing/detection

Transit time: $\tau_{\text{transit}} \propto T_{\text{depl}} / v_{\text{Fermi}} \rightarrow$ make $T_{\text{depl}} \approx 3.5$ nm

Depletion capacitance: $C_{\text{depl}} \approx \varepsilon A / T_{\text{depl}} \rightarrow$ make $A$ very small.

Junction impedance: $r_{\text{on}} = \pi kT/qI \rightarrow$ make $J = I/A$ very large

big problem: degenerate injection, $r_{\text{on}} \gg kT/qI$

Solution: array of 1-D diode junctions $\rightarrow r_{\text{on}} = \pi \hbar / q^2$

On-state time constant:

$r_{\text{on}} C_{\text{depl}} = (\pi \hbar / q^2) \cdot (\varepsilon A / T_{\text{depl}}) \propto A / T_{\text{depl}} \rightarrow$ make area small
What do we want?

VLSI: lots of on-current, no off-current, low voltage

THz: high frequencies. Low noise, high power, high gain.

How do we get it?

Extreme current densities
Extremely thin dielectrics (FETs)
Extremely low-resistivity contacts
few-nm critical dimensions
...and sufficient states to carry the current
Backup slides
InAs/InGaAs MOSET: Process Flow

Development process flow does not provide a small S/D contact pitch, But: in manufacturing, the vertical spacer can provide a small S/D contact pitch.
set aside slides
Transistor Design: What Matters?
Scaling: How \((V,I,R,C,\tau)\) varies with geometry

Depletion Layers
\[
C = \varepsilon \cdot \frac{A}{T}
\]
\[
\tau = \frac{T}{2v}
\]
\[
\frac{I_{\text{max}}}{A} = \frac{4\varepsilon v_{\text{sat}}(V_{\text{appl}} + \phi)}{T^2}
\]

Bulk and Contact Resistances
\[
R \approx \rho_{\text{contact}} / A
\]

Fringing Capacitances
\[
\frac{C_{\text{fingering}}}{L} \sim \varepsilon
\]

Thermal Resistance
\[
\Delta T_{\text{IC}} \propto \frac{P_{\text{IC}}}{K_{\text{th}} L}
\]
\[
\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{\text{th}} L \ln\left(\frac{L}{W}\right)}
\]

Available states to carry current
\[
x \rightarrow \text{capacitance, transconductance, contact resistance}
\]
**THz & nm Transistors: State Density Limits**

1-D conductivity: $\sigma = \frac{q^2}{\pi \hbar}$ (Landauer)

<table>
<thead>
<tr>
<th></th>
<th>2-D: FET</th>
<th>3-D: Bipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>$C_{DOS} = \frac{q^2 m^*}{2\pi \hbar^2}$</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>$J_{\text{sheet}} = \frac{2^{3/2} q^{5/2} (m^*)^{1/2} V^{3/2}}{3\pi^2 \hbar^2}$</td>
<td>$J = \frac{q^3 m* V^2}{4\pi^2 \hbar^3}$</td>
</tr>
<tr>
<td>Conductivity</td>
<td>$\sigma_c = \left(\frac{q^2}{\hbar}\right) \cdot \left(\frac{2}{\pi^3}\right)^{1/2} \cdot n^{1/2}$</td>
<td>$\sigma_c = \left(\frac{q^2}{\hbar}\right) \cdot \left(\frac{3}{8\pi}\right)^{2/3} \cdot n^{2/3}$</td>
</tr>
</tbody>
</table>

# available states / energy determines on-state capacitance, current & transconductance, contact/access resistance