Record $I_{on}$ (0.50 mA/μm at $V_{DD} = 0.5$ V and $I_{off} = 100$ nA/μm) 25 nm-Gate-Length ZrO$_2$/InAs/InAlAs MOSFETs

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Why III-V MOSFETs in VLSI applications?

Low $m^*$ in III-V material $\Rightarrow$ high $v_{\text{inj}}$
$\Rightarrow$ high transconductance

More transconductance per gate width
more current $\Rightarrow$ lower intrinsic delay
-or- reduced $V_{DD}$ $\Rightarrow$ less power consumption
-or- small FETs $\Rightarrow$ reduced IC size

Other advantages
Wide range of available materials
nm-precise growth $\Rightarrow$ 1-2 nm thick channel
Larger $\Delta E_c$ $\Rightarrow$ Better confinement, Small EOT
### Key Design Considerations

**Source/Drain:**
- Low $\rho_c \Rightarrow$ Small contact size
- Self-aligned $\Rightarrow$ Small contact pitch
- Shallow $\Rightarrow$ Scaling (electrostatics)

**Dielectric:**
- Thin $\Rightarrow$ high $I_{on}$, better SS and DIBL
- Low $D_{it} \Rightarrow$ Better SS

**Channel:**
- Thin $\Rightarrow$ Electrostatics
- Thin and wide bandgap $\Rightarrow$ Small band-band tunneling
- Thick and narrow bandgap $\Rightarrow$ higher injection velocity
**FET Structures**

**Inversion mode MOSFETs**
- Self-aligned ✔
- Implant damage ❌
- Large $R_{\text{access}}$ (limited doping) ❌

**MOS-HEMT**
- Good short channel effect ✔
- Large device footprint ❌
- Large $R_{\text{access}}$ (Barrier) ❌

**Trench-etch**
- Small footprint ✔
- Small $R_{\text{access}}$ ✔
- Limited $L_g$ scaling (wet etch) ❌

**Regrown S/D with gate-first**
- Small footprint and $L_g$ ✔
- Small $R_{\text{access}}$ ✔
- Abrupt junction ✔
- High damage (gate-stack etch) ❌

**Regrown S/D with gate-Last**
- Low damage (No dry etch) ✔
**Gate-Last Process (Simplified for Development)**

### Channel growth

**By MBE**

- **Cap:** 2 nm In$_{0.53}$Ga$_{0.47}$As (U.I.D)
- **Channel:** 3.5 nm InAs (Strained)
- **Setback:** In$_{0.52}$Al$_{0.48}$As Setback (U.I.D)
  - Pulse Doping (Si 2X10$^{12}$/cm$^2$)
- **Back Barrier:** In$_{0.52}$Al$_{0.48}$As (U.I.D)
- **P-type Doped Barrier:** In$_{0.52}$Al$_{0.48}$As (Be 10$^{17}$/cm$^3$)
- **Substrate:** InP (Semi-insulating)

### Dummy gate formation

**e-beam lithography**

- **HSQ**
  - Al$_2$O$_3$
  - InGaAs Cap
  - InAs Channel
  - In$_{0.52}$Al$_{0.48}$As Setback
  - In$_{0.52}$Al$_{0.48}$As Back Barrier
  - Pulse Doping
  - P-type Doped Barrier
  - InP (Substrate)

### Vertical spacer and N+ S/D regrowth in MOCVD

- **50 nm N+ In$_{0.53}$Ga$_{0.47}$As**
- **10 nm In$_{0.53}$Ga$_{0.47}$As**
- **Vertical Spacer**

### S/D metal contact formation

- **Ti/Pd/Au**
  - 0.7/3.0 nm Al$_2$O$_3$/N$_2$/ZrO$_2$

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**Mesa-isolation**

**Surface digital etching**

- **N+ In$_{0.53}$Ga$_{0.47}$As**
- **Regrown S/D**
  - 12 nm In$_{0.53}$Ga$_{0.47}$As
  - 2.5 nm InAs Channel
  - In$_{0.52}$Al$_{0.48}$As Setback
  - In$_{0.52}$Al$_{0.48}$As Back Barrier
  - P-type Doped Barrier
  - InP (Substrate)

**Gate stack formation**

- **N+ In$_{0.53}$Ga$_{0.47}$As**
  - (gate metal)
- **Regrown S/D**
  - 12 nm In$_{0.53}$Ga$_{0.47}$As
  - 2.5 nm InAs Channel
  - In$_{0.52}$Al$_{0.48}$As Setback
  - In$_{0.52}$Al$_{0.48}$As Back Barrier
  - P-type Doped Barrier
  - InP (Substrate)

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**S/D metal contact formation**

- **N+ In$_{0.53}$Ga$_{0.47}$As**
  - (gate metal)
- **Regrown S/D**
  - 12 nm In$_{0.53}$Ga$_{0.47}$As
  - 2.5 nm InAs Channel
  - In$_{0.52}$Al$_{0.48}$As Setback
  - In$_{0.52}$Al$_{0.48}$As Back Barrier
  - P-type Doped Barrier
  - InP (Substrate)
High-k : MOSCAP with 0.7/5.0 nm Al$_2$O$_{x}$N$_{y}$/ZrO$_2$

- Dielectric constant for ZrO$_2$ is 23; EOT is ~1 nm.
- 3.5 µF/cm$^2$ accumulation capacitance at 1MHz.
- ~1X10$^{12}$/cm$^2$-eV $D_{it}$ near midgap.
- Gate leakage < 1 A/cm$^2$ up $V_G$=2 V.

(V. Chobpattana, et al., ‘Scaled ZrO2 dielectrics for InGaAs gate stack with low interface trap densities’, APL 2014)
Off-state leakage and S/D spacers

Small S/D contact pitch

- N+ source
- N+ drain
- channel
- barrier

MOS-HEMT with large contact pitch

- N+ source
- N+ drain
- channel
- barrier

Band-band tunneling impact ionization

\[ L_g = 18 \text{ nm} \]
\[ V_{DS} = 0.1, 0.5 \text{ V} \]

\[ L_g = 35 \text{ nm} \]

Large lateral spacer \(\rightarrow\) low leakage, good short channel immunity

Large lateral spacer \(\rightarrow\) large S/D pitch

Current Density (mA/\(\mu\)m)

\[ g_m \text{ (mS/\(\mu\)m)} \]

Gate Bias (V)

D-H. Kim, IEDM 2012
Vertical Spacers $\rightarrow$ reduced off-state leakage

- Larger spacer
  $\rightarrow$ better short channel effect at short and long channels

(S. Lee, et al., EDL, June 2014)
Cross-sectional STEM image

- High-k($\text{Al}_2\text{O}_3\text{N}_y\text{ZrO}_2$)
- Gate metal (Ni/Au)
- Spacer/ N+ S/D ($\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$)
- Channel (InAs)
- Back Barrier ($\text{In}_{0.52}\text{Al}_{0.48}\text{As}$)
- Substrate (InP)

2.7 nm InAs channel (strained)
2.5 nm ZrO$_2$
1 nm Al$_2$O$_3$N$_{y}$

*Heavy elements look brighter

Courtesy of S. Kraemer (UCSB)
I-V characteristics for long channel device ($L_g = 1 \mu m$)

- 61 mV/dec Subthreshold swing at $V_{DS}=0.1$ V
- Negligible hysteresis
- $<1$ A/cm$^2$ gate leakage at measured bias range

$SS_{min} \sim 61$ mV/dec. (at $V_{DS} = 0.1$ V)

$SS_{min} \sim 63$ mV/dec. (at $V_{DS} = 0.5$ V)
I-V characteristics for short channel devices (L_g = 25 nm)

- ~2.4 mS/µm Peak g_m at V_DS=0.5 V
- ~300 Ohm-µm on-resistance at V_GS=0.7 V
- 77 mV/dec Subthreshold Swing at V_DS=0.5 V, 76 mV/V DIBL at 1 μA/µm
- 0.5 mA/µm I_on at I_off=100 nA/µm and V_DD=0.5 V
Source/drain series resistance

- From TLM measurement for N+S/D, $R_{\text{N+S/D sheet}} = 25 \text{ ohm/sq}$, $\rho_c = \sim 5.3 \text{ ohm-}\mu\text{m}^2$
- $R_{\text{spacer}}$ is estimated to be $\sim 35 \text{ ohm-}\mu\text{m}$ for both sides

<table>
<thead>
<tr>
<th>$R_{\text{contact}}$ [Ohm-\mu m]</th>
<th>$R_{\text{N+S/D}}$ [Ohm-\mu m]</th>
<th>$R_{\text{spacer}}$ [Ohm-\mu m]</th>
<th>$R_{\text{ballistic}}$ [Ohm-\mu m]</th>
<th>$R_{\text{on at zero } L_g}$ [Ohm-\mu m]</th>
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<tr>
<td>25</td>
<td>60</td>
<td>35</td>
<td>50</td>
<td>170</td>
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for both source and drain sides
Performance comparison: 2.5 nm VS 5.0 nm-thick channel

- Better SS at all gate length scale:
  - Better electrostatics, reduced BTBT
  - ~1:10 reduction in minimum off-state leakage
  - ~5:1 increase in gate leakage $\Rightarrow$ increased eigenstate
Performance comparison: 2.5 nm VS 5.0 nm-thick channel

- Peak $g_m$ vs. Gate Length
- Carrier Density vs. Gate Bias
- Gate Capacitance vs. Gate Bias
- Energy levels for different channel thicknesses

1D-Poisson-Schrödinger solver (coded by W. Frensley, UT Dallas)
SS and DIBL vs. $L_g$ (Benchmarking)

- <80 mV/dec at sub-30 nm $L_g$ and $V_{DS}=0.5$ V
- Record low subthreshold swing among any reported III-V FETs.
- Lowest DIBL among planar-type III-V FETs.

Peak $g_m$ and $I_{on}$ at fixed $I_{off}$ vs. $L_g$ (Benchmarking)

- >2.4 mS/µm peak $g_m$ at $V_{DS}=0.5$ V and sub-30 nm $L_g$.
- Highest $I_{on}$ at $I_{off}=100$ nA/µm and $V_{DD}=0.5$ V
- 0.5 mA/µm $I_{on}$ at sub-30 nm $L_g$

Benchmark with 22 nm node Si Fin- and nanowire FET

- Intel 22 nm FinFETs (HP) : ~0.5 mA/µm (?) @ $V_{GS}=0.5$ V, $V_{DS}=0.75$ V
- IBM 22 nm nanowire : ~0.4 mA/µm @ $V_{GS}=0.5$ V, $V_{DS}=0.5$ V
- Comparable performance with state-of-the-art Si-FinFETs (nanowire).
Conclusion

- Developed vertical spacer to reduce off-state leakage and to improve short channel effect.
- Integrated sub-1 nm EOT ZrO$_2$ high-k with low $D_{it}$
- Obtained 61 mV/dec at $V_{DS} = 0.1$ V and 1 $\mu$m-$L_g$.
- Obtained 0.5 mA/$\mu$m at $I_{off} = 100$ nA/$\mu$m and $V_{DD} = 0.5$ V (best reported $I_{on}$ among any reported III-V MOSFETs)
- Achieved comparable $I_{on}$ to state-of-art multi-gate Si-FETs
Acknowledgment

Thanks for your attention!
Questions?

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