50-500GHz Wireless Technologies: Transistors, ICs, and Systems

Mark Rodwell, UCSB


M. Urteaga, J. Hacker, Z. Griffith, B. Brar: Teledyne Scientific and Imaging

M. Seo: Sungkyunkwan University

* Now with Intel
Why mm-wave wireless?
Links
**mm-Waves: high-capacity mobile communications**

**Features:**
- Spatially-multiplexed mm-wave base stations
- MM-wave backhaul

**Examples:**
- 140 GHz, 10 Gb/s Adaptive Picocell Backhaul
- 60 GHz, 1 Tb/s Spatially-Multiplexed Base Station

**Needs → Research:**
- **RF front end:** phased array ICs, high-power transmitters, low-noise receivers
- **IF/baseband:** ICs for multi-beam beamforming, for ISI/multipath suppression, ...
mm-Waves: benefits & challenges

Large available spectrum

- Large available spectrum due to high frequency bands.

Massive # parallel channels

- Massive number of parallel channels required for increased capacity.
- Spatial multiplexing used to overcome high attenuation.

Need phased arrays (overcome high attenuation)

- Phased arrays are needed to overcome high attenuation in foul weather.

Need mesh networks

- Mesh networks are used for robust connectivity.
- Beamsteering and mesh networks help avoid blockage.

Angular resolution $\approx \frac{\text{wavelength}}{\text{array width}}$

Channel capacity $\propto \frac{B^2}{\lambda R + 1}$

P received

\[ \frac{P_{\text{received}}}{P_{\text{transmit}}} \propto N_{\text{receive}} N_{\text{transmit}} \frac{\lambda^2}{R^2} e^{-\alpha R} \]

Object having area $\sim \lambda R$ will block beam.

Blockage is avoided using beamsteering and mesh networks.

...high-frequency signals are easily blocked.

...this is easier at high frequencies.
mm-Wave LOS MIMO: multi-channel for high capacity

\[ B = ND \]

\[ N = \frac{B^2}{\lambda R} + 1 \]

number of channels \( \propto \frac{(\text{aperture area})^2}{(\text{wavelength} \cdot \text{distance})^2} \)

Torklinson: 2006 Allerton Conference
Sheldon: 2010 IEEE APS-URSI
Spatial Multiplexing: massive capacity RF networks

multiple independent beams
each carrying different data
each independently aimed
# beams = # array elements

Hardware: multi-beam phased array ICs

transmit matrix  

trx array  

rcvr array  

receive matrix

--- signal 1 ---  --- signal N ---

--- signal 1 ---  --- signal N ---
Millimeter-wave imaging

10,000-pixel, 94GHz imaging array → 10,000 elements

Demonstrated:
SiGe, 1.3 kW (UCSD/Rebeiz)

Lower-power designs:
InP, CMOS, SiGe
(UCSB, UCSD, Virginia Poly.)

235 GHz video-rate synthetic aperture radar

1 transmitter, 1 receiver
100,000 pixels
20 Hz refresh rate
5 cm resolution @ 1km
50 Watt transmitter
(tube, solid-state driver)
140 GHz, 10 Gb/s Adaptive Picocell Backhaul

array: 2x32

90° (h) by 10° (v) scan

individual antennas 1.4x12 mm
140 GHz, 10 Gb/s Adaptive Picocell Backhaul

- 350 meters range in 50mm/hr rain
- Realistic packaging loss, operating & design margins

PAs: 24 dBm $P_{\text{sat}}$ (per element) $\rightarrow$ GaN or InP

LNAs: 4 dB noise figure $\rightarrow$ InP HEMT
340GHz, 160Gb/s spatially multiplexed backhaul

- Eight 20 Gb/s MIMO units: each an 8x8 array
- Individual antennas: 6x6 mm

1° beamwidth; 8° beamsteering

600 meters range in 50 mm/hr rain

Realistic packaging loss, operating & design margins

PAs: 14 dBm $P_{\text{sat}}$ (per element) $\rightarrow$ InP

LNAs: 7 dB noise figure $\rightarrow$ InP HEMT
Optimum array size for low system power

\[
\frac{P_{\text{receive}}}{P_{\text{transmit}}} \propto N^2 \frac{\lambda^2}{R^2} \Rightarrow P_{\text{transmit}} \propto \frac{1}{N^2}
\]

Total system power = \(\frac{P_{\text{transmit}}}{\text{efficiency}} + N\) (power of LNA, phase shifters…)

Do large arrays save power?

At optimum-size array, target PA output power is typically 10-200 mW
50-500 GHz Wireless Transceiver Architecture

III-V LNAs, III-V PAs → power, efficiency, noise
Si CMOS beamformer → integration scale

...similar to today's cell phones.

High-gain antenna → large area
→ much too big for monolithic integration
Transistors

HBT64J

- W
- TiW
- Mo
- InGaAs
- InP

Gain [dB]

- MAG/MSG
- $f_{max} = 1070$ GHz

- $H_{21}$
- $f_t = 480$ GHz

- $A_e = 0.2 \cdot 2.9 \, \mu m^2$
- $V_{ce} = 2.0 \, V$
- $J_e = 18 \, mA/\mu m^2$
mm-wave CMOS (examples)

210 GHz amplifier: 32 nm SOI, positive feedback, 15 dB, 3 stages
Wang et al. (Heydari), JSSC, March 2014

150 GHz amplifier: 65 nm bulk CMOS, 8.2 dB, 3 stages (250GHz $f_{\text{max}}$)
Seo et al. (UCSB), JSSC, December 2009
**mm-Wave CMOS won't scale much further**

**Gate dielectric can't be thinned**
→ on-current, $g_m$ can't increase

$g_m$ vs. $(\text{electron effective mass})/m_o$

- EOT + body thickness term = 1nm
- 0.3 nm
- 0.4 nm
- 0.6 nm

**Shorter gates give no less capacitance**
dominated by ends; ~1fF/μm total

**Maximum $g_m$, minimum $C$** → upper limit on $f_t$
about 350-400 GHz.

**Tungsten via resistances reduce the gain**
Inac et al, CSICS 2011

**Present finFETs have yet larger end capacitances**
III-V high-power transmitters, low-noise receivers

**Cell phones & WiFi:**
GaAs PAs, LNAs

**mm-wave links need**
high transmit power,
low receiver noise

0.47 W @86GHz
H Park, UCSB, IMS 2014

0.18 W @220GHz
T Reed, UCSB, CSICS 2013

1.9mW @585GHz
M Seo, TSC, IMS 2013
Making faster bipolar transistors

<table>
<thead>
<tr>
<th>Change</th>
<th>Specifics</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter &amp; collector junction widths</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density (mA/µm²)</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>current density (mA/µm)</td>
<td>constant</td>
</tr>
<tr>
<td>collector depletion thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.4:1</td>
</tr>
<tr>
<td>emitter &amp; base contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

Narrow junctions.
Thin layers
High current density
Ultra low resistivity contacts
THz HBTs: The key challenges

Obtaining good base contacts

_in HBT vs. in contact test structure_ (emitter contacts are fine)

RC parasitics along finger length

metal resistance, excess junction areas

Baraskar _et al_, Journal of Applied Physics, 2013
THz HBTs: double base metal process

- **Blanket surface clean (UV O₃ / HCl)**
  - strips organics, process residues, surface oxides

- **Blanket base metal**
  - no photoresist; no organic residues
  - Ru refractory diffusion barrier
  - 2 nm Pt: penetrates residual oxides

- **Thick Ti/Au base pad metal liftoff**
  - thick metal → low resistivity

Rode et al., IEEE TED, Aug. 2015
Reducing Emitter Length Effects

before

large base post

1100 nm

220 nm

small base post undercut

after

small base post

830 nm

50 nm

large base post undercut

small emitter end undercut

large emitter end undercut

Rode et al., IEEE TED, Aug. 2015
Reducing Emitter Length Effects

before

HBT64A

Pt/Ti/Pd/Au

100 nm

after

HBT64J

Ti/Au

Pt/Ru/Pt

thicker Au base metal

narrower collector junction

Rode et al., IEEE TED, Aug. 2015
InP HBTs: 1.07 THz @200nm, ?? @ 130nm

Rode et al., IEEE TED, Aug. 2015
**130nm / 1.1 THz InP HBT: ICs to 670 GHz**

- **614 GHz fundamental VCO**
  M. Seo, TSC / UCSB

- **620 GHz, 20 dB gain amplifier**
  M. Seo, TSC
  IMS 2013
  also: 670GHz amplifier
  J. Hacker, TSC
  IMS 2013 (not shown)

- **300 GHz fundamental PLL**
  M. Seo, TSC
  IMS 2011

- **204 GHz static frequency divider (ECL master-slave latch)**
  Z. Griffith, TSC
  CSIC 2010

- **220 GHz 180 mW power amplifier**
  T. Reed, UCSB
  CSICS 2013

- **81 GHz 470 mW power amplifier**
  H-C Park UCSB
  IMS 2014

- **600 GHz Integrated Transmitter**
  PLL + Mixer
  M. Seo TSC

- **Integrated 300/350GHz Receivers: LNA/Mixer/VCO**
  M. Seo TSC

- **340 GHz dynamic frequency divider**
  M. Seo, UCSB/TSC
  IMS 2010
Towards a 3 THz InP Bipolar Transistor

Extreme base doping $\rightarrow$ low-resistivity contacts $\rightarrow$ high $f_{\text{max}}$

Extreme base doping $\rightarrow$ fast Auger ($NP^2$) recombination $\rightarrow$ low $\beta$.

Solution: very strong base compositional grading $\rightarrow$ high $\beta$
1/2-THz SiGe HBTs

500 GHz $f_{\text{max}}$ SiGe HBTs Heinemann et al. (IHP), 2010 IEDM

16-element multiplier array @ 500GHz (1 mW total output)
U. Pfeiffer et. al. (Wuppertal / IHP), 2014 ISSCC
Towards a 2 THz SiGe Bipolar Transistor

### Similar scaling

<table>
<thead>
<tr>
<th>InP</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>emitter</td>
<td></td>
</tr>
<tr>
<td>junction width</td>
<td>64</td>
</tr>
<tr>
<td>access resistivity</td>
<td>2</td>
</tr>
<tr>
<td>base</td>
<td></td>
</tr>
<tr>
<td>contact width</td>
<td>64</td>
</tr>
<tr>
<td>contact resistivity</td>
<td>2.5</td>
</tr>
<tr>
<td>collector</td>
<td></td>
</tr>
<tr>
<td>thickness</td>
<td>53</td>
</tr>
<tr>
<td>current density</td>
<td>36</td>
</tr>
<tr>
<td>breakdown</td>
<td>2.75</td>
</tr>
<tr>
<td>$f_\tau$</td>
<td>1000</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>2000</td>
</tr>
</tbody>
</table>

### Key distinction: Breakdown

InP has:
- thicker collector at same $f_\tau$,
- wider collector bandgap

### Key requirements:

low resistivity Ohmic contacts
note the high current densities

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions
Towards at 2.5 THz HEMT

First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 (Northrop-Grumman)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Change</th>
</tr>
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<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/mm), $g_m$ (mS/mm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport mass</td>
<td>constant</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

Need thinner dielectrics, better contacts
Towards at 2.5 THz HEMT

**VLSI III-V MOS**

- Ti/Pd/Au
- N+InGaAs
- N+InP
- Doping-graded InP
- U.I.D. InP spacer
- 1.5 nm InGaAs
- Ni/Ni
- 0.5 nm InGaAs
- Ti/Pd/Au

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>InAlAs U.I.D. spacer</td>
<td>5 nm</td>
<td></td>
</tr>
<tr>
<td>2 nm 1E19 cm^-3 N+InAlAs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 nm InAlAs U.I.D. buffer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>250 nm 1E17 cm^-3 P-InAlAs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 nm InAlAs U.I.D. buffer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S.I. InP substrate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**THz III-V MOS**

- InAlAs barrier
- ALD ZrO₂
- Pt/Au

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>36, 18, 9 nm</td>
</tr>
<tr>
<td>EOT</td>
<td>0.8, 0.4, 0.2 nm</td>
</tr>
<tr>
<td>well thickness</td>
<td>5.6, 2.8, 1.4 nm</td>
</tr>
<tr>
<td>effective mass</td>
<td>0.05, 0.08, 0.08 times m₀</td>
</tr>
<tr>
<td># bands</td>
<td>1, 1, 1</td>
</tr>
<tr>
<td>S/D resistivity</td>
<td>150, 74, 37 Ω·μm</td>
</tr>
<tr>
<td>extrinsic gᵣ</td>
<td>2.5, 4.2, 6.4 mS/μm</td>
</tr>
<tr>
<td>on-current</td>
<td>0.55, 0.8, 1.1 mA/μm</td>
</tr>
<tr>
<td>fᵣ</td>
<td>0.70, 1.2, 2.0 THz</td>
</tr>
<tr>
<td>f_max</td>
<td>0.81, 1.4, 2.7 THz</td>
</tr>
</tbody>
</table>

C. Y. Huang et al., DRC 2015
Power Amplifiers
220 GHz power amplifiers; 256nm InP HBT

90 mW

180 mW (330 mW design; thermally limited)

164 mW, 0.43 W/mm, 2.4% PAE

T. Reed (UCSB), Z. Griffith (TSC), IEEE CSIC 2012 & 2013; Teledyne 256nm InP HBT
mm-Wave Power Amplifier: Challenges

needed: High power / High efficiency / Small die area (low cost)

Extensive power combining

Compact power-combining

\[
\text{PAE} = \eta_{\text{drain/collector}} \left(1 - \frac{1}{\text{Gain}}\right) \cdot \eta_{\text{power-combiner}}
\]

Class E/D/F are poor @ mm-wave
insufficient \( f_{\text{max}} \),
high losses in harmonic terminations

Efficient power-combining

Goal: efficient, compact mm-wave power-combiners
Parallel Power-Combining

Output power: \( P_{\text{OUT}} = N \times V \times I \)
Parallel connection increases \( P_{\text{OUT}} \)

Load Impedance: \( Z_{\text{OPT}} = \frac{V}{(N \times I)} \)
Parallel connection decreases \( Z_{\text{opt}} \)

High \( P_{\text{OUT}} \) → Low \( Z_{\text{opt}} \)

Needs impedance transformation: lumped lines, Wilkinson, ...

High insertion loss ❌
Small bandwidth
Large die area
**Series Power-Combining & Stacks**

Parallel connections: \( I_{out} = N \times I \)

Series connections: \( V_{out} = N \times V \)

Output power: \( P_{out} = N^2 \times V \times I \)

Load impedance: \( Z_{opt} = V/I \)

Small or zero power-combining losses

Small die area

How do we drive the gates?

Local voltage feedback:
- drives gates, sets voltage distribution

**Design challenge:**
- need uniform RF voltage distribution
- need ~unity RF current gain per element
- ...needed for simultaneous compression of all FETs.

Shifrin et al., 1992 IEEE-IMS; Rodwell et al., U.S. Patent 5,945,879, 1999; Pornpromlikit et al., 2011 CSICS
Sub-\(\lambda/4\) Baluns for **Series** Combining

Balun combiner:
2:1 series connection
each source sees 25 \(\Omega\)
\(\rightarrow\) 4:1 increased \(P_{\text{out}}\)

Standard \(\lambda/4\) balun:
long lines
\(\rightarrow\) high losses \(\times\)
\(\rightarrow\) large die \(\times\)

Sub-\(\lambda/4\) balun:
stub\(\rightarrow\) inductive
tunes transistor \(C_{\text{out}}\) !
short lines\(\rightarrow\) low losses
short lines \(\rightarrow\) small die

Park *et al.*, 2013 CSICS, 2014 IEEE-IMS
2:1 series-connected 86GHz power amplifier

- 20 dB Gain
- 188mW $P_{\text{sat}}$
- 1.96 W/mm
- 32.8% PAE

Teledyne 250 nm InP HBT
2 stages, 1.0 mm$^2$
4:1 series-connected 81GHz power amplifier

17 dB Gain
470 mW $P_{\text{sat}}$
23% PAE
Teledyne 250 nm InP HBT
2 stages, $1.0 \text{ mm}^2$ (incl pads)
Teledyne: 1.9 mW, 585 GHz Power Amplifier
M. Seo et al., Teledyne Scientific: IMS2013

- 12-Stage Common-base
- 2.8 dBm $P_{\text{sat}}$
- $>20$ dB gain up to 620 GHz

What limits output power in sub-mm-wave amplifiers?
Sub-mm-wave PAs: need more current!

3 \( \mu \text{m} \) max emitter length (> 1 THz \( f_{\text{max}} \))
2 mA/\( \mu \text{m} \) max current density
\( I_{\text{max}} = 6 \text{ mA} \)

Maximum 3 Volt p-p output

Load: 3V/6mA = 500 \( \Omega \)

*Combiner cannot provide 500 \( \Omega \) loading*
Multi-finger HBTs: more current, lower $f_{\text{max}}$

More current
→ lower cell load resistance

**Reduced $f_{\text{max}}$, reduced RF gain:**
common-lead inductance → $Z_{12}$
feedback capacitance → $Y_{12}$
phase imbalance between fingers.

**Worse at higher frequencies:**
less tolerant of cell parasitics
less current per cell
higher required load resistance
Can optimum load be reached?

- emitter-collector capacitance
- unequal emitter inductances
Sub-mm-wave transistors: need more current

**InP HBTs:**
- thinner collector → more current
- hotter → improve heat-sinking
- or: longer emitters → thicker base metal

**GaN HEMTs:**
- much higher voltage
- 100+ GHz: large multi-finger FETs not feasible

*Need high current to exploit high voltage.*

**Example:**
- 2mA/μm, 100 μm max gate width, 50 Volts
- 200mA maximum current
- 50 Volts/200mA = 250 Ω load → unrealizable.

*Need more mA/μm or longer fingers*
50-500GHz Wireless
50-500 GHz Wireless Electronics

Mobile communication @ 2Gb/s per user, 1 Tb/s per base station

Requires: large arrays, complex signal processing, high $P_{\text{out}}$, low $F_{\text{min}}$

VLSI beamformers
VLSI equalizers
III-V LNAs & PAs

III-V Transistors may perform well enough even for 1 THz systems.
Talk is 40 min plus 10 min for questions...
35-40 slides
Sub-mm-wave PAs: need more current!

<3 μm emitter length for > 1 THz $f_{\text{max}}$

2 mA/μm max current density

$I_{\text{max}} = 6$ mA

Maximum 3 Volt p-p output

Load: $3V/6mA = 500 \, \Omega$

**Combiner cannot provide 500 \, \Omega loading**