12 nm-Gate-Length Ultrathin-Body InGaAs/InAs MOSFETs with $8.3 \times 10^5 I_{ON}/I_{OFF}$

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Late News
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III-V FETs at sub-10-nm nodes?

- III-V channels: low electron effective mass, high velocity, high mobility $\rightarrow$ higher $I_{\text{on}}$ at lower $V_{\text{DD}}$ $\rightarrow$ reducing switching power
- III-V FETs have high leakage current because:
  - Low bandgap $\rightarrow$ larger band-to-band tunneling (BTBT) leakage
  - High permittivity $\rightarrow$ worse electrostatics, large subthreshold leakage
- $I_{\text{off}} < 100\, \text{nA/µm}$ (High performance) and $I_{\text{off}} < 100\, \text{pA/µm}$ (Low power)
- Question: Can III-V MOSFETs scale to sub-10-nm nodes?

<table>
<thead>
<tr>
<th>300K</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InAs</th>
<th>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_e^*$</td>
<td>0.19</td>
<td>0.08</td>
<td>0.063</td>
<td>0.023</td>
<td>0.041</td>
</tr>
<tr>
<td>$\mu_e (\text{cm}^2/\text{V}\cdot\text{s})$</td>
<td>1450</td>
<td>3900</td>
<td>9200</td>
<td>33000</td>
<td>12000</td>
</tr>
<tr>
<td>$\mu_h (\text{cm}^2/\text{V}\cdot\text{s})$</td>
<td>370</td>
<td>1800</td>
<td>400</td>
<td>450</td>
<td>$&lt;300$</td>
</tr>
<tr>
<td>$E_g (\text{eV})$</td>
<td>1.12</td>
<td>0.664</td>
<td>1.424</td>
<td>0.354</td>
<td>0.75</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.7</td>
<td>16.2</td>
<td>12.9</td>
<td>15.2</td>
<td>13.9</td>
</tr>
<tr>
<td>$a (\text{Å})$</td>
<td>5.43</td>
<td>5.66</td>
<td>5.65</td>
<td>6.06</td>
<td>(InP)</td>
</tr>
</tbody>
</table>

Logic industry node | Physical gate length (nm)
--- | ---
16/14 | 20
10 | 17
7 | 14
5 | 12

Ref: 2013 ITRS Roadmap
Record high performance III-V FETs

S. Lee et al., VLSI 2014

$L_g \sim 25 \text{ nm}$

2.7 nm InAs channel (strained)

2.5 nm ZrO$_2$

N+ S/D

Vertical Spacer

1 nm Al$_2$O$_3$N$_y$

$\text{I}_{on} = 500 \mu\text{A/\mu m at I}_{off} = 100 \text{nA/\mu m}$

and $V_D = 0.5 \text{V}$

SS $\sim 72 \text{ mV/dec.}$

SS $\sim 77 \text{ mV/dec.}$

$g_m = 25 \text{ nm}$

$\text{Ion} = 500 \mu\text{A/\mu m}$ at $\text{I}_{off} = 100 \text{nA/\mu m}$

and $V_D = 0.5 \text{V}$

Current Density ($\text{mA/\mu m}$)

Gate Length (nm)

Gate Bias (V)

$V_{DS} = 0.5 \text{ V}$

$I_{on} = 100 \text{nA/\mu m}$
Record low leakage III-V FETs

- Minimum $I_{\text{off}} \approx 60 \, \text{pA/\mu m}$ at $V_D=0.5 \, \text{V}$ for $L_g=30 \, \text{nm}$
- Recessed InP shows 100:1 smaller $I_{\text{off}}$ compared to InGaAs spacers
- BTBT leakage is completely removed $\Rightarrow$ sidewall leakage dominates $I_{\text{off}}$

C. Y. Huang et al., IEDM 2014
TEM images of $L_g \sim 12$ nm devices

- Ti/Pd/Au
- N+InGaAs
- N+InP
- Doping-graded InP
- U.I.D. InP spacer

Cross-section:
- 1 nm InAs
- 5 nm InAlAs U.I.D. spacer
- 2 nm 1E19 cm$^{-2}$ N+InAlAs
- 100 nm InAlAs U.I.D. buffer
- 250 nm 1E17 cm$^{-3}$ P-InAlAs
- 50 nm InAlAs U.I.D. buffer
- S.I. InP substrate

Top View:
- $L_g \sim 12$ nm
- $t_{ch} \sim 2.5$ nm
- (1.5/1 nm InGaAs/InAs)

N+InGaAs

N+InP

InP spacer

Ni

InAlAs Barrier
**$I_D$-$V_G$ and $I_D$-$V_D$ curves of 12nm $L_g$ FETs**

**$L_g$-12nm**

- Ti/Pd/Au
- N+InGaAs
- N+InP
- Doping-graded InP
- U.I.D. InP spacer
- 1nm InAs
- 5nm InAlAs U.I.D. spacer
- 2nm 1E19 cm^{-3} N+InAlAs
- 100nm InAlAs U.I.D. buffer
- 250nm 1E17 cm^{-3} P-InAlAs
- 50nm InAlAs U.I.D buffer
- S.I. InP substrate

$I_{on}$ ~ 1.1 mA/μm

$I_{off}$ ~ 1.3 nA/μm

$I_{on}/I_{off} > 8.3 \cdot 10^5$

- $V_{DS} = 0.1$ to 0.7 V, 0.2 V increment
- $V_{GS} = -0.2$ to 1.2 V, 0.2 V increment

- $R_{on} = 302$ Ohm-μm

- $SS \sim 107.5$ mV at $V_{DS} = 0.5$ V
- $SS \sim 98.6$ mV at $V_{DS} = 0.1$ V

- $V_{GS} = 1.0$ V

- $SS \sim 107.5$ mV at $V_{DS} = 0.5$ V
- $SS \sim 98.6$ mV at $V_{DS} = 0.1$ V
On-state performance

- Slightly higher $G_m$ for a 2.5 nm composite channel than a 4.5 nm InGaAs channel $\rightarrow$ larger gate capacitance.

- A 2.5nm InAs channel with a 12 nm InGaAs spacer shows highest $G_m$ $\rightarrow$ high indium content channel is desirable for UTB III-V FETs.

- InP spacers increase parasitic $R_{S/D}$ to $\sim 260 \ \Omega \cdot \mu m$ $\rightarrow$ InP spacers need further optimization.
Subthreshold characteristics

- A 2.5nm InAs channel with a 12 nm InGaAs spacer shows the lowest SS and DIBL because of the best electrostatics.

- A 5 nm un-doped InP spacer with the atop 8 nm linearly doping-graded InP have shorter effective gate length as compared to 12 nm un-doped InGaAs spacers → worse electrostatics.

- SS~107 mV/dec. and DIBL~260 mV/V for 12 nm devices → FinFETs will cure this.


$\text{I}_{\text{on}}$ and $\text{I}_{\text{off}}$ versus $L_g$

- High In% content channels are required to improve $I_{\text{on}}$, but $I_{\text{off}}$ is relatively large ($\sim 10$ nA/µm).

- InGaAs channels with recessed InP source/drain spacers are required for low leakage FETs.

- A clear tradeoff between on-off performance.
Mobility extraction at $L_g$-25 μm long channel FETs

This work

Freq: 200 kHz
EOT~ 0.9~1 nm
1.5/1 nm InGaAs/InAs

InAs channel

Freq: 200kHz
W/L= 25μm/21 μm
$C_{ox} = 4.2 \, \mu F/cm^2$
EOT= 0.8 nm

Carrier density ($10^{12} \, cm^{-2}$)

Mobility~ 250 cm$^2$/V·s

$V_{DS} = 25 \, mV$ to $50 \, mV$

Mobility~ 280 cm$^2$/V·s

$m^*, R_{S/D}$ more important!
Summary

• We demonstrated a 12nm-$L_g$ ultrathin body III-V MOSFET with well-balanced on-off performance. ($I_{on}/I_{off}> 8.3 \cdot 10^5$)

• The 12nm-$L_g$ FET shows $G_m \sim 1.8 \text{ mS}/\mu\text{m}$ and $SS \sim 107 \text{ mS/dec.}$, and minimum $I_{off} \sim 1.3 \text{ nA/\mu m}$. 

• High indium content channel is required to improve on-state current. *(High performance logic)*

• Thin channels, InGaAs channels, and recessed InP source/drain spacers are the key design features for very low leakage III-V MOSFETs. *(Low Power Logic)*

• III-V MOSFETs are scalable to sub-10-nm technology nodes.
Acknowledgment

Thanks for your attention!
Questions?

- This research was supported by the SRC Non-classical CMOS Research Center (Task 1437.009) and GLOBALFOUNDRIES(Task 2540.001).
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(backup slides follow)
Record low subthreshold swing

SS_{min} \sim 61 \text{ mV/dec.} \quad (\text{at } V_{DS} = 0.1 \text{ V})

SS_{min} \sim 63 \text{ mV/dec.} \quad (\text{at } V_{DS} = 0.5 \text{ V})

Achieved SS \sim 61 \text{ mV/dec.}
Superior high-k dielectrics on III-V channels.

Dielectrics from Gift Chobpattana, Stemmer group, UCSB.
Why InAs channel is better…

- Electron scattering with oxide traps inside conduction band
- Electrons in high In% content channel have less scattering with oxide traps.

N. Taoka et al., IEEE IEDM 2011, 610.

Thicker InP spacer increases $R_{on}$, and degrades $G_m$

- Thinner spacer is desired at source to reduce $R_{S/D}$. 
Doping-graded InP spacer

- Doping-graded InP spacer reduces parasitic source/drain resistance and improves $G_m$.
- Gate leakage limits $I_{\text{off}} \sim 300$ pA/μm.
Fixing source-drain tunneling by corrugation

Transport distance > gate footprint length
Only small capacitance increase
In(Ga)As: low $m^* \rightarrow$ high velocity $\rightarrow$ high current (?)

**Ballistic on-current:**

\[ J = K_1 \cdot \left( 84 \frac{\text{mA}}{\mu\text{m}} \right) \cdot \left( \frac{V_{gs} - V_{th}}{1 \text{ V}} \right)^{3/2} \]

\[ K_1 = \frac{g \cdot (m^*/m_o)^{1/2}}{\left(1 + \left( \frac{c_{dos,o}}{c_{equiv}} \right) \cdot g \cdot (m^*/m_o) \right)^{3/2}} \]

\[ \frac{1}{c_{equiv}} = \frac{T_{ox}}{\varepsilon_{ox}} + \frac{T_{channel}}{2\varepsilon_{semiconductor}} \]

\[ g = \# \text{valleys} \]

More current unless dielectric, and body, are extremely thin.