

# Indium Phosphide Heterobipolar Transistor Technology Beyond 1-THz Bandwidth

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**Abstract**—Recent improvements in the fabrication technology of InGaAs/InP heterobipolar transistors have enabled highly scaled transistors with power gain bandwidths above 1 THz. Limitations of the conventional fabrication process that reduce RF bandwidth have been identified and mitigated, among which are high resistivity base ohmic contacts, resistive base electrodes, excessive emitter end undercut, and insufficient undercut of large-diameter base posts. A novel two-step deposition process for self-aligned metallization of sub-20-nm bases has been developed and demonstrated. In the first step, a metal stack is directly evaporated onto the base semiconductor without any lithographic processing so as to minimize contamination from resist/developer chemistry. The composite metal stack exploits an ultrathin layer of platinum that controllably reacts with base, yielding low contact resistance, as well as a thick refractory diffusion barrier, which permits stable operation at high current densities and elevated temperatures. Further reduction of overall base access resistance is achieved by passivating base and emitter semiconductor surfaces in a combined atomic layer deposition  $\text{Al}_2\text{O}_3$  and plasma-enhanced chemical vapor deposition  $\text{SiN}_x$  sidewall process. This technology enables the deposition of low-sheet-resistivity base electrodes, further improving overall base access resistance and  $f_{\text{max}}$  bandwidth. Additional process enhancements include the significant reduction of device parasitics by scaling base posts and controlling emitter end and base post undercut.

**Index Terms**—InGaAs/InP double heterobipolar transistor (HBT), ohmic contact, refractory, ultralow resistance.

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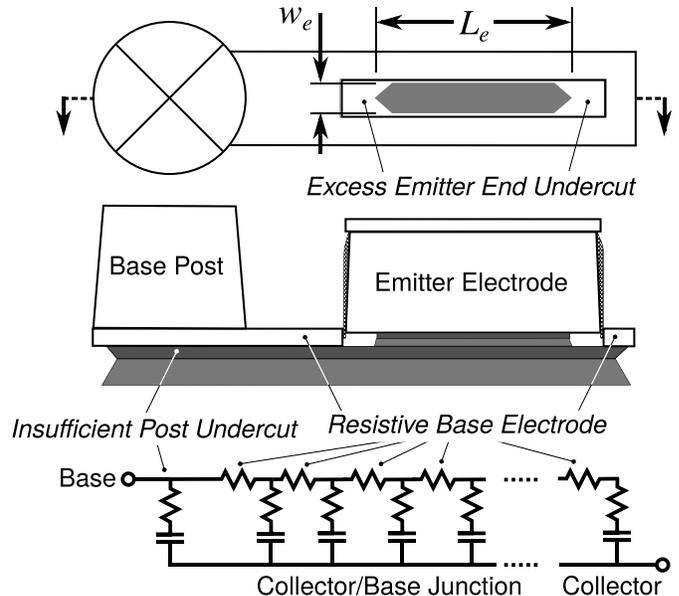


Fig. 1. Schematic layout and cross sections of a triple-mesa HBT showing base metal distributed resistance and excess collector–base junction areas and capacitances associated with the base post and the emitter end undercut. These  $RC$  parasitics reduce the HBT bandwidth.

## I. INTRODUCTION

**H**IGH-BANDWIDTH transistors enable new applications in submillimeter wave ICs and wideband communications [1], [2]. Bipolar transistor cutoff frequencies [3] are increased by scaling, with transit delays  $\tau_b$  and  $\tau_c$  reduced by thinning the epitaxial base and collector  $T_b$  and  $T_c$ , and with an  $RC$  charging delays reduced by shrinking the emitter and the base-collector junction widths  $W_e$  and  $W_c$ , by reducing contact resistivities, and by increasing the emitter current density. Yet, these scaling laws, derived in [3] and [4], address the junction cross-sectional dimensions but neglect capacitances and resistances distributed along the perimeter of the active device. These parasitics become progressively more significant with scaling. In addition, insufficiently scaled base posts dominate overall base/collector capacitance of highly scaled devices. Inadvertent end undercut of emitter stripes will further reduce bandwidths. Fabrication processes must be, therefore, improved to extend the power-gain cutoff frequency  $f_{\text{max}}$  significantly beyond 1 THz [5].

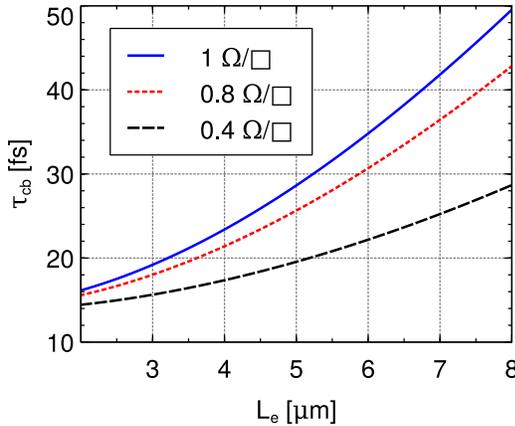


Fig. 2. Finite-element simulations of base–collector charging time  $\tau_{cb}$  associated with  $f_{\max}$  as a function of emitter length  $L_e$  and base metal sheet resistance  $R_{sh}$  for an HBT shown in Fig. 13.

Base ohmic contact fabrication is critical. To attain 1.3 THz  $f_{\max}$ , the base contact resistivity  $\rho_c$  should be less than  $\sim 5 \Omega\mu\text{m}^2$ ; 2 THz requires  $\sim 2.5 \Omega\mu\text{m}^2$  [4]. While contacts to p-type InGaAs with  $\rho_c \sim 1 \Omega\mu\text{m}^2$  have been reported [6], [7], integration into a heterobipolar transistor (HBT) fabrication process remains challenging. The semiconductor surface must be pristine: resist chemistry and electron beam lithography introduce surface contamination, increasing  $\rho_c$ . Furthermore, the contacts must not penetrate significantly into a base  $\sim 10$ – $15$  nm thick. Again, improved fabrication processes must be developed.

## II. MESA HBT BASE–COLLECTOR PARASITICS

Fig. 1 shows the RC parasitics associated with the HBT base–collector junction. These contribute to the base–collector junction  $R_{bb}C_{cb,\text{eff}}$  charging time [3], [8] and thereby decrease  $f_{\max}$ .

Key among the elements distributed along emitter length are the base metal resistance and the excess base–collector junction capacitances in the areas associated with the base post and with the ends of the emitter–base junction. As the device is scaled [3], the base contacts must be narrowed, with  $W_c \propto f_{\max}^{-2}$  [4]. Given some nonzero base metal sheet resistance  $R_{sh}$ , the base metal resistance  $R_{\text{metal}}$  thus increases rapidly with scaling. Unless  $R_{sh}$  is reduced,  $R_{\text{metal}}$  can become the dominant contributor to the total base access resistance  $R_{bb}$ , limiting the feasible  $f_{\max}$ .

$R_{\text{metal}}$  has both a component associated with the region between the base post and the emitter, and a component distributed along the emitter length. The variation of  $R_{\text{metal}}$  with  $L_e$  is, therefore, of the form  $R_0 + k_{r,1}L_e$ . Similarly, the base–collector capacitance  $C_{cb}$  has components associated with the base post and the two undercut ends of the emitter stripe, and a component distributed along the emitter–base junction length. The variation of  $C_{cb}$  with  $L_e$  is, therefore, of the form  $C_0 + k_{c,1}L_e$ . Consequently, the variation of the  $R_{\text{metal}}C_{cb}$  time constant with  $L_e$  is of the form  $\tau_0 + k_{\tau,1}L_e + k_{\tau,2}L_e^2$ . Omitting for brevity an analytic derivation, we present (Fig. 2) the results of a numerical

analysis of  $\tau_{cb} = f_{\tau}/8\pi f_{\max}^2$ , with the HBT represented as a series of incremental elements along the stripe length, each modeled by a hybrid- $\pi$  equivalent circuit, and with increments of  $R_{\text{metal}}$  distributed between HBT elements. The finite conductance of the base electrode reduces  $f_{\max}$  bandwidth by the same amount as an increase of base contact resistivity by  $\Delta\rho_c = W_{bc}/W_b R_{sh} L_e^2/k_c$ , with  $1 < k_c < 2$  depending on the relative composition of  $R_{bb}C_{cb,\text{eff}}$ , the base electrode/semiconductor overlap  $W_{bc}$ , and the width of the base electrode  $W_b$ .

The base post and the undercut ends of the emitter stripe increase the  $C_{cb}$  by the ratio  $(1 + C_0/(k_{c,1}L_e))$ :1, thereby also decreasing  $f_{\tau}$ . If the emitter is made long,  $f_{\max}$  is reduced by the increase in  $R_{\text{metal}}C_{bc}$ ; if the emitter is made short,  $f_{\tau}$  is reduced by the fractional increase in  $C_{cb}$  (Fig. 3).

To obtain high  $f_{\tau}$  and  $f_{\max}$ , the excess capacitance  $C_0$  must be reduced by shrinking the footprint of the base post to enable controlled undercut, by shortening the distance between base post and emitter, and by reducing the etch undercut distance (Fig. 1) at the emitter ends. Reducing  $C_0$  proportionally reduces the minimum  $L_e$  required to maintain a given  $f_{\tau}$  and thus reduces  $R_{\text{metal}}$ . The conductivity of the base electrode metal can be improved by increasing its thickness, adjusting its composition or by increasing its width relative to that of the contact [9], [10].

Extremely low-resistivity base contacts are required. Contamination from resist chemistry or prior process steps can increase  $\rho_c$ ; contamination must be avoided or removed, or the contaminated surface penetrated by the contact metal. Yet, because the base doping near the upper surface is high to enable low  $\rho_c$  [6], but decreases sharply with depth to reduce Auger recombination hence increase  $\beta$  [11], the contacts must not penetrate more than a few nanometers. The contacts must not degrade or deeply interdiffuse into the base during operation at high current densities or at elevated temperatures.

Previously reported HBT fabrication processes [4], [5], [12] used lifted off {Pd, Pt}/Ti/Pd/Au base contacts. In these, the Pd/Pt layer penetrates the base to a depth proportional to the deposited Pd/Pt thickness. If the Pt/Pd layer is too thick,  $\rho_c$  is increased because of deep interdiffusion [13] into the doping-graded base; a very deep penetration will cause base–collector junction failure. If the Pt/Pd layer is too thin, the Ti layer can reach the base semiconductor, forming alloys with As [14] driven by thermal processing and increasing  $\rho_c$ . If the base–emitter spacing is insufficient, lateral Pd/Pt interdiffusion toward the emitter will cause emitter–base junction failure.

Several refractory metals (Mo, W, Ru, Ir) are excellent diffusion barriers [15], can sustain high currents without degradation, are thermally stable, and yield reproducibly low  $\rho_c$  to p-InGaAs [6]. However, we have been unable to directly integrate refractory base metallization into processes similar to [5] and [12]: direct refractory metal evaporation or sputtering requires high energies hence damages photoresist. We have also observed rapid galvanic corrosion of refractory metals if exposed to photoresist stripper (N-Methyl-2-pyrrolidone) or other process chemicals. Although low  $\rho_c$  has been observed in test structures [6], we have observed unexpectedly high contact resistance using similar refractory metal base contacts

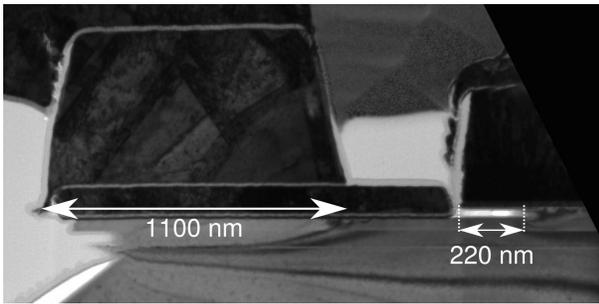


Fig. 3. TEM of an HBT fabricated in a conventional process along the emitter stripe with  $\approx 220$ -nm emitter end undercut and base post with  $\approx 1100$  nm diameter.

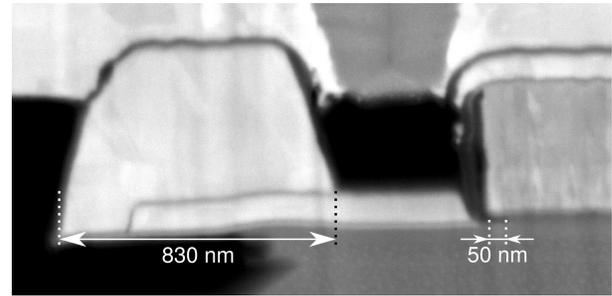


Fig. 4. Cross-sectional SEM of an HBT cut with a focused ion beam along the emitter stripe with  $\approx 50$ -nm emitter end undercut and base post with  $\approx 830$  nm diameter.

in HBTs; because refractory contacts will not getter surface oxides or penetrate surface contaminants, we infer that the high  $\rho_c$  is due to surface contamination from prior processing.

In this paper, we present a novel dual-deposition base metallization process [16] that utilizes a composite stack of reactive, refractory, and highly conductive metal yielding terahertz bandwidth transistors. To reduce surface contamination, lithography before contact metal deposition is avoided. With a 1–2 nm thin, reactive Pt layer to the base contact, we will show that low  $\sim 4 \Omega\mu\text{m}^2$  base contact resistivity can be obtained on a processed HBT. Conformally grown atomic layer deposition (ALD)  $\text{Al}_2\text{O}_3$  is exploited as passivation and protection layer for the emitter–base region. The addition of a base sidewall to the process enables thicker more conductive base metallization with higher gold content. Techniques for reducing parasitic base–collector and base–emitter capacitances are outlined. Finally, we compare HBTs fabricated in the conventional liftoff process to those fabricated with dual-deposited base metal, varying the thickness of the platinum base contact layer.

### III. FABRICATION PROCESS

The HBTs were fabricated in a self-aligned triple-mesa process using electron beam lithography for emitter and base and optical projection lithography for collector, posts, isolation, and interconnect metallization. A composite emitter metal stack Mo/TiW/W 20/250/250 nm is deposited on HBT wafers. Before and after removing the highly doped InGaAs emitter cap in a selective wet etch, plasma-enhanced chemical vapor deposition (PECVD)  $\text{SiN}_x$  sidewalls are formed. Base contacts are deposited around the emitter in a self-aligned process, and the base/collector mesa is formed by selective wet etches. After the deposition of collector contact and posts, the devices are isolated. A blanket PECVD  $\text{SiN}_x$  passivation layer is deposited prior to planarization in a low- $\epsilon$  dielectric benzocyclobutene (BCB). Fabrication is finished by forming interconnect metal wiring on the BCB.

#### A. Emitter End Undercut

Emitter end undercut  $L_{\text{undercut}}$  along fast etch facets degrades RF bandwidths by increasing  $C_{cb, \text{device}}/I_c \propto (1 - 2L_{\text{undercut}}/L_e)^{-1}$ . An anisotropic etch is, therefore, used to thin the emitter semiconductor, enabling shorter etch times and thereby minimizing  $L_{\text{undercut}}$ . Prior to wet-etching

the InP emitter, multiple cycles of UV  $\text{O}_3$  oxidation and subsequent oxide removal in dilute HCl dissolve upper surface layers; the process also removes organic contaminants which might otherwise sink onto the InGaAs base during InP removal. The 30-nm-thick InP emitter is removed in a 5 s wet etch in 4:1  $\text{H}_3\text{PO}_4:\text{HCl}$ , reducing the etch time by 40% in comparison to the conventional fabrication [17], [18]. As a result, the emitter end undercut has been curtailed from 220 nm per end to 50 nm (Fig. 4).

#### B. Dual-Deposited Base Metal

The base metallization is deposited in two steps. To avoid contamination from lithographic processes, the first step is a blanket contact metal deposition: the ohmic contact is formed with an ultrathin reactive layer that controllably penetrates through remaining surface contaminants. Subsequently evaporated thick refractory is exploited as a diffusion barrier. The second step is a patterned liftoff of thick base pad metal providing low base metal sheet resistivity.

Immediately after the InP etch, the sample is cleaned in solvents to remove etch residues. After a short deoxidizing dip in 1:10 HCl:DI, the sample is loaded to an electron beam evaporator. When a pressure below  $6 \times 10^{-7}$  torr has been reached, a blanket metal stack of Pt/Ru/Pt is evaporated onto the sample [Fig. 5(a)]. The initial thin layer of platinum is deposited at very low rates ( $0.1 \text{ \AA s}^{-1}$ ) to improve surface coverage. Among other refractories, Ru has been selected because the sheet resistance of thin e-beam evaporated layers is low and the metal can be dry-etched chemically. The 2-nm-thick upper noble metal platinum layer encapsulates the Ru, protecting metals exposed on the sample surface from galvanic corrosion in process chemicals. This metal stack has a sheet resistance of  $25 \Omega/\square$ ,  $\sim 20:1$  less than the base semiconductor sheet resistance.

After initial metal deposition, a 10-nm  $\text{Al}_2\text{O}_3$  layer is conformally deposited by ALD [Fig. 5(b)]. The  $\text{Al}_2\text{O}_3$  protects the exposed base regions between the base metallization and the emitter semiconductor from damage in subsequent processing and passivates the emitter–base surface. A 20-nm-thick PECVD  $\text{SiN}_x$  sidewall is formed [Fig. 5(c)], enabling the removal of  $\text{Al}_2\text{O}_3$  in the field in a wet etch either in 2.38% TMAH (etch rate  $3 \text{ nm min}^{-1}$ ) or 1:50 BHF:DI (etch rate  $\approx 30 \text{ nm min}^{-1}$ ). The sidewall also increases the spacing between by base metal accidentally deposited on the emitter

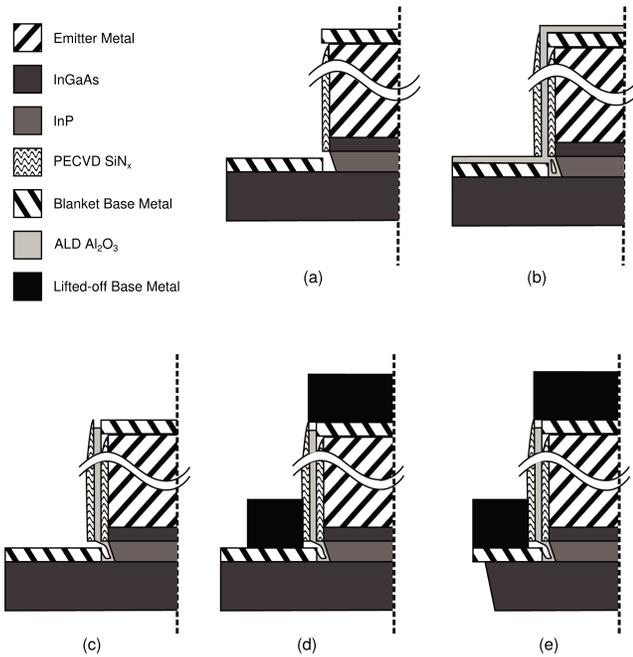


Fig. 5. Dual-deposited base metallization process. (a) Composite blanket base metal deposition. (b) Conformal  $\text{Al}_2\text{O}_3$  atomic layer deposition, formation of  $\text{SiN}_x$  sidewall. (c) Wet etch of  $\text{Al}_2\text{O}_3$  in the field. (d) Lift-off of base metal pads. (e) Dry etch of blanket base metal wet etch of base/collector mesa.

sidewalls and the emitter metal, reducing the base-emitter capacitance  $C_{be}$  and preventing short-circuits.

Base pad metal, Ti/Au 5/95 nm, is then lifted off in a standard, bilayer electron beam lithography process [Fig. 5(d)]. Prior to metal deposition, resist residues are removed in an oxygen plasma (20 s, 100 W, 300 mtorr): the presence of the base contact metal diminishes the risk of damaging the base semiconductor. The sheet resistance of the full composite base metal electrode is  $\approx 0.4 \Omega/\square$ , approximately half the sheet resistance of the conventional lifted off base metal stacks [12]. After depositing base posts, emitter/base regions are protected using electron beam lithography with 1- $\mu\text{m}$  thick resist (microposit maN-2410). A  $\text{Cl}_2/\text{O}_2$  dry etch (20/5 sccm, 0.67 Pa, 400 W RF, 100 W ICP, 40 s) etch removes the topmost blanket base layers Pt/Ru [19]. Without breaking vacuum, a short sputtering etch in  $\text{Ar}/\text{Cl}_2$  (45/5 sccm, 1 Pa, 600 W RF, 150 W ICP, 20 s) removes nonvolatile etch products from the field. The addition of  $\text{Cl}_2$  enables removal of etch redeposits on the resist sidewalls in subsequent wet etches. However, the sputtering etch is nonselective to InGaAs, removing  $\approx 25$  nm of the base/collector junction. The wet-etch times of the base/collector mesa are adjusted accordingly [Fig. 5(e)]. Plasma-damaged resist residues collapse onto the emitter and the base post during stripping and, are therefore, removed prior to deposition of interconnect metals in a short Ar sputter (20 s, 300 W ICP, 50 W RF, 20 sccm, 1 Pa).

### C. Base Post Scaling

Charging delays due to the parasitic base-collector capacitance of the base post  $C_{cb, BP} \propto A_{BP} = \pi(d_{BP}/2)^2$  become dominant on small footprint transistors when the post has been undercut insufficiently, limiting RF bandwidth. The base posts

TABLE I  
EPITAXIAL STRUCTURE DESIGN

T (nm)	Material	Doping ( $\text{cm}^{-3}$ )	Description
10	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$8 \times 10^{19} : \text{Si}$	Emitter Cap
15	InP	$5 \times 10^{19} : \text{Si}$	Emitter
15	InP	$5 \times 10^{18} : \text{Si}$	Emitter
20	$\text{In}_{\approx 0.5}\text{Ga}_{\approx 0.5}\text{As}$	$11 \cdot 7 \times 10^{19} : \text{C}$	Base
13.5	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$5 \times 10^{16} : \text{Si}$	Setback
16.5	InGaAs/InAlAs	$5 \times 10^{16} : \text{Si}$	B-C Grade
3	InP	$3.6 \times 10^{18} : \text{Si}$	Pulse Doping
67	InP	$5 \times 10^{16} : \text{Si}$	Drift Collector
7.5	InP	$2 \times 10^{19} : \text{Si}$	Sub-Collector
7.5	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$4 \times 10^{19} : \text{Si}$	Sub-Collector
300	InP	$1 \times 10^{19} : \text{Si}$	Sub-Collector
3.5	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	NID	Etch Stop
$\approx 625\text{k}$	SI InP		Substrate

have, therefore, been reduced from  $\approx 1.1 \mu\text{m}$  in [12] to 830 nm in diameter, reducing their footprint by 40%. The lithographic masks used for isolating transistors has been adjusted to almost completely undercut the base posts (Fig. 4).

## IV. EXPERIMENTAL RESULTS

A wafer HBT64 has been grown in a solid source molecular beam epitaxy reactor on a 4 in InP substrate by IQE (Table I). The surface doping of the 20-nm-thick base has been increased to  $11 \times 10^{19} \text{cm}^{-3}$ , reducing  $\rho_c$  [6] and generating a 90-meV conduction band slope. The 100-nm-thick collector consists of a 13.5-nm setback, a 16.5-nm chirped superlattice InGaAs/InAlAs grade, a pulse-doping layer, and a 67-nm drift collector region.

Three samples have been fabricated from the same wafer: 64A has lifted off base metalization of 2.5/12/17/70 nm Pt/Ti/Pd/Au with larger (1.1  $\mu\text{m}$ ) diameter base posts, and was fabricated using the process flow of [12]. The enhanced fabrication process described in Section III has been executed on samples 64C and 64J, altering only the thickness of the initial reactive Pt base contact layer 1 nm on 64C, respectively, 2 nm on 64J.

Extractions from transmission line model (TLM) measurements indicate base contact resistivity of  $38 \Omega\mu\text{m}^2$  and base sheet resistance of  $850 \Omega/\square$  on 64A. The base contact resistivity on 64J and 64C not be determined from TLM measurements due to inadvertent process damage to the TLM structures. Collector contact resistivity is  $\approx 15 \Omega\mu\text{m}^2$  among all samples.

FIB/transmission electron micrograph (TEM) analysis reveals the interdiffusion depth of base metal with InGaAs:  $\approx 6$  nm on 64A and 64J,  $\approx 3.1$  nm on 64C. Furthermore, damage to exposed semiconductor between emitter and base metal is observed on 64A, but not on 64J and 64C (Fig. 6).

A total emitter access resistivity  $\rho_{em} \approx 3 \Omega\mu\text{m}^2$  was extracted from RF data; this includes the contribution from electron degeneracy [4]. HBTs with emitter area  $A_e = 2.9 \times 0.2 \mu\text{m}^2$  show a peak dc gain  $\beta = 15$ . Figs. 8 and 9 show common-emitter and Gummel characteristics of the same transistor. The common-emitter breakdown

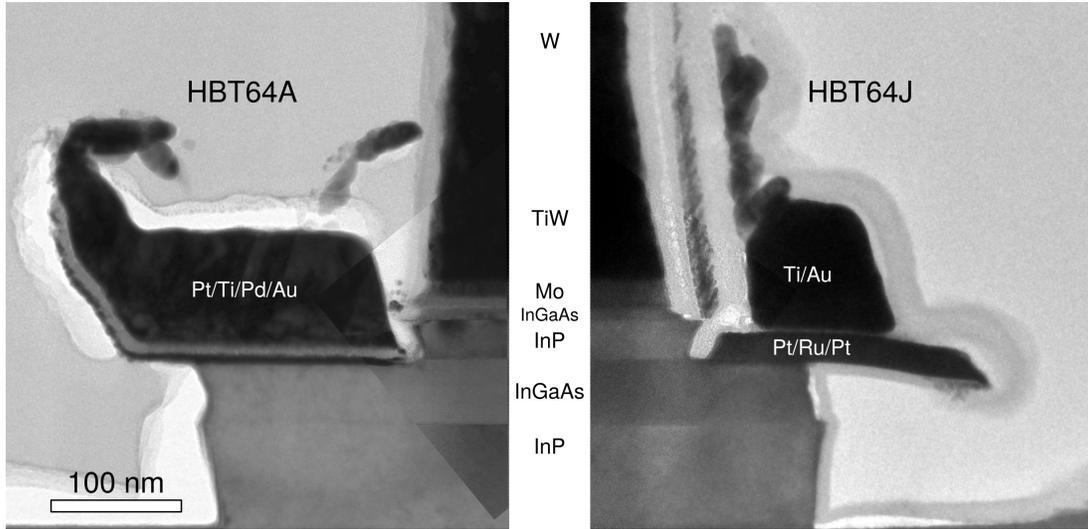


Fig. 6. Composite TEMs of the emitter/base region for devices fabricated in the conventional (left) and the dual-deposition (right) base metallization process.

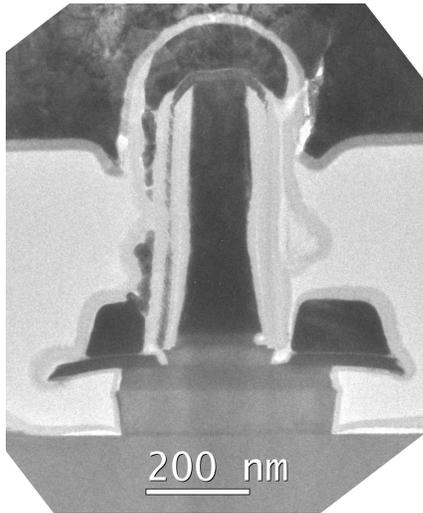


Fig. 7. TEM of a fabricated device on sample 64J. Emitter junction width  $W_e = 200$  nm, single-sided base contact width  $w_{bm} = 80$  nm, emitter–base contact spacing  $w_{Gap} \approx 15$  nm.

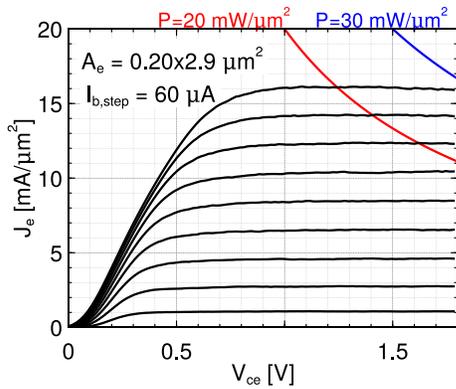


Fig. 8. Common-emitter characteristics for an HBT on sample 64J with  $180\text{-nm} \times 2.9\text{-}\mu\text{m}$  emitter junction area.

voltage is  $BV_{CEO} = 4.1$  V at  $J_c = 10$  kA/cm<sup>2</sup> (corresponding to 0.6% of the emitter current density at which peak  $f_{max}$  is measured) and 3.2 V at 1 kA/cm<sup>2</sup> (Fig. 10).

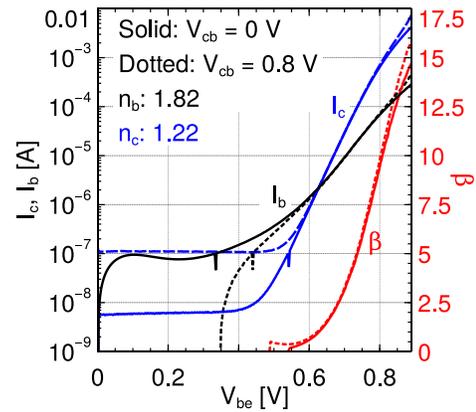


Fig. 9. Gummel characteristics for an HBT on sample 64J with  $200\text{-nm} \times 2.9\text{-}\mu\text{m}$  emitter junction area.

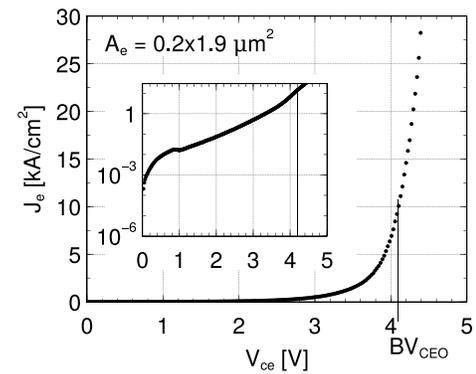


Fig. 10. Breakdown characteristics for an HBT on sample 64J with  $200\text{-nm} \times 1.9\text{-}\mu\text{m}$  emitter junction area.

The RF measurements from 0.5–67 GHz were carried out using an Agilent E8361A PNA using the calibration and pad deembedding procedure of [20]. The best extractable RF performance has been observed on sample 64J for a transistor with  $A_e = 2.9 \times 0.2 \mu\text{m}^2$  and a single-sided base contact width  $W_{bc} = 85$  nm. (Fig. 7): Fig. 11 shows the peak  $f_{max}$

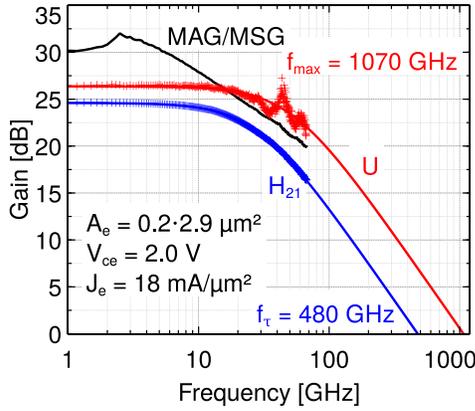


Fig. 11. Measured RF gains for an HBT on sample 64J with  $200\text{-nm} \times 2.9\text{-}\mu\text{m}$  emitter junction area and  $400\text{-nm}$  base-collector mesa width using off-wafer LRRM structures and on-wafer pad open/short deembedding. Single-pole fit to the measured data yields  $f_\tau$  480 GHz,  $f_{\max}$  1070 GHz.

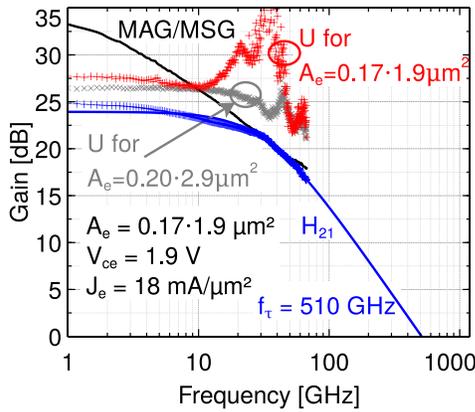


Fig. 12. Variation of  $f_\tau$ ,  $f_{\max}$ , and  $C_{cb}$  with  $J_e$  at  $V_{ce} = 2\text{ V}$  for an HBT on sample 64J with  $200\text{-nm} \times 2.9\text{-}\mu\text{m}$  emitter junction area and  $310\text{-nm}$  base-collector mesa width.

performance at  $I_c = 9.52\text{ mA}$ ,  $V_{ce} = 2.0\text{ V}$ ,  $V_{cb} = 1.13\text{ V}$ , and  $J_e = 18\text{ mA}/\mu\text{m}^2$ . Fig. 12 shows variation of RF bandwidths and  $C_{cb}$  with  $J_e$ . Despite a wider emitter junction ( $200\text{ nm}$  versus  $130\text{ nm}$ ) and a longer emitter stripe ( $2.9\text{ }\mu\text{m}$  versus  $2\text{ }\mu\text{m}$ ) the peak  $1070\text{ GHz}$   $f_{\max}$  is 93% of that reported in [5]; unfortunately, we are unable to obtain a reliable measurement of  $f_{\max}$  for smaller geometry HBTs on the present samples. A small signal equivalent hybrid- $\pi$  circuit has been developed from RF measurements (Fig. 13) showing good agreement between measured and simulated S parameters (Fig. 14). A device with identical emitter dimensions, but reduced base contact width  $W_{bc} = 30\text{ nm}$  exhibits with peak  $f_\tau$  performance at  $f_{\max} = 850\text{ GHz}$ ,  $f_\tau = 550\text{ GHz}$ .

For the most highly scaled ( $170\text{ nm}$   $W_e$ ,  $\sim 350\text{ nm}$   $W_{bc}$ ) devices on sample 64J, the transistor  $\Re\{Y_{12}\}$  becomes very small, approaching the level of errors in the calibrated S-parameter measurements. For these devices, the unilateral gain  $U$  and hence  $f_{\max}$  cannot be reliably determined. Before roll-off, however, the measured unilateral gain of small footprint devices exceeds the gain of larger devices (Fig. 15) while the current gain cutoff frequency is also increased.

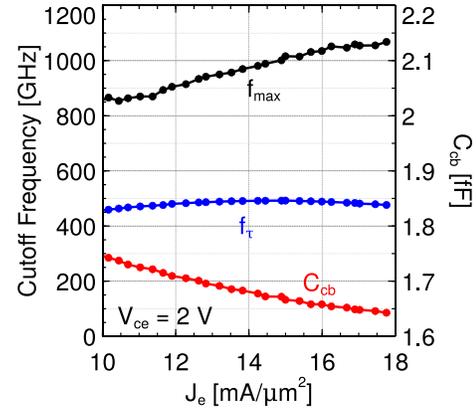


Fig. 13. Hybrid- $\pi$  equivalent circuit for the HBT of Fig. 11 at peak  $f_{\max}$  performance.

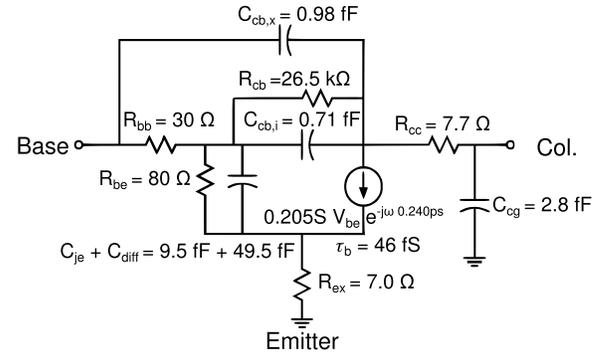


Fig. 14. Comparison of (solid line) measured S-parameters of Fig. 11 and (x) simulated S-parameters from the model of Fig. 13 from  $0.5\text{--}67\text{ GHz}$ .

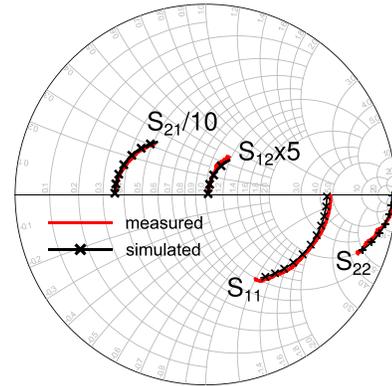


Fig. 15. Measured RF gains for an HBT on sample 64J with  $170\text{-nm} \times 1.9\text{-}\mu\text{m}$  emitter junction area and  $370\text{-nm}$  base-collector mesa width. Unilateral gain of transistor in Fig. 11 plotted for reference. Single-pole fit to the measured data yields  $f_\tau$  510 GHz.

Finite-element modeling suggests that HBTs with  $170\text{ nm}$   $W_e$  should have larger  $f_{\max}$  than HBTs having  $200\text{ nm}$   $W_e$ .

Peak RF performance on 64C with  $f_{\max} = 910\text{ GHz}$ ,  $f_\tau = 480\text{ GHz}$  has been measured on a device with  $A_e = 2.9 \times 0.22\text{ }\mu\text{m}^2$  and a single-sided base contact width  $w_{bc} = 170\text{ nm}$ . The best RF performance obtained on sample 64A is  $f_{\max} = 667\text{ GHz}$ ,  $f_\tau = 476\text{ GHz}$  on a transistor with  $A_e = 2.9 \times 0.22\text{ }\mu\text{m}^2$  and a single-sided base contact width  $w_{bc} = 320\text{ nm}$ .

## V. DISCUSSION

Estimations from RF measurements place the base contact resistivity at  $8 \Omega\mu\text{m}^2$  on 64C (1 nm Pt base contact) and  $4 \Omega\mu\text{m}^2$  on 64J (2 nm Pt base contact), much lower than the extracted contact resistivity  $\approx 40 \Omega\mu\text{m}^2$  on 64A. The high  $f_{\text{max}}$  observed on 64J is a direct consequence of this low contact resistivity. Despite identical surface treatment prior to base metal deposition on all samples, the dual metallization process has yielded contact resistivity improved by an order of magnitude. We therefore assert that lithographic processes of the conventional fabrication technology have introduced contaminants to the base surface, limiting the minimum attainable contact resistance and subsequently  $f_{\text{max}}$ . The power gain bandwidth is further diminished on 64A by high base metal sheet resistance ( $0.8 \Omega/\square$ ), whereas the composition and thickness of the base electrodes on 64C and 64J yielded sufficiently low sheet resistance ( $0.4 \Omega/\square$ ).

We note that the surface coverage of 1 nm Pt deposited by electron beam evaporation is incomplete. Better surface coverage and consequently better ohmics are attained for 2 nm Pt. At interdiffusion depths roughly three times the Pt thickness, this technology remains usable for 12 nm thick bases.

Alternate on-wafer calibration structures [5], [21] are necessary to accurately determine  $f_{\text{max}}$  in the future. Better dimensional control over emitter metal width and shape, more conductive base metallization and advanced surface cleaning techniques will further enhance RF bandwidth, to values consistent with the scaling roadmap of [4].

## VI. CONCLUSION

A novel fabrication technology InP HBTs has been presented. Dual-deposition base metallization yields low resistance contacts of thin bases with highly conductive electrodes. Reduction of parasitics by precisely controlled emitter and base post undercut as well as base post scaling has enabled further increases of the RF bandwidth. The process has been executed on two samples, yielding devices with  $f_{\text{max}}$  in excess of 1 THz at  $f_{\tau} = 480$  GHz while maintaining breakdown voltage  $\text{BV}_{\text{CEO}} = 4.1$  V. Other devices exhibit  $f_{\tau}$  of 550 GHz at  $f_{\text{max}}$  of 850 GHz. In comparison with conventional fabrication, the improved technology has demonstrated clear advantages.

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Authors' photographs and biographies not available at the time of publication.