Extremely high simulated ballistic currents in triple-heterojunction tunnel transistors

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Future VLSI devices will require low CV_DD/2 switching energy, large on-currents (IoN), and small off-currents (I_OFF). Low switching energy requires a low supply voltage V_DD, yet reducing V_DD typically increases I_OFF and reduces the IoN/I_OFF ratio. Though tunnel FETs (TFETs) have steep subthreshold swings and can operate at a low V_DD, yet their I_ON is limited by low tunneling probability. Even with a GaSb/InAs heterojunction (HJ), given a 2nm-thick-channel (001)-confined TFET, [100] transport, and assuming V_DD=0.3V and I_OFF=10^3 A/m, the peak tunneling probability is <3% (fig.1a) and I_ON is only 24 A/m (fig.1b) [1]. This low I_ON will result in large CV_DD delay and slow logic operation.

Techniques to increase I_ON include graded AlSb/AlGaSb source HJ (see fig2) and allows the tunnel barrier to be further thinned.

But, if the InAs layer is thinned below 3.5 nm and the PN junction field increases, the tunnel barrier thins, and the tunneling transmission probability and delay increases. A resonant state, both increasing on the P, OFF state (fig. 3a) and allows the tunnel barrier to be further thinned. Table 1 lists the corresponding tunneling distances. At 15nm LG, the channel-HJ TFET has a better ON/OFF ratio and better subthreshold swing than the source-HJ TFET, in part due to smaller source/drain tunneling from a smaller valence-band barrier and a larger channel electron effective mass. At both 15nm and 30nm LG, the triple-HJ TFET has the highest I_ON of all designs, this due to the strongest junction electric field and smallest tunneling distance. A graded source HJ further increases the junction electric field and decreases the tunnel barrier width; its design includes an AlSb source (N_A=3×10^19 cm^-3), an 1.6 nm Ga0.5Al0.5Sb (N_A=6×10^17 cm^-2) grade layer, an 2.8 nm GaSb (N_A=5×10^19 cm^-2) P-junction layer, an 3.3 nm InAs undoped N-junction layer, and an undoped In0.70Al0.21As0.70Sb0.21 channel. It achieves an 800A/m ballistic I_ON at 30nm LG and 460A/m at 15 nm.

We avoid placing the source resonant state above the source valence band or the channel resonant state below the channel conduction band, as this would increase I_OFF by combined tunneling and thermionic emission. Nevertheless, in the off-state, evanescent states in the source and channel wells couple (fig. 4a) to states across the barrier; these states will increase I_OFF through phonon-assisted tunneling, an effect not modeled here, but modeled in [2]. Source thermalization with 5meV broadening reduces I_ON to 350A/m at 15nm LG, but does not significantly reduce I_OFF at 30nm LG. We will report a more detailed analysis of the mechanisms controlling I_OFF.

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Fig. 1. Band diagram (a) and transmission probability (b) of a (001)-confined tunnel FET in ON-state bias. The transport is along [100]. The maximum transmission probability is 2.5%.

Fig. 2. Band diagram (a) and transmission probability (b) of a TFET with an InAs/InAlAsSb channel heterojunction and (110) confinement. Transport is along [110]. $E_Fs$ and $E_{Fd}$ refer to source and drain Fermi levels.

Fig. 3. Device cross-section of a TFET with a GaSb/InAs tunnel heterojunction (a), a InAs/InAlAsSb channel heterojunction (b), a AlSb/GaSb source heterojunction (c), and with both source and channel heterojunctions (d). In (d), the source heterojunction can be graded.

Fig. 4. Local density of states in OFF-state (a) and on-state bias (b) of a (110)-confined triple-HJ TFET. Resonant states are circled.

Fig. 5. Band diagram (a) and transmission probability (b) of a (110)-confined GaSb/InAs TFET and a triple-HJ TFET with source grading. Transport is along [110].

Fig. 6. Transfer characteristics of (110) confined TFETs for $L_c=15$nm (a) and $L_c=30$nm (b). Transport is along [110].

Table 1: $I_{ON}$ and tunneling distance for (110) GaSb/InAs HJ, source HJ, channel HJ, and triple-HJ TFETs. These are compared to a reference (001)-confined GaSb/InAs design.