The base-collector junction capacitance \( C_{bc} \) is a key factor limiting HBT’s high frequency performance. To reduce \( C_{bc} \), we report an HBT structure with a collector pedestal under the HBT’s intrinsic region by using selective ion implantation and MBE regrowth (Fig.1), the first such structure reported in III-V HBTs. It is designed so that the depleted collector thickness in HBT’s extrinsic region is much larger than the depleted collector thickness in HBT’s intrinsic region, and therefore substantially reducing the extrinsic base-collector capacitance. Although \( C_{bc} \) can also be reduced by forming a narrow N+ subcollector stripe lying under the emitter\(^1\), such structures can have large collector access resistance \( R_c \) arising from long, narrow N+ layer. The collector pedestal structure, however, does not significantly increase collector access resistance relative to a standard mesa structure, and is consequently the approach most widely employed in Si/SiGe technology. We had earlier reported collector pedestal HBTs with low leakage and good DC characteristics \(^2\); here we report devices with the expected large reduction in \( C_{bc} \).

Fig. 2 shows the fabrication process. The subcollector template was grown by MBE and consisted of a 2000Å n+ InP subcollector layer, a 50Å InGaAs n+ subcollector contact layer, a 1800Å undoped InP collector pedestal layer, and a 500Å undoped InGaAs sacrificial cap layer. After the growth of this template, tungsten alignment marks were formed and a 0.8µm thick PECVD SiN implant mask was defined. The implant window width was varied in a series of devices to study the effectiveness of the selectively implanted collector pedestal for \( C_{bc} \) reduction. \(^{28}\)Si was then implanted at 110KeV with a dose of \( 8 \times 10^{13} \text{cm}^{-2} \) at 200°C and annealed at 750°C for 10 sec for dopant activation. The InGaAs sacrificial layer was then removed and the p-type delta-doping layer, collector drift layer, base, and emitter were regrown by MBE (Table1). Due to the n-type charge accumulation at the regrowth interface between InP layers, for HBTs directly regrown on collector pedestal layers, the extrinsic base-collector region could not be fully depleted until a high reverse bias voltage higher (>2V) was applied\(^3\)\(^4\). This was successfully corrected by inserting 40Å carbon-doped InGaAs delta-doping layer on the regrowth interface, which led the 1800Å collector pedestal layer fully depleted at a reverse bias less than 0.5V (Fig. 3). As a result the collector depletion region above the collector pedestal was 900 Å thick, while outside the pedestal the depletion layer was 2700 Å thick. After MBE regrowth, triple-mesa HBTs were fabricated using optical lithography and wet etching.

Fig. 4(a) shows the Gummel characteristics of a 0.4×7 µm\(^2\) device, measured with 0.3V collector-base reverse bias so that the base-collector junction leakage \( I_{cbo} \) could be observed. Fig. 4(a) indicates \( I_{cbo}=0.5 \text{nA} \). Fig. 4(b) shows the common-emitter I-V curves of the same device, measured from 0-10 mA/µm\(^2\) current density. The breakdown voltage \( V_{CEO} \) is 5.5V, which is exceptionally high for a device with 900Å collector. This high breakdown can be attributed to the buried collector pedestal structure which eliminates the high surface state density on the N+ collector mesa sidewalls, normally being the dominant factor limiting device’s breakdown voltage. The microwave 2-port parameters were characterized and the total base-collector capacitance \( C_{bc} \) determined from \( Y_{12} \). Fig. 5 shows the measured \( C_{bc} \) as a function of \( J_c \) at \( V_{CEO}=0.3V \) for devices with different collector pedestal width. As expected, \( C_{bc} \) decreased as the collector pedestal width became smaller. Compared to the HBT with 2.1µm wide collector pedestal under the base mesa, which was equivalent to a conventional mesa HBT with 900Å collector, the HBT with 1.0µm wide collector pedestal achieved nearly 40% \( C_{bc} \) reduction. From the variation of \( C_{bc} \) with pedestal width, it is determined that the pedestal is 300 nm wider than the implant mask width.

In conclusion, a new InP HBT structure with a selectively implanted collector pedestal has been demonstrated. The present results exhibit excellent DC characteristics including extremely low \( I_{cbo} \) and high breakdown voltage \( V_{CEO} \). Total base-collector capacitance was successfully reduced by 40%.


Fig. 1 Schematic cross-section of the HBT with selectively implanted collector pedestal.

Fig. 2 Fabrication steps: (a) implant window definition and Si ion implant, (b) implant mask removal and HT annealing, (c) HBT structure regrowth, (d) triple-mesa HBT fabrication.

Fig. 3 C-V measurements across the base-collector junction of large-area test devices with and without p-type InGaAs compensating layer

Fig. 4 (a) Gummel plots and (b) Common Emitter characteristics of an HBT with 0.4×7 µm² emitter

Fig. 5 C_{BC} dependence on J_C for devices with different collector pedestal width

Table 1 Parameters of the HBT epitaxial layers grown above the collector pedestal layer.