Selectively implanted subcollector DHBTs

Dept. of Electrical and Computer Engineering, University of California, Santa Barbara, CA

M. Urteaga, K. Shinohara, B. Brar
Rockwell Scientific Company, Thousand Oaks, CA

This work was supported under the DARPA-TFAST program
<table>
<thead>
<tr>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Motivation</td>
</tr>
<tr>
<td>• InP HBTs: solutions towards the future</td>
</tr>
</tbody>
</table>
  1. *Implanted Subcollector HBTs*  
  2. *Pedestal-Subcollector HBTs* |
<p>| • Conclusions |</p>
<table>
<thead>
<tr>
<th>Why are fast transistors required?</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fiber Optic Communication Systems</strong></td>
</tr>
<tr>
<td>40 Gb/s commercially available</td>
</tr>
<tr>
<td>80 and 160 Gb/s(?) long haul links</td>
</tr>
<tr>
<td><strong>High speed Instrumentation</strong></td>
</tr>
<tr>
<td>mixed-signal ICs with large dynamic range</td>
</tr>
<tr>
<td><strong>mm-Wave Wireless Transmission</strong></td>
</tr>
<tr>
<td>high frequency communication links,</td>
</tr>
<tr>
<td>atmospheric sensing, military and commercial radar</td>
</tr>
</tbody>
</table>
### Some common figures of merit

**$f_t$** is the unity current gain frequency

$$\frac{1}{2\pi f_t} = \tau_{\text{base}} + \tau_{\text{collector}} + RC_s...$$

**$f_{\text{max}}$** is the power gain cut-off frequency

$$f_{\text{max}} \approx \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cb}}}$$

---

Digital delay not well correlated with $\tau_F$

(V_{LOGIC}/I_c) (C_{cb}) is a major delay

$$\Rightarrow \frac{C_{cb}}{I_c} \propto \left( \frac{A_{\text{COLLECTOR}}}{A_{\text{EMITTER}}} \right) T_c$$

Collector Base capacitance must be reduced
**InP vs Si/SiGe HBTs**

*InP system has inherent material advantages over Si/SiGe*

- 20x lower base sheet resistance,
- 5x higher electron velocity,
- 4x higher breakdown—at same $f_t$.

*but...*

*today's SiGe HBTs are fast catching up due to 5x smaller scaling and offer much higher levels of integration due to the Si platform*

### Scaling Laws for HBTs

- *Reduce vertical dimensions to decrease transit times*
- *Reduce lateral dimensions to decrease RC time constants*
- *Increase current density to decrease charging time*
InP HBTs today... and tomorrow?

### Key Challenges for InP HBTs

- Scaling of collector-base junction
- Planar, manufacturable process for high levels of integration
- Narrow base-emitter junction formation and also low $R_{ex}$
- Parasitic base collector capacitance under base contacts
- Base ohmic transfer length limits collector scaling
- Non-planar device

A Radical approach is necessary
The end goal: SiGe-like highly scaled InP HBT

Objectives:
- Extreme parasitic reduction: speed
- Planar Geometry: yield

Regrown submicron emitter
- submicron emitter scaling: speed
- large emitter contact: low $R_{ex}$, speed

Extrinsic base
- thick extrinsic base: low $R_{bb}$, speed

Pedestal collector
- submicron collector scaling: speed
- One sided collector: integration

Isolated subcollector
- large base pad: yield
- zero base pad capacitance: speed

MODULE 1

MODULE 2
The end goal: SiGe-like highly scaled InP HBT

Isolated subcollector
zero base pad capacitance: speed
Module 1: Access Pad Capacitance in InP HBTs

- $C_{cb, \text{pad}} \approx 30\%$ of overall $C_{cb}$
- Increasingly significant for short emitter lengths

IMPORTANT FOR FAST, LOW POWER LOGIC
**Implanted subcollector InP DHBTs**

**Approach**
- Selectively implanted N++ subcollector
- Growth of drift collector, base & emitter
- Device formation

**Interface charge compensation**
- N++ charge present on exposed InP surface
- Fe implant suppresses interface charge
Implanted subcollector DHBT with Fe: The Process

1. Shallow Fe implant
2. Semi Insulating InP substrate
3. Anneal
4. Si subcollector implant
5. Fe implanted region
6. Semi Insulating InP substrate
7. Anneal and MBE growth
8. Device formation
9. Emitter
10. Base
11. Collector
12. N++ subcollector
13. Semi Insulating InP substrate
**Implanted subcollector DHBTs with Fe – DC results**

DC characteristics - Gain, Ideality factors, Leakage currents...are similar to fully epitaxial device

**Common Emitter curves**

- $A_{je} = 0.65 \times 4.3 \ \mu m^2$
- $I_{b \ step} = 100 \ \mu A$
- $V_{ce} = 0 \ V$

**Gummel characteristics**

- $V_{CB} = 0.3 \ V$
- $I_c \eta = 1.1$
- $I_b \eta = 1.5$
- 60 pA

Peak $\beta \approx 35$, $BV_{CBO} = 5.31 \text{V } (I_c=50 \ \mu A)$

Base (from TLM) : $R_{\text{sheet}} = 1050 \ \Omega / \text{sq}$, $R_{\text{cont}} = 50 \ \Omega \cdot \mu m^2$

Collector (from TLM) : $R_{\text{sheet}} \sim 25.0 \ \Omega / \text{sq}$, $R_{\text{cont}} \sim 110 \ \Omega \cdot \mu m$
**Implanted subcollector DHBTs with Fe – RF results**

- $f_t = 363$ GHz, $f_{max} = 410$ GHz

- **Gains (dB)**
  - $A_{jbe} = 0.65 \times 4.3$ $\mu$m$^2$
  - $I_c = 19.1$ mA, $V_{ce} = 1.97$ V
  - $J_e = 6.8$ mA/$\mu$m$^2$

- **Frequency (Hz)**
  - $f_t = 363$ GHz, $f_{max} = 410$ GHz

- $C_{cb}$ reduced by $\sim 25\%$
Module 2: Submicron collector scaling

Pedestal collector submicron collector scaling: speed

Collector contact
$N^{++}$ pedestal

Isolated subcollector
large base pad: yield
zero base pad capacitance: speed
An elegant approach to collector scaling
The triple implanted subcollector-pedestal HBT

Approach

1. deep N$^{++}$ InP subcollector by selective Si implant
   $\rightarrow$ isolate base pad (Module 1)

2. SI layer $\sim$0.2$\mu$m, by Fe implant
   $\rightarrow$ decrease extrinsic $C_{cb}$

3. Second Si implant creates N$^{++}$ pedestal for current flow

4. Growth of drift collector, base & emitter and device formation

N. Parthasarathy et al., Electron Device Letters, Vol. 27(5), May 06
An elegant approach to collector scaling
The triple implanted subcollector-pedestal HBT

Advantages over standard mesa device

1. Collector Base junction can be independently scaled
2. Pad capacitance eliminated
3. Increased Breakdown voltages

More benefits....

4. Highly planar, fully implanted process, no regrowth required → manufacturability
5. Implants before growth endless variations in subcollector-pedestal layers without compromising device planarity
6. Fe compensates interface charge → reliability and repeatability
RF performance: fully implanted subcollector-pedestal HBT

$f_t = 352 \text{ GHz, } f_{\text{max}} = 403 \text{ GHz}$

$C_{cb}$ reduced by $\sim 50\%$

N. Parthasarathy et al., Electron Device Letters, May 06
**Conclusion**

*Implanted collector InP HBTs at 500 nm scaling generation* ~ 400 GHz $f_t$ & $f_{max}$

- Implanted subcollector DHBTs – eliminate pad capacitance
- Implanted pedestal-subcollector DHBTs – independent collector scaling

**InP HBT future: 125 nm scaling generation with implanted pedestal-subcollectors**

~1 THz $f_t$ & $f_{max}$, 400 GHz digital latches & 600 GHz amplifiers?

**Applications**

- 160+ Gb/s fiber ICs, 300 GHz MMICs for communications, radar, & imaging
- & applications unforeseen & unanticipated

“The principal applications of any sufficiently new and innovative technology always have been – and will continue to be – applications created by that technology.”

-Kroemer’s Lemma of New Technology