Frequency Limits of Bipolar Integrated Circuits

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THz Transistors:
What does this mean?
What are they for?
How do we make them?
What could we do with a THz Transistor?

High-Resolution Microwave ADCs and DACs

- mm-wave radio: 40+ Gb/s on 250 GHz carrier
- 340 GHz imaging systems
- 320 Gb/s fiber optics

Why develop transistors for mm-wave & sub-mm-wave applications?

→ compact ICs supporting complex high-frequency systems.
THz Transistors: What does this mean?

A 1 THz current-gain cutoff frequency \( f_\tau \) alone has little value. A transistor with 1000 GHz \( f_\tau \) and 100 GHz \( f_{\text{max}} \) cannot amplify a 101 GHz signal.

RF-ICs & MIMICs need high power-gain cutoff frequency \( f_{\text{max}} \) also need high breakdown & high safe operating area (power density).

100+ GHz digital also needs low \( \left( C_{\text{depletion}} \frac{\Delta V}{I} \right) \) and low \( \left( I*R_{\text{parasitic}} / \Delta V \right) \).

So, how do we make a transistor with

- \( >1 \) THz \( f_\tau \)
- \( >1 \) THz \( f_{\text{max}} \)
- \( <50 \) fs \( C \Delta V / I \) charging delays

and \( < 100 \) mV \( I*R_{\text{parasitic}} \) parasitic voltage drops?
THz Transistors:
How do we make them?
Present Status of Fast III-V Transistors

\[ f_t \text{ or } f_{\text{max}} \text{ alone} \]
\[ \frac{(f_t + f_{\text{max}})}{2} \]
\[ \sqrt{f_t f_{\text{max}}} \]
\[ \frac{1}{f_t + 1/f_{\text{max}}} \]

**popular metrics:**
- Power amplifiers: PAE, associated gain, mW/\mu m
- Low noise amplifiers: \( F_{\text{min}} \), associated gain
- Digital: \( f_{\text{clock}} \), hence
  - \( \frac{C_{cb} \Delta V}{I_c} \)
  - \( \frac{R_{ex} I_c}{\Delta V} \)
  - \( \frac{R_{bb} I_c}{\Delta V} \)
  - \( \tau_b + \tau_c \)

Red = manufacturable technology for 10,000- transistor ICs

Updated July 5 2006
Bipolar Transistor Scaling Laws

*Design changes required to double transistor bandwidth*

<table>
<thead>
<tr>
<th>key device parameter</th>
<th>required change</th>
</tr>
</thead>
<tbody>
<tr>
<td>collector depletion layer thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.414:1</td>
</tr>
<tr>
<td>emitter junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>collector junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>emitter resistance per unit emitter area</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>base contact resistivity (if contacts lie above collector junction)</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>base contact resistivity (if contacts do not lie above collector junction)</td>
<td>unchanged</td>
</tr>
</tbody>
</table>
### InP HBT Scaling Roadmaps

#### Key scaling challenges
-Emitter & base contact resistivity
-Current density

→ Device heating

Collector-base junction width scaling & Yield!

#### Key figures of merit for logic speed

<table>
<thead>
<tr>
<th>Parameter</th>
<th>scaling law</th>
<th>Gen. 2 (500 nm)</th>
<th>Gen. 3 (250 nm)</th>
<th>Gen. 4 (125 nm)</th>
<th>Gen. 5 (62.5 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MS-DFF speed</td>
<td>$\gamma^1$</td>
<td>150 GHz</td>
<td>235 GHz</td>
<td>330 GHz</td>
<td>440 GHz</td>
</tr>
<tr>
<td>Amplifier center frequency</td>
<td>$\gamma^1$</td>
<td>245 GHz</td>
<td>400 GHz</td>
<td>650 GHz</td>
<td>750 GHz</td>
</tr>
<tr>
<td>Emitter Width</td>
<td>$\gamma^2$</td>
<td>1/500 nm</td>
<td>1/250 nm</td>
<td>1/125 nm</td>
<td>1/62.5 nm</td>
</tr>
<tr>
<td>Resistivity</td>
<td>$\gamma^2$</td>
<td>16 $\Omega$-$\mu$m$^2$</td>
<td>9 $\Omega$-$\mu$m$^2$</td>
<td>4 $\Omega$-$\mu$m$^2$</td>
<td>2 $\Omega$-$\mu$m$^2$</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>$1/\gamma$</td>
<td>300 $\AA$</td>
<td>250 $\AA$</td>
<td>212 $\AA$</td>
<td>180 $\AA$</td>
</tr>
<tr>
<td>Contact width</td>
<td>$\sim1/\gamma$</td>
<td>300 nm</td>
<td>175 nm</td>
<td>120 nm</td>
<td>70 nm</td>
</tr>
<tr>
<td>Doping</td>
<td>$\gamma^0$</td>
<td>$7 \times 10^{19}$/$\text{cm}^2$</td>
<td>$7 \times 10^{19}$/$\text{cm}^2$</td>
<td>$7 \times 10^{19}$/$\text{cm}^2$</td>
<td>$7 \times 10^{19}$/$\text{cm}^2$</td>
</tr>
<tr>
<td>Sheet resistance</td>
<td>$\gamma^{1/2}$</td>
<td>500 $\Omega$</td>
<td>600 $\Omega$</td>
<td>707 $\Omega$</td>
<td>830 $\Omega$</td>
</tr>
<tr>
<td>Contact $\rho$</td>
<td>$1/\gamma^{1/2}$</td>
<td>20 $\Omega$-$\mu$m$^2$</td>
<td>10 $\Omega$-$\mu$m$^2$</td>
<td>5 $\Omega$-$\mu$m$^2$</td>
<td>5 $\Omega$-$\mu$m$^2$</td>
</tr>
<tr>
<td>Collector Width</td>
<td>$\gamma^2$</td>
<td>1.2 $\mu$m</td>
<td>0.60 $\mu$m</td>
<td>0.37 $\mu$m</td>
<td>0.20 $\mu$m</td>
</tr>
<tr>
<td>Thickness</td>
<td>$\gamma$</td>
<td>1500 $\AA$</td>
<td>1060 $\AA$</td>
<td>750 $\AA$</td>
<td>530 $\AA$</td>
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<tr>
<td>Current Density</td>
<td>$\gamma^2$</td>
<td>4.5 mA/$\mu$m$^2$</td>
<td>9 mA/$\mu$m$^2$</td>
<td>18 mA/$\mu$m$^2$</td>
<td>36 mA/$\mu$m$^2$</td>
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<tr>
<td>$A_{\text{collector}}/A_{\text{emitter}}$</td>
<td>$\gamma^0$</td>
<td>2.4</td>
<td>2.4</td>
<td>2.9</td>
<td>2.8</td>
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<tr>
<td>$f_T$</td>
<td>$\gamma^1$</td>
<td>370 GHz</td>
<td>530 GHz</td>
<td>730 GHz</td>
<td>1.0 THz</td>
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<tr>
<td>$f_{\text{max}}$</td>
<td>$\gamma^1$</td>
<td>490 GHz</td>
<td>801 GHz</td>
<td>1.30 THz</td>
<td>1.5 THz</td>
</tr>
<tr>
<td>$I_E/I_E$</td>
<td>$\gamma^0$</td>
<td>2.3 mA/$\mu$m$^2$</td>
<td>2.3 mA/$\mu$m$^2$</td>
<td>2.3 mA/$\mu$m$^2$</td>
<td>2.3 mA/$\mu$m$^2$</td>
</tr>
<tr>
<td>$\tau_f$</td>
<td>$1/\gamma$</td>
<td>340 fs</td>
<td>240 fs</td>
<td>180 fs</td>
<td>130 fs</td>
</tr>
<tr>
<td>$C_{cb}/I_c$</td>
<td>$1/\gamma$</td>
<td>400 fs/$V$</td>
<td>280 fs/$V$</td>
<td>250 fs/$V$</td>
<td>190 fs/$V$</td>
</tr>
<tr>
<td>$C_{cb\Delta V_{\text{logic}}}/I_c$</td>
<td>$1/\gamma$</td>
<td>120 fs</td>
<td>85 fs</td>
<td>74 fs</td>
<td>57 fs</td>
</tr>
<tr>
<td>$R_{ob}/(\Delta V_{\text{logic}}/I_c)$</td>
<td>$\gamma^0$</td>
<td>0.76</td>
<td>0.54</td>
<td>0.34</td>
<td>0.39</td>
</tr>
<tr>
<td>$C_{je}(\Delta V_{\text{logic}}/I_c)$</td>
<td>$1/\gamma^{3/2}$</td>
<td>380 fs</td>
<td>180 fs</td>
<td>94 fs</td>
<td>50 fs</td>
</tr>
<tr>
<td>$R_{ex}/(\Delta V_{\text{logic}}/I_c)$</td>
<td>$\gamma^0$</td>
<td>0.24</td>
<td>0.24</td>
<td>0.24</td>
<td>0.24</td>
</tr>
</tbody>
</table>
2005: InP DHBTs @ 500 nm Scaling Generation

Target Performance:
400 GHz $f_{\tau}$
500 GHz $f_{\text{max}}$
150 GHz digital clock rate (static dividers)
250 GHz power amplifiers

collector: 150 nm thick, 5 mA/μm² current density
10 mW/μm² power density @ 2V

emitter: 500 nm width, 15 Ω⋅μm² contact resistivity

base contact: 300 nm width, 20 Ω⋅μm² contact resistivity

InGaAs base
BC grade
collector

emitter contact
emitter

N-drift collector
N+ sub collector

S.l. InP substrate
Target Performance:
500 GHz $f_\tau$
700 GHz $f_{\text{max}}$
230 GHz digital clock rate (static dividers)
400 GHz power amplifiers

emitter: 250 nm width, $7.5 \, \Omega \cdot \mu m^2$ contact resistivity

base contact: 150 nm width, $10 \, \Omega \cdot \mu m^2$ contact resistivity

collector: 100 nm thick, 10 mA/\mu m$^2$ current density
20 mW/\mu m$^2$ power density @ 2V
125 nm Scaling Generation → almost-THz HBT

Target Performance:
700 GHz $f_\tau$
~1000 GHz $f_{\text{max}}$
330 GHz digital clock rate (static dividers)
600 GHz power amplifiers

emitter: 125 nm width, $5 \, \Omega \cdot \mu \text{m}^2$ contact resistivity

base contact: 75 nm width, $5 \, \Omega \cdot \mu \text{m}^2$ contact resistivity

collector: 75 nm thick,
20 mA/$\mu\text{m}^2$ current density
40 mW/$\mu\text{m}^2$ power density @ 2V
~3-4 V breakdown (BVCEO)

InGaAs base
BC grade
collector

N-drift collector
N+ sub collector

S.I. InP substrate
65 nm Scaling Generation → beyond 1-THz HBT

Target Performance:
1.0 THz $f_\tau$
1.7 GHz $f_{\text{max}}$
450 GHz digital clock rate (static dividers)
1 THz power amplifiers

emitter: 62.5 nm width, 2.5 $\Omega\cdot\mu\text{m}^2$ contact resistivity

base contact: 70 nm width, 5 $\Omega\cdot\mu\text{m}^2$ contact resistivity

InGaAs base
BC grade
collector

N+ sub collector
N- drift collector
S.I. InP substrate

collector: 53 nm thick, 35 mA/$\mu\text{m}^2$ current density
70 mW/$\mu\text{m}^2$ power density @ 2V
→ 2-3 V breakdown (BVCEO)
THz Transistors: addressing the key scaling challenges
Our HBT Base Contacts Today Use Pd or Pt to Penetrate Oxides

TEM: Lysczek, Robinson, & Mohney, Penn State
Sample: Urteaga, RSC

Our HBT Base Contacts Today Use Pd or Pt to Penetrate Oxides

Wafer first cleaned in reducing
Pd & Pt react with III-V semiconductor
Penetrate surface oxide
Today provide 5 Ω-μm² resistivity (base)
→ investigate better cleaning, alternative reaction metals

Reducing Emitter Resistance: ErAs Emitter Contacts

<table>
<thead>
<tr>
<th>Material</th>
<th>Lattice constant</th>
<th>mismatch to ErAs</th>
<th>mismatch to ErSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>ErAs</td>
<td>5.7427Å</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ErSb</td>
<td>6.108Å</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GaAs</td>
<td>5.6532Å</td>
<td>-1.6%</td>
<td>-8.0%</td>
</tr>
<tr>
<td>InP</td>
<td>5.8687Å</td>
<td>2.1%</td>
<td>-4.0%</td>
</tr>
<tr>
<td>GaSb</td>
<td>6.0959Å</td>
<td>5.8%</td>
<td>-0.2%</td>
</tr>
</tbody>
</table>

Epitaxial semimetal similar crystal structure to III-V semiconductors can be grown by MBE

In-situ contacts → no oxides, no contaminants
Lattice matched → few defect states → no surface Fermi pinning
Thermodynamically stable → little intermixing
Well-controlled (atomic precision) interface
Temperature Rise Within Transistor & Substrate

For each doubling in digital clock rate
emitter width $W_e$ decreases $4:1$
HBT spacing $D$ decreases $2:1$

HBT scaling → logarithmic temperature increase

$$\Delta T_{InP,1} \approx \frac{P}{\pi K_{InP} L_E} \ln \left( \frac{L_e}{W_e} \right) + \ldots$$

Thinning the substrate aggressively allows acceptable substrate temperature rise even at 300 GHz digital clock rate

$$T_{sub} = 15 \ \mu m \times \left( 160 \ \text{GHz}/f_{\text{clock}} \right)$$
Temperature Rise Within Package

For each doubling in digital clock rate
- emitter width $W_e$ decreases 4 : 1
- HBT spacing $D$ decreases 2 : 1
- chip dimensions $W_{chip}$ decrease 2 : 1

Total Package Temperature Rise

$$\Delta T_{package} \approx \left( \frac{2 + \pi}{2\pi} \right) \frac{P_{chip}}{K_{Cu} W_{chip}}$$

At 3 mA per transistor (100 Ω loading)
acceptable package temperature rise
with 1000 transistors / IC
even at 300 GHz digital clock rate.

Assumptions:
- Transistor spacing : 20 μm (150 GHz/$f_{max}$)
- $V_c = 2$ V bias
- 1000 transistors/IC
- IC power = 1.5 x (transistor dissipation)
UCSB DHBTs: 500-600 nm Scaling Generation

1.7 μm base-collector mesa

1.3 μm base-collector mesa

600 nm emitter width
InP DHBT: 600 nm lithography, 120 nm thick collector, 30 nm thick base

$\beta \approx 40$, $V_{BR,CEO} = 3.9$ V.

Emitter contact $R_{cont} < 10 \Omega \cdot \mu m^2$

Base: $R_{sheet} = 610 \Omega /sq$, $R_{cont} = 4.6 \Omega \cdot \mu m^2$

Collector: $R_{sheet} = 12.1 \Omega /sq$, $R_{cont} = 8.4 \Omega \cdot \mu m^2$
InP DHBT: 600 nm lithography, 75 nm collector, 20 nm base

**DC characteristics**

\[
\begin{align*}
A_{je} &= 0.65 \times 4.3 \ \mu m^2, \ I_{b, \text{step}} = 175 \ \mu A \\
\text{Average } \beta &\approx 50, B V_{CEO} = 3.2 \ V, B V_{CBO} = 3.4 \ V (I_c = 50 \ \mu A) \\
\text{Emitter contact (from RF extraction), } R_{\text{cont}} &\approx 8.6 \ \Omega \cdot \mu m^2 \\
\text{Base (from TLM)} : \ R_{\text{sheet}} = 805 \ \Omega / \text{sq}, \ R_{\text{cont}} = 16 \ \Omega \cdot \mu m^2 \\
\text{Collector (from TLM)} : \ R_{\text{sheet}} = 12.0 \ \Omega / \text{sq}, \ R_{\text{cont}} = 4.7 \ \Omega \cdot \mu m^2
\end{align*}
\]

\[
\begin{align*}
V_{cb} = 0 \ V &\quad \text{Peak } f_c \quad f_t = 544 \ \text{GHz}, f_{\text{max}} = 347 \ \text{GHz} \\
V_{cb} = 0.0 \ V \ (\text{dashed}) &\quad \text{Peak } f_{\text{max}} \\
V_{cb} = 0.3 \ V \ (\text{solid}) \\
I_b, I_c &\quad V_{be} \ (\text{A}) \\
H_{21} &\quad U \\
\text{RF characteristics}
\end{align*}
\]
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

<table>
<thead>
<tr>
<th>units</th>
<th>data current steering</th>
<th>data emitter followers</th>
<th>clock current steering</th>
<th>clock emitter followers</th>
</tr>
</thead>
<tbody>
<tr>
<td>size</td>
<td>µm²</td>
<td>0.5 x 3.5</td>
<td>0.5 x 4.5</td>
<td>0.5 x 4.5</td>
</tr>
<tr>
<td>current density</td>
<td>mA/µm²</td>
<td>6.9</td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td>C_{cb/ lc}</td>
<td>psec / V</td>
<td>0.59</td>
<td>0.99</td>
<td>0.74</td>
</tr>
<tr>
<td>V_{cb}</td>
<td>V</td>
<td>0.6</td>
<td>0</td>
<td>0.6</td>
</tr>
<tr>
<td>f_{c}</td>
<td>GHz</td>
<td>301</td>
<td>260</td>
<td>301</td>
</tr>
<tr>
<td>f_{max}</td>
<td>GHz</td>
<td>358</td>
<td>268</td>
<td>358</td>
</tr>
</tbody>
</table>

P_{DC, total} = 659.8 mW
divider core without output buffer ≈ 594.7 mW

Minimum input power (dBm) vs. frequency (GHz)

IC design: Z. Griffith, UCSB
HBT design: RSC / UCSB / GCS
IC Process / Fabrication: GCS
Test: UCSB / RSC / Mayo

probe station chuck @ 25°C
175 GHz Amplifiers with 300 GHz $f_{\text{max}}$ Mesa DHBTs

- 7.5 mW output power
- 7 dB gain measured @ 175 GHz
- 2 fingers x 0.8 um x 12 um, ~250 GHz $f_t$, 300 GHz $f_{\text{max}}$, $V_{\text{br}}$ ~ 7V, ~ 3 mA/um$^2$ current density
- $S_{21}$, $S_{11}$, $S_{22}$ dB
- 7-dB small-signal gain at 176 GHz
- 8.1 dBm output power at 6.3 dB gain
250 nm scaling generation DHBTs

- 100 % I-line lithography
- Emitter contact resistance reduced 40%: from 8.5 to 5 $\Omega \cdot \mu$m$^2$
- Base contact resistance is < 5 $\Omega \cdot \mu$m$^2$ --hard to measure
- Recall, 1/8 $\mu$m scaling generation needs $\leq 5$ $\Omega \cdot \mu$m$^2$ emitter $\rho_c$
0.30 µm emitter junction, \( W_c/W_e \sim 1.6 \)
First mm-wave results with 250 nm InP DHBTs

150 nm material
250 nm emitter width

\[ f_\tau = 420 \text{ GHz} \]
\[ f_{\text{max}} = 650 \text{ GHz} \]
\[ \sim 6 \text{ V breakdown} \]
\[ 30 \text{ mW/\(\mu m^2\) power handling} \]

results submitted postdeadline to 2006 DRC, E. Lind et al
330 GHz Cascode Power Amplifiers In Design

Thin-film microstrip lines
Output $P_{\text{sat}} = 50$ mW (17 dBm)
10-dB associated power gain
use the 650 GHz $f_{\text{max}}$ transistors
Frequency Limits of Bipolar Integrated Circuits

Done:

- $\sim 475$ GHz $f_t$ & $f_{\text{max}}$
- 150 GHz static dividers
- 160 Gb/s MUX & DMUX (Chalmers/Vitesse)

250 nm results coming very soon.

- expect $\sim 200$ GHz digital clock rate, 340 GHz amplifiers

THz transistors will come

The approach is scaling.

The limits are contact and thermal resistance.
Performance Parameters for Fast Logic & Mixed-Signal

Gate Delay Determined by:

Depletion capacitance charging through the logic swing

\[ \left( \frac{\Delta V_{\text{LOGIC}}}{I_c} \right) \left( C_{cb} + C_{be, \text{depletion}} \right) \]

Depletion capacitance charging through the base resistance

\[ R_{bb} \left( C_{cb} + C_{be, \text{depletion}} \right) \]

Supplying base + collector stored charge through the base resistance

\[ R_{bb} \left( \tau_b + \tau_c \right) \left( \frac{I_c}{\Delta V_{\text{LOGIC}}} \right) \]

The logic swing must be at least

\[ \Delta V_{\text{LOGIC}} > 4 \cdot \left( \frac{kT}{q} + R_{ex} I_c \right) \]

(\(\tau_b + \tau_c\)) typically 10 - 25% of total delay;

Delay not well correlated with \(f_t\)

\[ \left( \frac{\Delta V_{\text{LOGIC}}}{I_c} \right) \left( C_{cb} + C_{be, \text{depletion}} \right) \] is 55% - 80% of total.

High \((I_c / C_{cb})\) is a key HBT design objective.

\(R_{ex}\) must be very low for low \(\Delta V_{\text{logic}}\) at high \(J\)

Design HBTs for fast logic, not for high \(f_t\) & \(f_{\text{max}}\)
Performance Parameters for mm-wave Power

**Gain...under large-signal conditions**

![Graph showing MSG and MAG gain for common base, common emitter, and common collector configurations.]

...gain is less than MAG/MSG...

**Breakdown AND power density**

![Graph showing breakdown voltage BVCEO and power density.]  

\[ P_{\text{max}} = \left(\frac{1}{8}\right)(V_{\text{max}} - V_{\text{min}})I_{\text{max}} \]