InP HBT Digital ICs and MMICs in the 140-220 GHz band

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What could we do with 100-350 GHz integrated circuits?

**Optical Fiber Transmission**

40 Gb/s: InP and SiGe ICs commercially available

**80 & 160 Gb/s is feasible**
80-160 Gb/s InP ICs now clearly feasible
~100 GHz modulators demonstrated
100 + GHz photodiodes are easy
challenge: fiber dispersion

**Radio-wave Transmission / Radar / Imaging**

65-80 GHz, 120-160 GHz, 220-300 GHz
100 Gb/s transmission over 1 km in heavy rain
300 GHz imaging for foul-weather aviation

science
spectroscopy, radio astronomy

**Mixed-Signal ICs for Military Radar/Comms**
direct digital frequency synthesis, ADCs, DACs
high resolution at very high bandwidths sought

Why develop transistors for mm-wave & sub-mm-wave applications?
→ compact ICs supporting complex high-frequency systems.
## Frequency Limits and Scaling Laws of (most) Electron Devices

**Principle of Scaling**

- **$R_s$**
- **$R_j$**
- **$C$**
- **$L$**
- **$W$**
- **$D$**

### Contributing Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Time Constant</th>
<th>To Double Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transit time</td>
<td>$\tau \propto \frac{D}{v_{electron}}$</td>
<td>reduce $D$ by 2:1</td>
</tr>
<tr>
<td>$C \propto WL / D$</td>
<td>$R_{s, bottom} C \propto W / D$</td>
<td>reduce $W$ by 4:1</td>
</tr>
<tr>
<td>$R_{s, bottom} \propto \frac{1}{L}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C \propto WL / D$</td>
<td>$R_{s, top} C \propto \rho_{contact} / D$</td>
<td>reduce $\rho_{contact}$ by 4:1</td>
</tr>
<tr>
<td>$R_{s, top} \propto \frac{\rho_{contact}}{WL}$</td>
<td>$R_{s, top} C \propto \rho_{contact} / D$</td>
<td>use Schottky: $\rho_{contact} = 0$</td>
</tr>
<tr>
<td>$C \propto WL / D$</td>
<td>$R_{j, bottom} \propto WL / ID$</td>
<td>use flared contact: $R_{s, top} L \sim \rho_c \ln(1/W)$</td>
</tr>
<tr>
<td>$R_{j, bottom} \propto kT / qI$</td>
<td>$R_{j, bottom} \propto WL / ID$</td>
<td>increase $J$ by 4:1</td>
</tr>
<tr>
<td>Space-charge limited $J$</td>
<td>$J \propto \frac{(V + \phi)v_{electron}}{D^2}$, increases 4:1</td>
<td></td>
</tr>
</tbody>
</table>
R/C/τ Limits the Bandwidth of (most) Electron Devices

resistance  capacitance  transit time

device bandwidth

Applies to:
bipolar transistors, field-effect transistors, Schottky diodes
RTDs, photomixers, photodiodes

Applies whenever AC signals are removed through Ohmic contacts

Effective THz devices
must minimize, eliminate, or circumvent
contact resistance, capacitance, & transit time
Why aren't semiconductor lasers \( R/C/\tau \) limited?

Dielectric waveguide mode confines AC field away from resistive bulk and contact regions.

AC signal is not coupled through electrical contacts.

Dielectric mode confinement is harder at lower frequencies.
Diode & Transistor Integrated Circuits to ~ 1 THz

10-nm to 100-nm electron drift devices:

100 nm-generation InP DHBTs
signal generation with power to ~500 GHz

< 30 nm-generation InP HEMTs
30 nm devices now get ~600 GHz $f_t$
→ low noise figure at 300 GHz

<50 nm-generation InP or GaAs Schottky mixer diodes
many THz RC and transit time frequencies

And Silicon VLSI for applications below ~150 GHz!
**Fast IC Technologies**

**InP HBT:** 500 nm emitter
455 GHz $f_t$ / 485 GHz $f_{max}$
~4 V breakdown
150 GHz static dividers
178 GHz amplifiers

**SiGe HBT:** 130 nm emitter
300 GHz $f_t$ / 350 GHz $f_{max}$
96 GHz static dividers
77 GHz amplifiers
150 GHz push-push VCO- 75 GHz fundamental

**CMOS:** 90 nm node:
~200 GHz $f_t$ / 250 GHz $f_{max}$
60 GHz 2:1 mux
91 GHz amplifiers

**InP HBTs:**
450 GHz bandwidth at 500 nm scaling
Potential for much wider bandwidths at 100 nm scaling
We design HBTs for fast logic, not for high $f_\tau$ & $f_{\text{max}}$

Gate Delay Determined by:
Depletion capacitance charging through the logic swing:
$$\frac{\Delta V_{\text{LOGIC}}}{I_C} (C_{cb} + C_{be,\text{depletion}})$$

Depletion capacitance charging through the base resistance
$$R_{bb} (C_{cbi} + C_{be,\text{depletion}})$$

Supplying base + collector stored charge through the base resistance
$$R_{bb} (\tau_b + \tau_c) \left( \frac{I_C}{\Delta V_{\text{LOGIC}}} \right)$$

The logic swing must be at least
$$\Delta V_{\text{LOGIC}} > 4 \cdot \left( \frac{kT}{q} + R_{\text{ex}} I_C \right)$$

$$\tau_b + \tau_c \text{ typically 10 - 25\% of total delay;}$$
Delay not well correlated with $f_\tau$

$$\frac{\Delta V_{\text{LOGIC}}}{I_C} (C_{cb} + C_{be,\text{deplet}}) \text{ is 55\% - 80\% of total.}$$

High $(I_C / C_{cb})$ is a key HBT design objective.

$$J_{\text{max,Kirk}} = 2 e \overline{V}_{\text{electron}} (V_{ce, \text{operating}} + V_{ce, \text{full depletion}}) / T_C^2$$

$$\Rightarrow \frac{C_{cb} \Delta V_{\text{LOGIC}}}{I_C} = \frac{\Delta V_{\text{LOGIC}}}{2V_{CE,\text{min}}} \left( \frac{A_{\text{collector}}}{A_{\text{emitter}}} \right) \left( \frac{T_C}{2\overline{V}_{\text{electron}}} \right)$$

$R_{\text{ex}}$ must be very low for low $\Delta V_{\text{logic}}$ at high $J$
### Bipolar Transistor Scaling Laws & Scaling Roadmaps

**Scaling Laws:**
design changes required to double transistor bandwidth

<table>
<thead>
<tr>
<th>key device parameter</th>
<th>required change</th>
</tr>
</thead>
<tbody>
<tr>
<td>collector depletion layer thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>base thickness</td>
<td>decrease 1.414:1</td>
</tr>
<tr>
<td>emitter junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>collector junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>emitter resistance per unit emitter area</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>current density</td>
<td>increase 4:1</td>
</tr>
<tr>
<td>base contact resistivity (if contacts lie above collector junction)</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>base contact resistivity (if contacts do not lie above collector junction)</td>
<td>unchanged</td>
</tr>
</tbody>
</table>

**InP Technology Roadmap**

**40 / 80 / 160 Gb/s digital clock rate**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Gen. 1</th>
<th>Gen. 2</th>
<th>Gen. 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>MS-DFF speed</td>
<td>60 GHz</td>
<td>121 GHz</td>
<td>260 GHz</td>
</tr>
<tr>
<td>Emitter Width</td>
<td>1 µm</td>
<td>0.8 µm</td>
<td>0.3 µm</td>
</tr>
<tr>
<td>Parasitic Resistivity</td>
<td>50 Ω·µm²</td>
<td>20 Ω·µm²</td>
<td>5 Ω·µm²</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>400 Å</td>
<td>400 Å</td>
<td>300 Å</td>
</tr>
<tr>
<td>Doping</td>
<td>5 (10^{19}/\text{cm}^2)</td>
<td>7 (10^{19}/\text{cm}^2)</td>
<td>7 (10^{19}/\text{cm}^2)</td>
</tr>
<tr>
<td>Sheet resistance</td>
<td>750 Ω</td>
<td>700 Ω</td>
<td>700 Ω</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>150 Ω·µm²</td>
<td>20 Ω·µm²</td>
<td>20 Ω·µm²</td>
</tr>
<tr>
<td>Collector Width</td>
<td>3 µm</td>
<td>1.6 µm</td>
<td>0.7 µm</td>
</tr>
<tr>
<td>Collector Thickness</td>
<td>3000 Å</td>
<td>2000 Å</td>
<td>1000 Å</td>
</tr>
<tr>
<td>Current Density</td>
<td>1 mA/µm²</td>
<td>2.3 mA/µm²</td>
<td>12 mA/µm²</td>
</tr>
<tr>
<td>(A_{\text{collector}}/A_{\text{emitter}})</td>
<td>4.55</td>
<td>2.6</td>
<td>2.9</td>
</tr>
<tr>
<td>(f_i)</td>
<td>170 GHz</td>
<td>248 GHz</td>
<td>570 GHz</td>
</tr>
<tr>
<td>(f_{\text{max}})</td>
<td>170 GHz</td>
<td>411 GHz</td>
<td>680 GHz</td>
</tr>
</tbody>
</table>

**Key scaling challenges**

- emitter & base contact resistivity
- current density
- device heating
- collector-base junction width scaling & Yield!
Transistors & ICs at 500-600 nm Scaling Generation

1.7 μm base-collector mesa

1.3 μm base-collector mesa

600 nm emitter width
InP DHBT: 600 nm lithography, 150 nm thick collector, 30 nm thick base

Average $\beta \approx 36$, $V_{BR, CEO} = 5.1$ V ($I_c = 50$ $\mu$A)

Emitter contact (from RF extraction), $R_{cont} = 10.1 \Omega \cdot \mu$m$^2$

Base (from TLM): $R_{sheet} = 564 \Omega$/sq, $R_{cont} = 9.6 \Omega \cdot \mu$m$^2$

Collector (from TLM): $R_{sheet} = 11.9 \Omega$/sq, $R_{cont} = 5.4 \Omega \cdot \mu$m$^2$
\[ \beta \approx 40, \quad V_{BR,CEO} = 3.9 \, V. \]

Emitter contact \( R_{cont} < 10 \, \Omega \cdot \text{μm}^2 \)

Base: \( R_{\text{sheet}} = 610 \, \Omega / \text{sq}, \quad R_{cont} = 4.6 \, \Omega \cdot \text{μm}^2 \)

Collector: \( R_{\text{sheet}} = 12.1 \, \Omega / \text{sq}, \quad R_{cont} = 8.4 \, \Omega \cdot \text{μm}^2 \)

\[ A_{jbe} = 0.6 \times 4.3 \, \text{μm}^2 \]

\[ J_c = 20.6 \, \text{mA}, \quad V_{ce} = 1.53 \, \text{V} \]

\[ J_e = 8.0 \, \text{mA/μm}^2, \quad V_{cb} = 0.6 \, \text{V} \]

\[ f_t = 450 \, \text{GHz}, \quad f_{\text{max}} = 490 \, \text{GHz} \]
InP DHBT: 600 nm lithography, 100 nm thick collector, 30 nm thick base

Summary of device parameters—

Average $\beta \approx 40$, $V_{BR,CEO} = 3.1$ V ($I_c = 50$ $\mu$A)

Emitter contact (from RF extraction), $R_{cont} \approx 7.8$ $\Omega \cdot \mu$m$^2$

Base (from TLM): $R_{\text{sheet}} = 629$ $\Omega$/sq, $R_{cont} = 6.2$ $\Omega \cdot \mu$m$^2$

Collector (from TLM): $R_{\text{sheet}} = 12.9$ $\Omega$/sq, $R_{cont} = 4.0$ $\Omega \cdot \mu$m$^2$
InP DHBT: 600 nm lithography, 75 nm thick collector, 25 nm thick base

Average $\beta \approx 50$, $BV_{CEO} = 3.1$ V, $BV_{CBO} = 3.4$ V ($I_c = 50 \mu$A)

Emitter contact (from RF extraction), $R_{cont} \approx$ TBD $\Omega \cdot \mu$m²

Base (from TLM): $R_{sheet} = 805$ $\Omega$/sq, $R_{cont} = 16$ $\Omega \cdot \mu$m²

Collector (from TLM): $R_{sheet} = 12.0$ $\Omega$/sq, $R_{cont} = 4.7$ $\Omega \cdot \mu$m²
Summary of published HBT performance

**Popular metrics:**

\[
\frac{f_r + f_{\text{max}}}{2} \\
\sqrt{\frac{f_r f_{\text{max}}}{\tau}} \\
\left( \frac{1}{f_r} + \frac{1}{f_{\text{max}}} \right)^{-1}
\]

**Better metrics:**

- Power amplifiers:
  - PAE,
  - associated gain, mW/\(\mu\)m
- Low noise amplifiers:
  - \(F_{\text{min}}\),
  - associated gain, associated DC power

**Digital:**

- \(f_{\text{clock}}\), hence
- \(C_{eb} \Delta V / I_c\),
- \(R_{es} I_c / \Delta V\),
- \(R_{bb} I_c / \Delta V\),
- \((\tau_b + \tau_c)\)

---

**UCSB results are @ 600 nm; further progress requires scaling to 250 nm**

Stated dimensions are collector thickness
Devices are DHBTs except when labelled otherwise
Updated Sept, 2005
Digital circuits: towards 200 GHz clock rate

142 GHz latch from NNIN @ UCSB, 150 GHz ICs from UCSB/GSC/RSC, 200 GHz is the next goal

underlying technology: 400-500 GHz InP transistors

Z Griffith
Static Frequency Divider: Standard Digital Benchmark

ECL Master-Slave Latch with Inverting Feedback

Forms 2:1 Frequency Divider.

Maximum clock frequency is measure of technology speed.

Standard circuit configuration for consistent benchmarking - no tricks.

Small inductive peaking (L/R~1.3 ps).
CPW has parasitic modes, coupling from poor ground plane integrity.

Microstrip has high via inductance, has mode coupling unless substrate is thin.

Slot mode

Ground straps suppress slot mode, but multiple ground breaks in complex ICs produce ground return inductance. Ground vias suppress microstrip mode, wafer thinning suppresses substrate modes.

We prefer (credit to NTT) thin-film microstrip wiring, inverted is best for complex ICs.
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

<table>
<thead>
<tr>
<th>units</th>
<th>data current steering</th>
<th>data emitter followers</th>
<th>clock current steering</th>
<th>clock emitter followers</th>
</tr>
</thead>
<tbody>
<tr>
<td>size</td>
<td>μm²</td>
<td>0.5 x 3.5</td>
<td>0.5 x 4.5</td>
<td>0.5 x 4.5</td>
</tr>
<tr>
<td>current density</td>
<td>mA/μm²</td>
<td>6.9</td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td>C_{cb}/I_c</td>
<td>psec / V</td>
<td>0.59</td>
<td>0.99</td>
<td>0.74</td>
</tr>
<tr>
<td>V_{cb}</td>
<td>V</td>
<td>0.6</td>
<td>0</td>
<td>0.6</td>
</tr>
<tr>
<td>f_{τ}</td>
<td>GHz</td>
<td>301</td>
<td>260</td>
<td>301</td>
</tr>
<tr>
<td>f_{max}</td>
<td>GHz</td>
<td>358</td>
<td>268</td>
<td>358</td>
</tr>
</tbody>
</table>

P_{DC,total} = 659.8 mW
divider core without output buffer ≈ 594.7 mW

probe station chuck @ 25°C
UCSB 142 GHz Master-Slave Latches (Static Frequency Dividers)

**Static 2:1 divider:**

**UCSB technology 2004:**
InP mesa HBT technology 12-mask process 600 nm emitter width 142 GHz maximum clock.

**Implications:**
160 Gb/s fiber ICs
100 + Gb/s serial links
Target is 260 GHz clock rate at 300 nm scaling generation
Reducing Digital Circuit Dissipation

**ECL with impedance-matched 50 Ohm bus:**
- 25 Ohm load → switch 12 mA
- $12 \text{ mA} \times 7 \times 4 \text{ V} = 336 \text{ mW/latch}$

**CML with impedance-matched 50 Ohm bus:**
- 25 Ohm load → switch 12 mA
- $12 \text{ mA} \times 3 \times 3 \text{ V} = 108 \text{ mW/latch}$

**Low-Power CML**
- 100 Ohm loaded → switch 3 mA
- $3 \text{ mA} \times 3 \times 3 \text{ V} = 27 \text{ mW/latch}$

High speed @ low power = low $C_{wiring}$, low $C_{cb,\text{pad}}$

Significant dissipation in the clock emitter-follower level-shifters; some published work omits this from stated dissipation
Low Power CML Static Divider Designs

Simulated divider speed...

Without $C_{cb}$ reduction
$A_{jbe} = 3.0 \, \mu m^2$, $f_{max} = 130$ GHz
$A_{jbe} = 2.5 \, \mu m^2$, $f_{max} = 136$ GHz

With Implanted Sub-collector
$A_{jbe} = 3.0 \, \mu m^2$, $f_{max} = 143$ GHz
$A_{jbe} = 2.5 \, \mu m^2$, $f_{max} = 151$ GHz

With Pedestal
$A_{jbe} = 3.0 \, \mu m^2$, $f_{max} = 156$ GHz
$A_{jbe} = 2.5 \, \mu m^2$, $f_{max} = 164$ GHz

$P_{divider \, core}$, $\approx 214 \, mW$
Divide-by-4 at 128.6 GHz, $S^3$ RSC Technology

Measurements performed at UCSB, GUNN Source Used For CLK Input
RSC Wafer # xxxx, Divider ID: R3C2 #5A, Fabricated at RSC, Design at UCSB
$V_{\text{clk, offset}} = -0.45 \text{ V}$, $V_{\text{EE, div1,2}} = -3.4 \text{ V}$, $I_{\text{EE, total}} = 192 \text{ mA} - I_{\text{div1,2}}$ at $f_{\text{clk, max}} \leq 65 \text{ mA}$ per divider ckt
Power dissipation of input divider core w/out output buffer $< 221 \text{ mW}$ — room temp, no cooling
Ultra Low Power CML Static Divider Design

Simulated divider speed...

With Collector Pedestal

$A_{jbe} = 1.0 \, \mu m^2, \quad f_{max} = 100 \, GHz$

$P_{\text{divider core}} \approx 31 \, mW$
Ultra low-power RSC / UCSB CML dividers

Output waveform @ 6.0 GHz, $f_{\text{clk}} = 12$ GHz

Output waveform @ 25.5 GHz, $f_{\text{clk}} = 51$ GHz

The divider is operational from 12 GHz to 51 GHz

At $f_{\text{clk}} = 51$ GHz, $P_{\text{flip-flop}} = 29.2$ mW $\rightarrow$ Latch power $\times$ delay = 143 fJ, no emitter followers = 79.0 fJ

Confirms the circuit is fully static
Deep Submicron Bipolar Transistors for 140-220 GHz Amplification

**raw 0.3 μm transistor: high power gain @ 200 GHz**

1-transistor amplifier: 6.3dB @ 175 GHz

3-transistor amplifier: 8 dB @ 195 GHz
Mesa DHBT Power Amplifiers for 100-200 GHz Communications

7.5 mW output power

7 dB gain measured @ 175 GHz

175 GHz Power Amplifier Demonstrated in a 300 GHz f_{max} process
500 GHz f_{max} DHBTs available now, 600 GHz should be feasible soon
→ feasibility of power amplifiers to 350 GHz
→ Ultra high frequency communications

2 fingers x 0.8 um x 12 um, ~250 GHz f_t, 300 GHz f_{max}, V_{br} ~ 7V, ~ 3 mA/um² current density
Common-Base Has Highest Gain, but Layout Parasitics Matter!

V. Paidi, Z. Griffith, M. Dahlström
Single-Sided Collector Contacts Improve Common-Base Gain

![Diagram of collector contacts](image)

**Graph:**
- **X-axis:** Frequency, GHz
- **Y-axis:** MSG/MAG
- **Curves:**
  - Single sided collector
  - Double sided collector
  - Amplifier designs

**Figure Details:**
- Base plug
- Base
- Emitter
- Collector
- Interconnect metal
- N+ subcollector
- N- collector
- Semi-insulating InP

**References:**
- V. Paidi, Z. Griffith, M. Dahlström
172 GHz Common-Base Power Amplifier

8.3 dBm saturated output power
4.5-dB associated power gain at 172 GHz
DC bias: $I_c=47 \text{ mA}$, $V_{cb}=2.1\text{V}$.
176 GHz Two-Stage Amplifier

7-dB gain at 176 GHz
8.1 dBm output power, 6.3 dB power gain at 176 GHz
9.1 dBm saturated output power at 176 GHz

Gain, dB, Output Power, dBm

Gain, PAE

Output Power

Input Power, dBm

SAW, S11, S22

S21, S11, S22 dB

Frequency, GHz

Gain, PAE

PAE (%)
Transistor ICs → compact sub-mm-wave systems

Compact, Single-Chip Monolithic Frequency Multiplier Chains

Sub-mm-wave Frequency Generation by phase-locked source
Today: InP DHBTs @ 500 nm Scaling Generation

Device Performance: ~ 400 GHz $f_\tau$ and ~500 GHz $f_{\text{max}}$

Has enabled 150 GHz digital clock rate (static dividers)

Should enable 300 GHz power amplifiers (175 GHz realized with 300 GHz $f_{\text{max}}$)

**emitter**: 500 nm width, **15 $\Omega \cdot \mu m^2$** contact resistivity

**base contact**: 300 nm width, **20 $\Omega \cdot \mu m^2$** contact resistivity

**collector**: 150 nm thick, 5 mA/$\mu m^2$ current density, 10 mW/$\mu m^2$ power density @ 2V, **15 K/(mW/$\mu m^2$)** thermal resistance

S.I. InP substrate

InGaAs base

BC grade collector

$N$- drift collector

$N+$ sub collector

emitter contact
**Next: 250 nm Scaling Generation, 1.414:1 faster**

Goals: 500 GHz $f_t$ and 700 GHz $f_{\text{max}}$
- 230 GHz digital clock rate (static dividers)
- 400 GHz power amplifiers

**Direct, brute-force scaling**
- **Emitter:** 250 nm width, $7.5 \, \Omega \cdot \mu m^2$ contact resistivity
- **Base Contact:** 150 nm width, $10 \, \Omega \cdot \mu m^2$ resistivity
- **Collector:** 110 nm thick, $10 \, mA/\mu m^2$ current density
- $20 \, mW/\mu m^2$ power density @ 2V
- $7.5 \, K/(mW/\mu m^2)$ thermal resistance

Requiring innovations in emitter & base contacts: processes & metallurgy

**Parasitic Reduction**
- **Regrown Emitter with Wide Contact:** reduces access resistance
- **Collector Pedestal:** reduces capacitance under base contacts, allows wider & more resistive base contacts

Requiring implants and regrowth processes
Manufacturable Emitter Dielectric Sidewall Processes

First-Generation: UCSB and Rockwell Scientific
Miguel Urteaga

- $\text{Si}_3\text{N}_4$
- thin emitter
- base contacts by planarization & etch-back

266 GHz $f_t$, 133 GHz $f_{max}$, $C_{cb/i} = 0.4$ ps/V

2nd-Generation: Rockwell Scientific
Miguel Urteaga, Petra Rowell

- electroplated emitter and base contacts

250 nm emitter

Urteaga, Rodwell, Pierson, Rowell, Brar, Nguyen, Nguyen: UCSB, RSC, GCS

Urteaga, Rowell, Pierson, Brar: RSC
HBT with Epitaxial Extrinsic Emitter

InAlAs/InP Current Barrier
InP Emitter
Emitter Contact
Base Contact
InGaAs Extrinsic Base
InGaAs Intrinsic Base
InP Collector
InP Subcollector

$I_c$ [mA] vs. $V_{ce}$ [V]

$I_b$, step = 2 mA

$J_c$ [mA/um$^2$]

$0 \leq V_{be} \leq 1.5$

$V_{offset} = 0.0$ V

$W_E = 1.0$ µm

Max($\beta$) = 7.0

$V_{offset} = 0.0$ V

$I_b, I_c$ [A]

$I_b, I_c$ vs. $V_{be}$ [V]
Subcollector & Pedestal Implant

Subcollector implant eliminates $C_{cb}$ in base pad area - key for high speed in lower-power logic.

Pedestal further reduces $C_{cb}$.
Roadmap for the 125 nm Scaling Generation

Target transistor performance: 700 GHz $f_\tau$, 1100 GHz $f_{\text{max}}$, comparable improvement of other key parameters: $C_{cb}\Delta V/I_c$, $R_{exc}/\Delta V$, $R_{bbl}/\Delta V$

Target circuit performance
330 GHz digital clock rate (static dividers)
600 GHz power amplifiers

What would be needed to obtain this?

emitter: 125 nm width, $5 \, \Omega\cdot\mu\text{m}^2$ contact resistivity

base contact: 75 nm width, $\sim 5 \, \Omega\cdot\mu\text{m}^2$ contact resistivity

collector: 75 nm thick, 20 mA/$\mu\text{m}^2$ current density, 40 mW/$\mu\text{m}^2$ power density @ 2V, 4 K/(mW/$\mu\text{m}^2$) thermal resistance

S.I. InP substrate
Indium Phosphide HBTs for 100-600 GHz ICs

**InP HBT now: at 500 nm scaling generation**
- 455 GHz $f_t$ & 485 GHz $f_{max}$
- 150 GHz static dividers & 180 GHz amplifiers demonstrated
- 200 GHz digital latches & 300 GHz amplifiers are feasible

**InP HBT: future, at 125 nm scaling generation**
- 2:1 increase in bandwidth (?)
- 700 GHz $f_t$ & 1.1 THz $f_{max}$, 330 GHz digital latches & 600 GHz amplifiers ?
- demands 4:1 better Ohmic contacts
- demands 4:1 increased current density.

**Applications:**
- 160+ Gb/s fiber ICs,
- 300 GHz MIMICs for communications, radar, & imaging
- GHz ADCs / DACs / DDFS / etc.
- & applications unforeseen & unanticipated
Backups
Submicron diodes for sub-millimeter-waves

Scaled Schottky diodes ICs for near-Triz Instruments

GaAs Nonlinear Transmission Line ICs:
0.5 ps pulse generators &
DC-700 GHZ sampling circuits

underlying Semiconductor Technology:
scaled Triz Schottky varactor diodes

0.5 ps diodes

Instrumentation, not communication technology:
NLTL, harmonic conversion loss ~1e", noise figure of sampling

NLTL-gated diode sampling ICs: results from the 1990's

Warrenton, Garrison, by NLTL

DC-700 GHz sampling IC

instrumentation and circuit analysis

instrumentation and circuit layout

Deep submicron diode ICs for (sub)-mm-wave applications

Submicron Schottky, novel: Power Source Diodes

Diode bandwidth limits:
transistor: RC limits
This device: JFET (UCSB - late 90s)
100 mm x 0.5 um T-gate, 150 A depletion depth
~15 THzRC & transit line cutoff frequencies

JFET Schottky-diode harmonic mixer

Submicron Schottky-JFET transistor: RTD

RTD Scaling:
reduce contact width: 0.1 um
reduce depletion depth: 100 A
increase JFET: 100 A/cm²
use zero-resistance Schottky contact

Ge-Element Schottky-RTD oscillator at 65-200 MHz

0.1 μm, 22 Hz Schottky-RTD

array oscillators, 0.1 μm, 22 Hz Schottky-RTD
Hierarchy of ECL Static Frequency Divider

**ECL NAND/NOR Gate**

**ECL Latch: level-clocked memory element**

**Master-Slave Latch:** transition-clocked memory element

**2:1 Static Frequency Divider**
Transit time Modulation Causes $C_{cb}$ Modulation

\[ Q_{\text{base holes}} = \text{constant} + Q_{\text{base electrons}} + \int_{V_{cb}}^{V_{T}} qn(x)A(x-y)dx + V_b eA/T_c = f(I_c, V_{cb}) \]

\[ C_{cb} = -\frac{\partial Q_{\text{base holes}}}{\partial V_{cb}} \]

\[ \tau_f = \frac{\partial Q_{\text{base holes}}}{\partial I_c} \Rightarrow \frac{\partial C_{cb}}{\partial I_c} = -\frac{\partial \tau_f}{\partial V_{cb}} \]

Camnitz and Moll, Betser & Ritter, D. Root

**Collector Velocity Modulation:**

\[ \frac{\partial \tau_f}{\partial V_{cb}} > 0 \Rightarrow \frac{\partial C_{cb}}{\partial I_c} < 0 \]

*Increase in $\tau_c$ with $V_{cb} \rightarrow$ reduced $C_{cb}$*

- strong effect in InGaAs SHBTs
- weak effect in InP DHBTS

**Kirk Effect:**

\[ \frac{\partial \tau_f}{\partial V_{cb}} < 0 \Rightarrow \frac{\partial C_{cb}}{\partial I_c} > 0 \]

*Increase in $C_{cb}$ is due to both*

- base pushout into collector
- and modulation of $\tau_c$ by $V_{cb}$
Transit time Modulation $\rightarrow$ Negative Resistance $\rightarrow$ Infinite Gain

- $\Delta V$ is negative
- $\Delta J = J_e (\Delta V / V_0)$
- $\Delta T = 2 \tau_c (V_0 + \Delta V)$

Negative capacitance

$C_{ch,cancc} = -I_c \left( \frac{\partial \tau_f}{\partial V_{ch}} \right)$

Negative resistance

$R = 2 (\tau_c / 3C_{ch,cancc})$

Positive $G_{12}$ = negative conductance

Negative $G_{22}$ = negative conductance