A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-In Dynamic OR Gates

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***Abstract*—Dynamic gates have been excellent choice in the design of high-performance modules in modern microprocessors. The only limitation of dynamic gates is their relatively low noise margin compared to that of standard CMOS gates. Traditionally, this issue has been resolved by employing a pMOS keeper circuit that compensates for leakage current of the pull-down nMOS network. In the earlier technology nodes, the keeper circuit could improve reliability of the dynamic gates with minor performance penalty. However, aggressive scaling trends of CMOS technology along with increasing levels of process variations have reduced effectiveness of the traditional keeper approach. This is because to maintain an acceptable noise margin level in deep sub-100 nm technologies, large pMOS keepers must be employed, which generates substantial contention between the keeper and the pull-down network, and hence results in severe loss of performance and high power consumption. This problem is more severe in wide fan-in dynamic gates due to the large number of leaky nMOS devices connected to the dynamic node. In this paper, a novel variation-tolerant keeper architecture is proposed, which is capable of significantly reducing contention and improving performance and power consumption. Using circuit simulations, the overall improved characteristics of the proposed keeper are demonstrated in comparison to those of the traditional as well as several state-of-the-art keepers. The proposed keeper exhibits the lowest delay deviation under different levels of process variations. Also, it is shown that for an eight-input OR gate, in presence of 15% $V_{\rm th}$ fluctuations, the proposed architecture can lead to 20%, 15%, and more than 40% reduction in power consumption, mean delay, and standard deviation of delay, respectively, when compared to the traditional keeper circuit.**

***Index Terms*—CMOS, dynamic gates, integrated circuit (IC) design, keeper circuit, leakage currents, low-power design, microprocessors, process variation, robustness, variation tolerant.**

I. Introduction

A PROCESS variation-tolerant keeper architecture for wide fan-in dynamic gates is proposed, which can result in higher performance and lower power consumption compared to conventional dynamic gates with traditional keepers. Wide fan-in dynamic OR gates are one of the most critical building blocks of register file circuits in modern microprocessors [1]. However, as we will discuss in the following sections, robustness and performance of wide fan-in dynamic gates significantly degrade with increasing levels of subthreshold leakage and process variations. As a result, it becomes extremely difficult to achieve satisfactory robustness–performance tradeoffs under such circumstances. Several attempts have been made to address these issues in the literature. The novelty of our contribution is that the proposed circuit simultaneously improves performance and decreases power consumption. Moreover, as will be shown by simulation results, the new keeper is much less sensitive to process variations. In this section, first, we provide a brief overview of the importance of wide fan-in gates in the design of high-performance register files, and then, we explain implications of process variation on the design of such gates. Finally, we summarize previous works and demonstrate the novelty of the proposed architecture.

A. Wide Fan-In Dynamic OR Gates in Register File Architectures

Register files are one of the most important modules in the critical path of modern microprocessors [1]. The basic operation of a register file is to store temporary and intermediate variables that are being used in the execution of a sequence of instructions. Fig. 1 shows the block diagram of Intel's Pentium 4 processor architecture. In this processor, two register files are deployed in the data path, which are boxed for emphasis. As it can be observed, to execute each instruction, data should either be written to or read from these register files. Therefore, fast register file architectures are crucial in achieving high-performance operation in microprocessors.

Fig. 2(a) shows a block diagram of a simplified register file, which is composed of an array of static RAM (SRAM) based registers, a read and a write port. It should be noted that actual register files have multiple read and write ports and also have much more registers. Read and write ports are generally implemented using multiplexer (for read port) and demultiplexer (for write port) circuits. On the other hand, these multiplexer and demultiplexer circuits are usually realized by employing OR and inverter gates, as shown in Fig. 2(b). This figure illustrates a simple 4×1 multiplexer with four input lines ($D_0 - D_3$), two address bits (S_0 and S_1), and one output. Note that a register file with 2^n registers needs n-bit address lines, and hence n-input OR gates. As a result, for large register files, wider fan-in dynamic OR gates are required for address coding/decoding. As will be discussed in the next section, in sub-100 nm regime, design of

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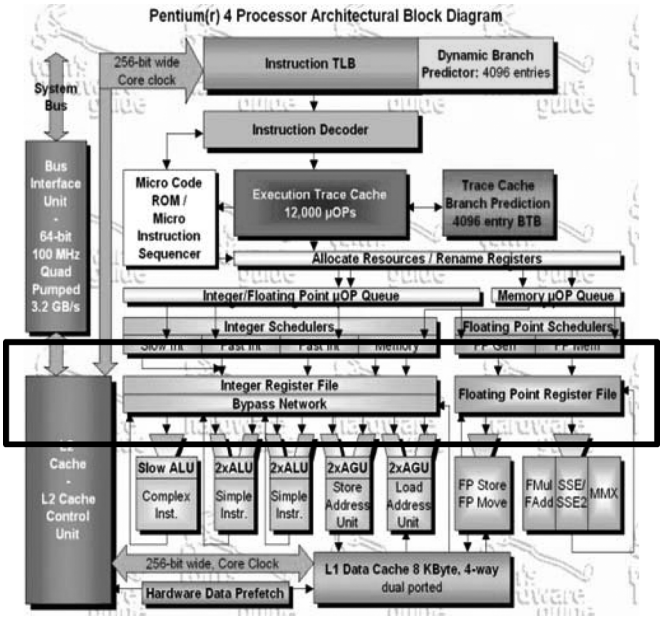

Fig. 1. Register files deployed in Intel's Pentium 4 architecture.

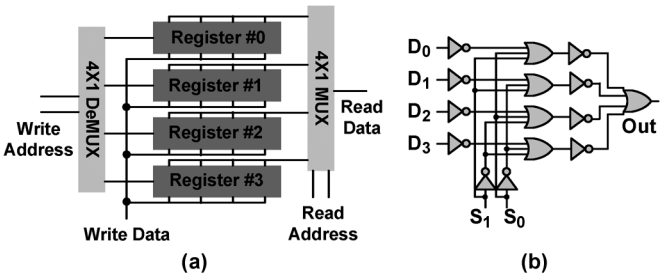

Fig. 2. (a) Block diagram of a simplified register file and (b) read port implemented using 4×1 multiplexer (MUX).

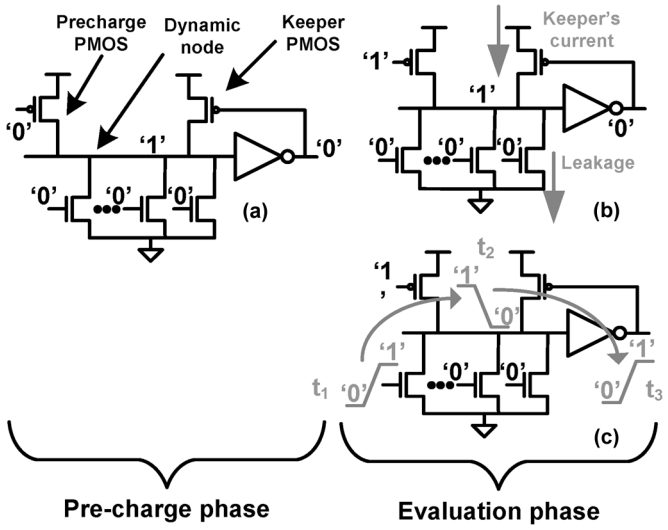

Fig. 3. Dynamic OR gate with traditional keeper indicating (a) precharge phase and the evaluation phase with (b) all inputs = "0" and (c) at least one input = "1."

robust and high-performance wide fan-in dynamic OR gates is a challenging task due to impact of process variations.

B. Implications of Process Variation on Dynamic Logic Gates

Dynamic implementation of wide fan-in OR gates offers low latency, because unlike its static CMOS counterpart, it does not require a pMOS transistor stack in the pull-up network, as shown in Fig. 3(a). In this logic style, all inputs are applied to the nMOS devices of the pull-down network. Operation of dynamic gates occurs in two successive phases: precharge and evaluation. In the precharge phase, as shown in Fig. 3(a), all inputs remain low and the dynamic node is pulled up to V_{dd} through a precharge pMOS device. On the other hand, in the evaluation phase, depending on the input pattern, either charge of the dynamic node is retained [Fig. 3(b)] or removed [Fig. 3(c)]. However, the major disadvantage of dynamic gates is their low noise margin, due to the fact that the dynamic node is not always connected to dc voltage sources, and hence, stored charge on the dynamic node can be discharged by leakage current of the pull-down network. Traditionally, this issue has been addressed by employing a pMOS keeper that compensates for leakage current of the pull-down network. If all inputs are zero, output of the OR gate must be zero, and hence, dynamic node must remain high, and consequently, the pMOS keeper transistor must stay ON to compensate for any leakage current drawn out of the dynamic node [Fig. 3(b)]. In the case where at least one input is high, stored charge on the dynamic node must be removed. However, in this case, both the pull-down and keeper circuits stay ON simultaneously during the time interval from when the pull-down network starts conducting [t_1 in Fig. 3(c)] until voltage of the output node reaches a certain high voltage [t_3 in Fig. 3(c)]. This contention between the keeper and the pull-down network increases both delay of the OR gate and its power consumption [2]. As it can be observed, in the case of Fig. 3(b), a strong keeper is desirable to increase noise margin while in contrast, in case of Fig. 3(c), a week keeper is preferred to speed up the switching transition. These conflicting requirements give rise to tradeoff between achievable performance/power consumption and noise margin of the dynamic circuit [3].

This tradeoff is becoming increasingly demanding in sub-100 nm technology nodes because of two reasons. First, as technology is being scaled, leakage current of transistors increases dramatically, which implies that dynamic gates require much larger keepers. Second, process variation [4], [5] leads to a significant variation in leakage current of gates located on different regions of a die. As a result, to maintain appropriate level of noise margin for different dynamic OR gates spread over a chip, designers must use large pMOS keepers such that sufficient amount of current is supplied to the dynamic node even in worst-case scenarios. However, this results in significant contention between the keeper and the pull-down network leading to large power dissipation as well as performance degradation.

C. Prior Works

In the literature, several attempts have been made to address the robustness problem of dynamic gates. These papers can be classified into two groups: designs in the first category try to decrease the leakage current through reengineering of the pull-down network [6], [7]. On the other hand, papers in the second group, including this paper, focus on the design of innovative

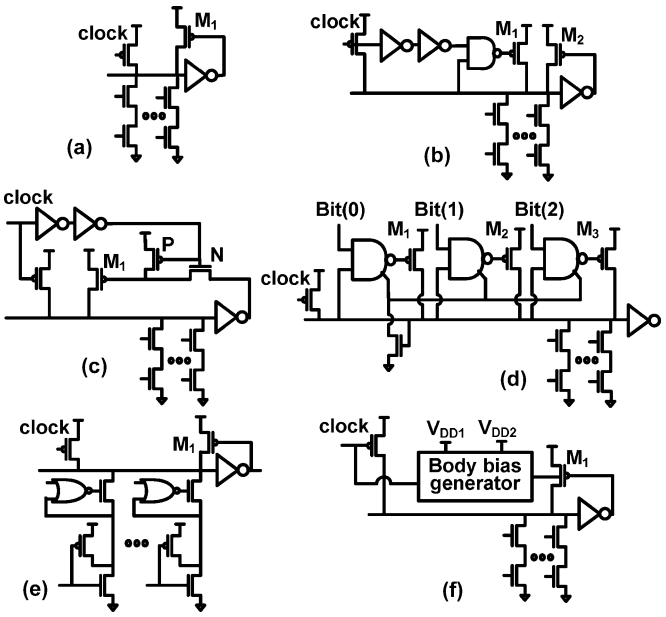

Fig. 4. (a) Traditional keeper. (b) Alvandpour *et al.* [8]. (c) Anis *et al.* [9]. (d) Kim *et al.* [10]. (e) Krishnamurthy *et al.* [6]. (f) Kursun and Friedman [11].

keeper circuits [2], [8]–[11]. Since, redesign of keeper usually has less overhead than modification of the pull-down network, these works focus on presenting new keeper circuits. Alvandpour *et al.* [8] [Fig. 4(b)] have split the keeper circuit into two parts so that during the evaluation phase, first part is always ON and the second component turns ON after a delay. Delay is used to decrease the amount of contention between the pMOS keeper and the pull-down network throughout switching transition. The drawback of this approach is that the keeper is significantly weak during the transition of the precharge/evaluation clock signal. Moreover, during the clock transition, considerable noise can be imposed on the dynamic node through coupling capacitances between the dynamic node and other switching signals in the circuit, which makes the dynamic node extremely vulnerable.

Anis *et al.* [9] [Fig. 4(c)] have proposed a different circuit where the keeper circuit is composed of only one pMOS transistor, which remains OFF during the early part of the evaluation phase and only turns ON if the dynamic node is supposed to remain high for the rest of the period depending on the input pattern. Similar to the approach proposed by Alvandpour *et al.*, this approach can also result in lower noise margin at the beginning of the evaluation phase when the dynamic node is floating.

Kim *et al.* [10] [Fig. 4(d)] have proposed a programmable keeper circuit, so that its strength can be adjusted using a 3-bit enable digital input. This keeper has three stages with relative strengths of 1, 2, and 4. Parameter variation is measured with a sensor, and then, appropriate strength for the keeper is chosen by applying the 3-bit input. In this approach, dynamic node is heavily loaded by gate and junction capacitance of control and keeper transistors, and hence, performance can be degraded. Furthermore, Krishnamurthy *et al.* [6] have proposed a modified pull-down network [Fig. 4(e)] where the leakage current is significantly reduced by creating a negative V_{GS} across the top transistors in the pull-down network when all inputs are "0." This is achieved by connecting the gate of the top transistors to ground using NOR gates while applying V_{DD} to their drain terminals employing small pMOS devices. Note that in this circuit, unlike the other approaches outlined in Fig. 4, low-power operation is achieved by redesigning the pull-down network as opposed to using keeper design.

Kursun and Friedman [11] [Fig. 4(f)] have proposed a circuit to lower the contention between the keeper and the pull-down network during the switching period by applying a body bias to the keeper transistor. The body of the keeper is connected to V_{DD1} during normal operation and to V_{DD2} at the time of transition. Since $V_{DD2} > V_{DD1}$, the keeper supplies less current due to body effect during the switching, which results in lower delay and power consumption.

Li and Mazumder [2] have proposed a new approach in which, instead of a pMOS transistor, a semiconductor device (non-CMOS) with negative resistance characteristics has been used that is not easily integrable in a CMOS process.

D. Scope of This Paper

In this paper, a novel variation-aware low-power/high-performance keeper architecture is presented, which is capable of improving performance and power consumption of dynamic gates. Circuit simulations have been used to show superior performance of the proposed architecture in comparison to existing works and the traditional keeper. Under different levels of process variations, the proposed keeper demonstrates the lowest delay deviation, and hence, it is the most variation tolerant choice among the different architectures existing in the literature. It is shown that in presence of 15% $V_{\rm th}$ fluctuations, an eight-input OR gate with the new keeper compared to the same gate with the traditional keeper leads to 20%, 15%, and more than 40% reduction in power consumption, mean delay, and standard deviation of delay, respectively.

Rest of the paper is organized as follows. Section II includes characterization of the tradeoff between noise margin and performance of dynamic gates through a graphical presentation leading to the main idea behind the proposed circuit. In Section III, the architecture of the proposed keeper is presented and details about its implementation are discussed. Section IV includes simulation results and comparison between the proposed and other keeper circuits outlined in Fig. 4. Finally, concluding remarks are made in Section V.

II. Keeper Sizing for Dynamic OR Gates

Higher performance of wide fan-in dynamic OR gates comes at the cost of their lower noise margins. This tradeoff is shown graphically in Fig. 5 for an eight-input dynamic OR gate with a simple pMOS keeper. Here, *Y*- and *X*-axis represent normalized worst-case delay and the noise margin in volts, respectively. Each of the three curves shown in this figure corresponds to a different level of process variation measured in terms of standard deviation of the threshold voltage $(\sigma_{V_{\rm th}})$ as percentage of its nominal value $(\mu_{V_{\rm th}})$. As it can be observed, in order to achieve higher reliability, performance penalty that must be compromised increases significantly. Moreover, for a particular value of noise margin, performance penalty also increases as the

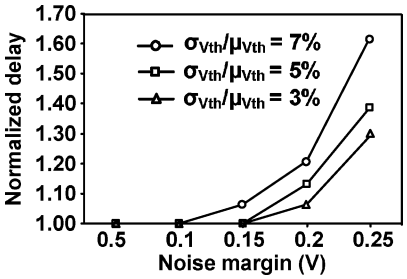

Fig. 5. Tradeoffs between the noise margin and performance of the dynamic gate during pMOS keeper sizing for different levels of process variations. To achieve higher noise margin, higher performance penalty must be compromised.

level of process variations rises from $\sigma_{V_{\rm th}} = 3\%$ to 5% and 7% of $\mu_{V_{\rm th}}$.

In our investigations, as will be discussed in the following subsections, we observed that the traditional keeper is not the optimal solution for the tradeoff between performance and robustness. In other words, with an improved design for the keeper, it is possible to achieve higher performance without compromising robustness. The idea behind the improved keeper proposed in this paper is based on a graphical representation of the tradeoff between performance and noise margin. However, before exploring the design idea, we will clarify the definitions of noise margin and performance metrics that have been used in this paper.

A. Noise Margin and Its Characterization

In the literature, several metrics have been proposed to characterize the noise margin of dynamic gates [3]. In this paper, a noise margin metric called *unity noise gain* (UNG) has been used [2]. UNG is defined as the voltage level, which if applied to all inputs of a dynamic gate results in a signal of same amplitude at the output node. This is shown in Fig. 6(a), where a dc voltage source of amplitude V_{NM} is applied to all the nMOS input transistors of the pull-down network and the size of pMOS keeper is chosen in a way so that voltage of the output node is also equal to V_{NM}. It should be noted that if threshold voltage of the transistors in the pull-down network is altered due to process variation, a keeper with different size will be needed to support the same noise margin of V_{NM}. In this paper, we only consider the systematic $V_{\rm th}$ variations, which means that the impact of random variations is neglected, because of the large size of transistors in the dynamic gates (the effect of random variation is more pronounced in smaller devices). It should be noted that systematic variations occur due to subwavelength lithography where the wavelength of light beams used in the fabrication process is longer than the size of transistors. As a result, transistors located within a certain spatial proximity exhibit highly correlated physical features (such as channel lengths). Therefore, in a dynamic gate, one can assume that both nMOS and pMOS devices have longer/shorter channel length, and hence higher/lower threshold voltages.

To assess the effectiveness of the traditional keeper [shown in Fig. 6(a)], we would like to characterize the behavior of an "ideal keeper." An ideal keeper can be defined as a keeper circuit, which, for a particular noise margin, supplies the minimum required amount of current to the dynamic node. To quantify the

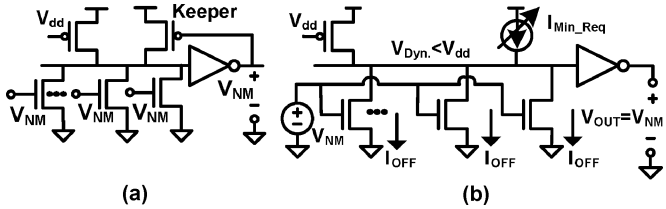

Fig. 6. (a) Definition of UNG and (b) measurement of minimum required current in presence of $V_{\rm th}$ variations for a particular noise margin.

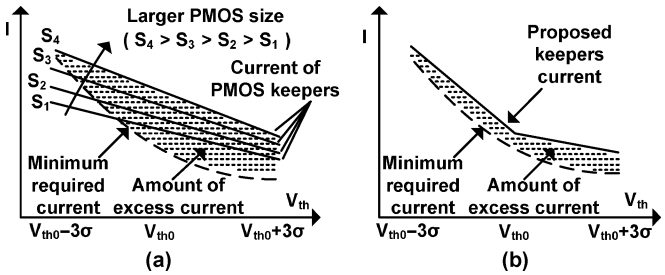

Fig. 7. (a) Minimum required current (broken curve) and current of traditional keepers (solid lines). (b) Minimum required current and current of the proposed keeper to lower contention (hashed area).

behavior of such an ideal keeper, we simulated the circuit configuration of Fig. 6(b) where the keeper is replaced by a current source. In this circuit, for a given level of noise margin V_{NM}, the current source is tuned so that it supplies just enough current $(I_{\rm Min\_Req})$ to the dynamic node to make voltage of the output node $V_{\rm OUT}$ equal to V_{NM}. We refer to the amplitude of the current source $I_{\rm Min\_Req}$ as the *minimum required current*.

In presence of threshold voltage variation, leakage current reveals large deviation; therefore, minimum required current will also vary. To account for the impact of variation, the configuration in Fig. 6(b) has been simulated by sweeping the threshold voltage over its range of variation and measuring the minimum required current at each point. One can plot these simulation results on a curve where minimum required current is shown on the vertical axis and threshold voltage on the horizontal axis. A sketch of such a curve is shown in Fig. 7(a) where it is assumed that all the devices are affected in a similar way by the systematic threshold voltage variation (for instance, whenever we assume that $V_{\rm th}$ is 3σ higher than its nominal value, it is true for both pMOS and nMOS devices), and hence, threshold voltage of the keeper also changes in the same direction. The broken curve in this figure displays minimum required current over the threshold voltage ranging from $V_{\rm th0} - 3\sigma$ to $V_{\rm th0} + 3\sigma$, where $V_{\rm th0}$ and σ are nominal value and standard deviation of the threshold voltage, respectively. As expected, the minimum required current is much higher at the lower end of the range (around $V_{\rm th0} - 3\sigma$). Alternatively, the solid lines represent drive currents of traditional pMOS keepers with different sizes $(S_1, S_2, \ldots, S_4)$, which exhibit linear behavior with respect to threshold voltage variations.

To meet the minimum current criteria over the entire threshold voltage variation range, pMOS keeper must be sized up and in this figure, only the top solid line (S_4) satisfies such a requirement. Since the minimum required current curve represents the behavior of an ideal keeper, it can be used to evaluate

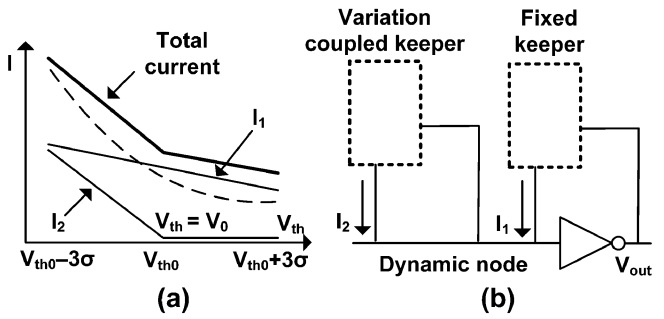

Fig. 8. (a) Generating the current curve of the new keeper by adding up two current curves I_1 and I_2 supplied to the dynamic node. (b) Block diagram of the proposed keeper architecture composed of two independent keeper circuits each responsible for generating one of the current curves I_1 and I_2.

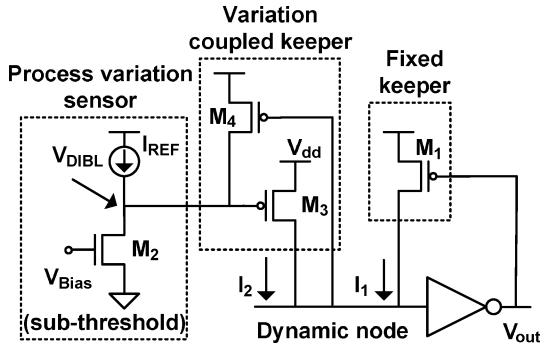

Fig. 9. Circuit level diagram of the proposed keeper architecture.

the performance of traditional keepers. Although the pMOS keeper S_4 satisfies the minimum current criteria over the entire range of $V_{\rm th}$, there is a large gap between its current and that of the ideal keeper. In other words, the hashed area in Fig. 7(a) corresponds to the excess amount of current injected into the dynamic node that is higher than the necessary amount. This excess current (hashed area) can be reduced with proper design of the keeper, as shown in Fig. 7(b). It is desirable to design a keeper with current curve similar to the depicted broken line, which can significantly reduce the amount of contention. Now, we explain how the proposed keeper generates a current curve similar to the solid line in Fig. 7(b).

In the proposed architecture [Fig. 8(a)], minimum required current is generated through superposition of two independent current sources [12]. The first component is a small traditional pMOS keeper and its current curve (I_1) is a straight line with a small slope, while the second component is a process variation-coupled circuit, which has insignificant current up to the point V_0 and begins to supply current afterwards (I_2) with a large slope. The bold solid line is the total current supplied to the dynamic node by these two components. Accordingly, the hardware implementation of the proposed keeper is also composed of two parts, which are connected to the dynamic node in parallel, as shown in Fig. 8(b). Details related to the design of this keeper architecture are provided in Section III.

Although redesigning the keeper circuit reduces contention current, its implementation requires additional circuitry compared to the traditional single pMOS keeper, which can diminish the potentially achievable performance enhancement. Therefore, the proposed keeper circuitry must be designed carefully considering its impact on the performance of the dynamic OR gates.

B. *Performance of a Dynamic* OR *Gate*

To maintain high performance, there are two major factors that should be considered when designing a keeper circuit: first, additional loading caused by the keeper and its control circuitry. Second, the keeper circuit should be capable of switching OFF very fast because longer it remains ON during evaluation, more it will compete with the nMOS pull-down network. Most of the existing keeper designs in the literature either heavily load the OR gate dynamic nodes, or involve control circuitry that respond so slowly that the overall design fails to fully exploit the potential improvements [7], [10].

The proposed keeper in this paper addresses these two issues with its uncomplicated and fast architecture. As shown in Fig. 9, loading wise, this approach only requires two additional connections to the dynamic node. Additionally, the control circuit (process variation sensor) is very fast so that it can shut down the variation-coupled keeper almost instantly, even before the small (fixed) pMOS keeper turns OFF. Precise design and sizing of transistors provide significant performance improvements, as will be discussed in Section IV.

III. Proposed Keeper Circuit

The proposed architecture has three major modules [12]: two keepers, which are called fixed and variation-coupled, and one sensor for process variation [7]. In the following sections, details about the operation of these circuits are presented.

A. *Effect of Process Variation on Dynamic* OR *Gates*

Process variation is generally classified into random and systematic parameter fluctuations [13], [14]. Random variation affects each device individually and independent of other nearby devices. However, in systematic variation, adjacent devices are affected in the same manner and there is a strong correlation between parameters of transistors located in a neighborhood [5]. In this paper, we focus on systematic variation, and hence, it is assumed that threshold voltage of all transistors in a dynamic gate have been altered in the same way. To account for the random variations, which unlike the systematic variations affect each device independently from other transistors, one can target slightly higher noise margin from actual desired UNG level. This noise margin guard bound must be chosen according to the level of random variations at a given technology node. However, note that noise margin overhead is likely to be very low because of two reasons. First, it is known that the impact of random variations is more severe in minimum-sized devices and since transistors of the pull-down network are large, they will not be considerably affected by the random process variations. Second, it is very likely that random variations will affect each device of the pull-down network in a different direction, and therefore, taken as a whole, the impact of random variation on the leakage of the pull-down network will be small due to the averaging effect. However, since the leakage current is exponentially dependent on the threshold voltage, the total leakage current will always

have a tendency to increase (rather than decrease) by a small amount.

B. Process Variation Sensor

The variation sensor [7] used in this paper is based on drain-induced barrier lowering (DIBL) effect, which is known to cause the threshold voltage of a short-channel MOSFET to be modulated by the deviation of drain voltage [16]. In other words, high drain voltage can lower the source-channel barrier so that channel is formed at lower gate voltages (lower threshold voltage). As a result, in a short channel device, assuming all other parameters to be constant, the threshold voltage becomes linearly dependent on the drain voltage. The process variation sensor is shown in Fig. 9, where M_2 is biased using the voltage source $V_{\rm Bias}$ and the current source $I_{\rm REF}$. The role of the bias circuitry is critical here, because it is assumed that the bias condition remains the same over the entire threshold voltage range. Such a process variation insensitive circuitry has been proposed in [17] and used in our keeper circuit. The reference current and voltage generated by the bias circuitry are only a function of the thermal voltage and width of transistors in this circuit, and hence, they are effectively independent of channel length variations. Assuming that bias sources are designed in such a way that they are insensitive to process variations (as will be discussed in following paragraphs), drain voltage of M_2 (node $V_{\rm DIBL}$) will be a linear function of systematic process variations. The interesting point about this sensor is that the drain voltage fluctuations will be approximately tenfold of the threshold voltage fluctuations, as will be discussed in the following sections. Hence, if, for example, the variation increases threshold voltage of M_2 by 50 mV, $V_{\rm DIBL}$ will drop by $\approx$500 mV and *vice versa*. Therefore, one can use this sensor to design circuits to offset the impact of systematic process variation.

As observed in Fig. 2, register files employ more than one OR gates. Since duplicating the entire sensor circuitry for each gate is not efficient, and hence, here, we show how it is possible to reuse the same circuitry to make more independent sensor circuits for multiple gates. It should be noted that the most complicated and area-intensive part of the variation sensor circuitry in Fig. 9 is its current source. The voltage source, as will be discussed here, can be easily constructed once the current source is available.

The sensor circuit in Fig. 9, which is composed of transistor M_2 and current and voltage sources, is re-drawn in Fig. 10(a) along its transistor-level design in Fig. 10(b). The bias current $(I_{\rm Bias})$ is generated using a current source $(I_{\rm REF})$ and a "current mirror," which consists of M_I and M_C. Since both these devices have identical gate-to-source voltages, the current of M_2 is equal to $I_{\rm Bias} = I_{\rm REF} \times ((W/L)_{M_I}/(W/L)_{M_C})$. Utilizing current mirror circuits allows us to use a single current source to generate bias currents for several sensor circuits with minimal circuit overhead (only two transistors). The bias voltage in Fig. 10(a) is implemented using transistors M_V, M_A, and M_B [Fig. 10(b)]. Here, M_V and M_C form a current mirror, where with proper sizing of devices, the bias current of M_A and M_B can set to be $I_{\rm Bias}$. It can be easily shown (refer to the Appendix for details of the derivation) that if M_A and M_B are both biased in the subthreshold region, $V_{\rm Bias}$ is independent of $I_{\rm Bias}$

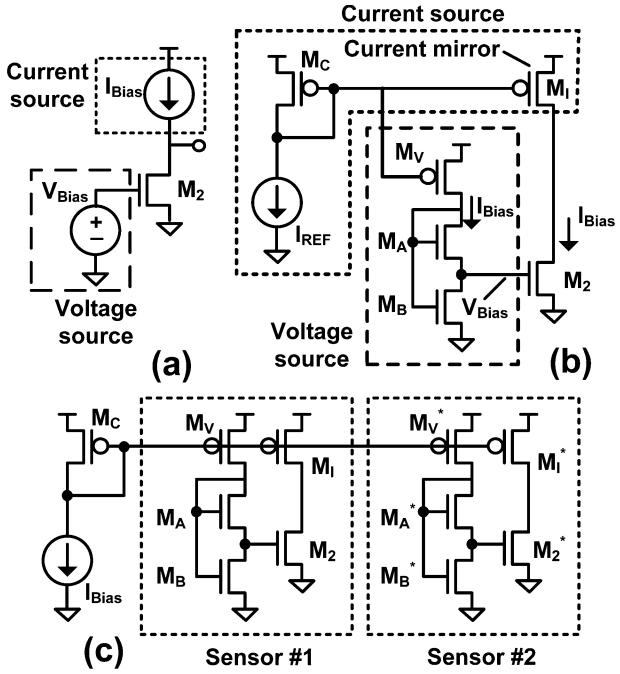

Fig. 10. Circuit implementation of multiple sensors using a single current source. (a) Block diagram schematic of the sensor. (b) Its transistor-level design. (c) Implementation of multiple sensors using a single current source.

value and is equal to $n(kT/q)\times(W_A/W_B)$, where W_A and W_B are the widths of M_A and M_B, respectively. Using current mirrors, it is possible to implement more sensor circuits (which can be used in other OR gates) employing the same current source $(I_{\rm REF})$. Such an approach is as shown in Fig. 10(c) where two identical sensors are realized with minimal design overhead.

It should be noted that, generally, noise generated by digital circuits that propagates through both interconnects and substrate can influence the operation of analog circuits. However, unlike other analog circuits such as A/D or D/A converters, which are extremely sensitive to noise, the operation of the proposed circuit will not be considerably affected by the induced noise. The reason is that, as discussed before, the operation of the bias circuit is effectively a function of fixed parameters $[(kT/q) \times (W_A/W_B)]$ and insensitive to fluctuations induced by either noise or process variation. Furthermore, there are some approaches that can be employed to lower the impact of induced noise. For instance, introducing a capacitor between power and ground lines can reduce "bouncing" effects of supply voltage by providing a high-frequency current path [17].

C. Fixed Keeper

In this section, we derive analytical equation for drive current of the traditional keeper versus $V_{\rm th}$ [$I_1 - V_{\rm th}$ curve in Fig. 8(a)] using circuit configuration shown in Fig. 11. In this figure, it is assumed that voltage of all inputs and the output node is V_{NM} (the condition under which UNG must be measured), and hence, dynamic node (V_X) is approximately at a voltage close to V_{dd}. As a result, one can easily observe that M_1 is operating in its linear region, and consequently, drive current of the fixed pMOS

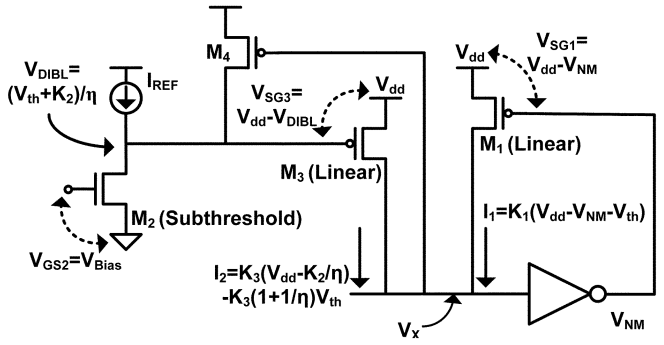

Fig. 11. Analysis of the proposed keeper architecture. Details of derivation of equations are explained in the text. Values of parameters K_1, K_2, and K_3 can be found in (3), (6), and (9), respectively.

keeper (M_1) is approximately a linear function of its threshold voltage

$$I_1 = I_p = \mu_p C_{\rm ox}\left(\frac{W}{L}\right)_{M1}(V_{SG1} + V_{{\rm th}p})(V_{dd} - V_X). \quad (1)$$

Note that in this circuit, voltage difference between gate and source of the pMOS keeper (M_1) is a constant value, because this equation is derived under condition specified by definition of UNG. Therefore, assuming $V_{SG1} = V_{dd} - V_{NM}$ and $V_{{\rm th}p} = -V_{\rm th}$, (1) can be rewritten as

$$I_1 = K_1(V_{dd} - V_{NM}) - K_1 V_{\rm th} \quad (2)$$

$$K_1 = \mu_p C_{\rm ox}\left(\frac{W}{L}\right)_{M1}(V_{dd} - V_X) \quad (3)$$

and V_{NM} is the noise margin level. Equation (2) justifies the situation where increasing the size of the pMOS device to meet the minimum required current level at $V_{\rm th0} - 3\sigma$ also raises its current around $V_{\rm th0} + 3\sigma$ [Fig. 7(a)].

D. Variation-Coupled Keeper

In this section, we derive current curve [$I_2 - V_{\rm th}$ curve in Fig. 8(a)] of the variation-coupled keeper. The proposed architecture (Fig. 11) is designed so that only M_3 or M_4 is conducting at a given time. If the dynamic node is high, M_4 is OFF and the gate of M_3 is controlled by the drain voltage of M_2. Whenever dynamic node switches from high to low, M_4 turns ON, pulling up gate voltage of M_3 and turning it OFF. Note that M_2 is in its subthreshold region, and hence, M_4 can easily lift up gate voltage of M_3. When this keeper is conducting, the gate of M_3 is controlled by the drain voltage of M_2. Therefore, to find drain current of $M_3(I_2)$, first, we need to derive an equation for drain voltage of M_2. Since $V_{\rm Bias}$ is chosen to be less than the threshold voltage of M_2, this transistor is in the subthreshold region. Subthreshold leakage current for a MOSFET can be modeled as [15]

$$I_{ds} = \mu_n C_{\rm ox}\frac{W}{L}V_T^2 e^{\frac{V_{gs_2} - (V_{\rm th} - \eta V_{ds})}{nV_T}} \quad (4)$$

where μ_n is the effective mobility, $C_{\rm ox}$ is the gate-oxide capacitance, L is the effective channel length, W is the effective width, V_T is the thermal voltage, $V_{\rm th}$ is the threshold voltage of transistor, and η is the DIBL constant. Since current of $I_{\rm REF}$ is independent of process variations, all of the parameters in (4) are constant except for $V_{\rm th}$ and V_{ds} (which is $V_{\rm DIBL}$ in Fig. 11).

It should be noted that the channel length variation results in fluctuation of several electrical properties of the CMOS devices such as threshold voltage and gate capacitance. However, the dominant effect of this variation is considered to be the threshold voltage fluctuations. Therefore, gate capacitance fluctuations caused by channel length variation is neglected in this paper due to its less important effects (note that the gate capacitance varies linearly with the channel length whereas subthreshold leakage is an exponential function of the channel length). Moreover, the transistors in the pull-down network are always sized to be relatively large (say, $W/L = 5$) to achieve faster switching speed. Therefore, assuming the same level of variation in the length and width of the devices $(\Delta W = \Delta L)$, the percentage variation in the width $(\Delta W/W)$ is significantly smaller than the percentage fluctuation in the length $(\Delta L/L)$ due to the fact that $W \gg L$; hence, the width variation can be neglected. Therefore, the only significant source of variation is the threshold voltage fluctuations. Hence, according to (4), any variation in threshold voltage of M_2 can only be compensated by deviation of V_{ds}. $V_{\rm DIBL}$ can be obtained in terms of other parameters from (4)

$$V_{ds} = V_{\rm DIBL} = \frac{1}{\eta}(V_{\rm th} + K_2) \quad (5)$$

where

$$K_2 = nV_T \ln\left(\frac{I_{\rm Bias}}{\mu_n C_{\rm ox}\left(\frac{W}{L}\right)_{M2} V_T^2}\right) - V_{\rm Bias}. \quad (6)$$

We know that gate–source voltage of M_3 is the voltage difference between V_{DD} and DIBL nodes; therefore, $V_{GS3} = V_{ds} - V_{DD}$ and also $V_{{\rm th}p} = -V_{\rm th}$. As a result, current characteristics of variation-coupled keeper (I_2) can be easily obtained as

$$I_2 = I_p = \mu_p C_{\rm ox}\left(\frac{W}{L}\right)_{M3}(V_{SG3} + V_{{\rm th}p})(V_{dd} - V_X) \quad (7)$$

$$I_2 = K_3\left(V_{dd} - \frac{K_2}{\eta}\right) - K_3\left(1 + \frac{1}{\eta}\right)V_{\rm th} \quad (8)$$

where

$$K_3 = \mu_p C_{\rm ox}\left(\frac{W}{L}\right)_{M3}(V_{dd} - V_X). \quad (9)$$

Equation (8) is very interesting because it presents a straight line in $I_2 - V_{\rm th}$ plane and that its intersection with $V_{\rm th}$ axis (function of M_2's size, $V_{\rm Bias}$, and $I_{\rm Bias}$) and its slope (function of M_3's size) are entirely independent.

E. Keeper Design Framework

The value of V_0 (Fig. 8) is one of the design parameters that can be chosen independently from the rest of the design parameters as long as it is reasonably located somewhere between $V_{\rm th0} - 3\sigma$ and $V_{\rm th0} + 3\sigma$. In this paper, V_0 is set to be exactly in the middle of this range or at the nominal $V_{\rm th}$. Also, M_4 should be minimum sized in order to ensure smallest possible loading

[1][Online]. Available: http://www.eas.asu.edu/~ptm/

on the dynamic node. The size of M_1 must be chosen [using (1)–(3)] so that fixed keeper [I_1 in Fig. 8(a)] can maintain minimum required current over $V_{\rm th}$ spread from $V_{\rm th0}$ to $V_{\rm th0}+3\sigma$ as the variation coupled keeper is OFF in this range $(I_2 = 0)$. Consequently, size of M_2, $V_{\rm Bias}$, and $I_{\rm REF}$ should be chosen [using (5) and (6)] such that the variation-coupled keeper remains OFF from $V_{\rm th0}$ to $V_{\rm th0} + 3\sigma$ and conducts only for the rest of the threshold voltage range. Finally, M_3 should be chosen [using (7)–(9)] such that the total current of two keepers $(I_1 + I_2)$ stays above minimum required current in $V_{\rm th}$ range from $V_{\rm th0} - 3\sigma$ to $V_{\rm th0}$ [Fig. 8(a)].

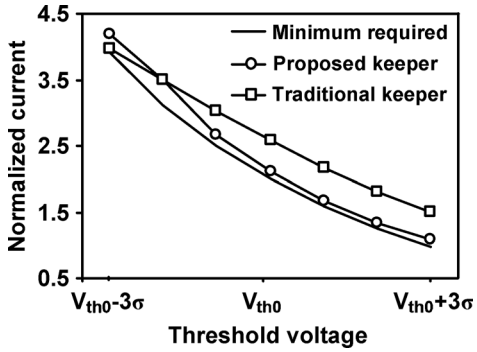

Fig. 12. Minimum required current for an eight-input dynamic OR gate compared to the currents of proposed and traditional keepers.

IV. Implementation and Results

To study its relative performance in terms of delay and power consumption, the proposed keeper is compared to the traditional circuit and three existing works in the literature (Fig. 4) using HSPICE simulations. To model the process variation (which, in this paper, is considered to be only due to the systematic channel length variations), $V_{\rm th}$ parameters for both nMOS and pMOS in the HSPICE models are varied together in the same direction. For instance, if the nMOS transistors have 3σ higher $V_{\rm th}$ values, the threshold voltage of pMOS devices are also increased by the same amount. Three metrics are used for comparison: 1) the mean value of the worst-case delay $(\mu_{\rm Delay})$; 2) standard deviation of the worst-case delay $(\sigma_{\rm Delay})$; and 3) the mean value of power consumption. We have used PTM models[1] for 90 nm technology with $V_{dd} = 1$ V, temperature of 110 °C, and $\rm UNG = 0.2$ V for all simulations. Other than Fig. 13, all simulations were carried out for eight-input dynamic OR gates. As per [14], standard deviation of $V_{\rm th}(\sigma_{V_{\rm th}})$ is assumed to be 5% of nominal $V_{\rm th}(\mu_{V_{\rm th}})$ for all simulations, except for Table II and Fig. 17, in which we vary $\sigma_{V_{\rm th}}$ values.

Fig. 12 shows the minimum required current along with current supplied by the traditional and proposed keepers for an eight-input dynamic OR gate. Vertical and horizontal axes are normalized current and threshold voltage, respectively. Fig. 12 agrees with the sketched curves presented in Fig. 7, where the traditional keeper has a linear behavior and the proposed circuit provides a nonlinear supply current. This figure suggests that the new keeper creates less contention over almost the entire variation range especially around nominal $V_{\rm th}(V_{\rm th0})$ and values higher than that. Also, it can be seen that the proposed keeper supplies slightly more current than the traditional circuit around $V_{\rm th0} - 3\sigma$ region.

Superior performance of both 8- and 16-input dynamic OR gates, which employ the proposed keeper, over gates with the traditional keeper is shown in Fig. 13. In this figure, the *y*-axis is normalized worst-case delay and the *x*-axis shows $V_{\rm th}$. Due to lower contention, for both 8- and 16-input OR gates, over almost the entire range of the $V_{\rm th}$ variation, the new keeper offers higher performance. Only in a small region around $V_{\rm th0} - 3\sigma$, our circuit exhibits slightly higher delay because of higher contention there, as could be predicted from Fig. 12. Moreover, over the entire $V_{\rm th}$ spread, worst-case delay of the proposed OR gates roughly remains constant and exhibits less variation compared to that of the traditional circuit, which can be considered as higher robustness to process variation. Note that the advantage of the proposed circuit increases with width of OR gate.

To further demonstrate the efficiency of our approach, four existing keeper designs from the literature (shown in Fig. 4) have been simulated along with the proposed and traditional keeper. Alvandpour *et al.* [8] [Fig. 4(b)] split the keeper into two parts so that, in the evaluation phase, the first part is always ON and the second component turns ON with a delay, resulting in reduced contention. Kim *et al.* [10] [Fig. 4(c)] uses a 3-bit digital input to adjust keeper strength according to the process variation. Krishnamurthy *et al.* [6] [Fig. 4(d)] tries to decrease leakage current through reengineering of the nMOS pull-down network. Finally, Kursun and Friedman [11] [Fig. 4(f)] have proposed a circuit to lower the contention between the keeper and the pull-down network by body bias tuning of the keeper transistor.

Figs. 14 and 15 show normalized delay and power consumption of the aforementioned five circuits over the entire spread of $V_{\rm th}$. Table I lists transistor sizes used for simulations of various circuits. All transistors are sized so that all OR gates offer the same noise margin of 0.2 V under the process variation of $\sigma_{V_{\rm th}} = 5\%\ \mu_{V_{\rm th}}$. Different transistors are referred by their corresponding numbers from Fig. 9 for the proposed work and from Fig. 4 for the rest of the circuits. The pull-down nMOS network transistors in all the designs (including the proposed circuit) have W/L ratio of 5 and bias circuitry for the proposed keeper is chosen to be $I_{\rm REF} = 5\ \mu$A and $V_{\rm Bias} = 0.2$ V.

Fig. 14 suggests that the proposed architecture has lowest delay over almost the entire range of $V_{\rm th}$ variation. Although implementation of [9] exhibits less delay around the $V_{\rm th0} - 3\sigma$ region, our keeper offers lower delay around $V_{\rm th0}$, which is of higher interest because, statistically, majority of transistors fall into this category. It should also be noted that the circuit of [6] is designed to be of very low power, and consequently, it has high latency.

Fig. 15 shows normalized power consumption of simulated circuits. In this simulation, power consumption of the process variation sensor as well as the bias circuitry is considered for all implementations. It can be observed that for most part of the $V_{\rm th}$ variation range, the new keeper performs better than the traditional keeper and those presented in [7] and [10]. Only the keeper of [6] has lower power consumption, which comes at the cost of its very low speed, as pointed out in Fig. 14.

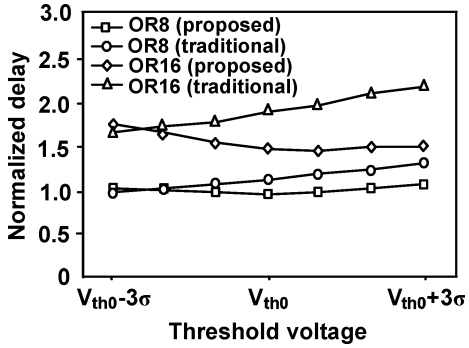

Fig. 13. Performance comparison between 8- and 16-input dynamic OR gates with proposed and traditional keeper circuits.

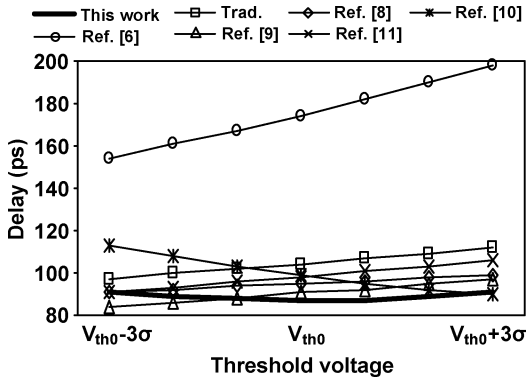

Fig. 14. Comparison of mean delay versus threshold voltage between eight-input OR gates with proposed keeper and previous works.

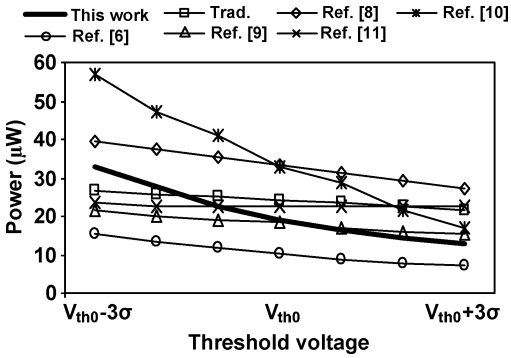

Fig. 15. Comparison of power consumption versus threshold voltage for eight-input OR gates with proposed keeper and previous works.

TABLE I
SIZING OF TRANSISTORS USED FOR SIMULATION OF DIFFERENT CIRCUITS

This work	W/L(M_1)=1.5, W/L(M_2)=2, W/L(M_3)=2 and W/L(M_4)=1
Trad.	W/L(M_1)=2.5
Ref. [6]	W/L(M_1)=0.25
Ref. [8]	W/L(M_1)=1.5 and W/L(M_2)=1.5
Ref. [9]	W/L(M_1)=3
Ref. [10]	W/L(M_1)=0.5, W/L(M_2)=1 and W/L(M_3)=2
Ref. [11]	W/L(M_1)=3

Since all of the proposed keepers in the literature employ extra circuitry to improve the performance of the dynamic gates, the area overhead of these circuits can be compared to that of a dynamic gate with the traditional keeper. Fig. 16 presents such a

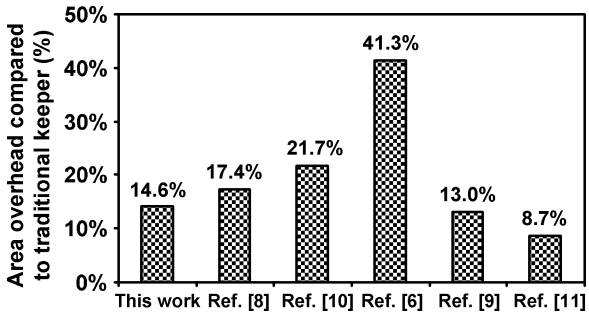

Fig. 16. Area overhead of dynamic gates with the proposed keeper and other low-power keeper architectures compared to area of a traditional dynamic gate.

TABLE II
COMPARISON BETWEEN MEAN DELAY, STANDARD DEVIATION OF DELAY, AND POWER CONSUMPTION FOR PROPOSED KEEPER AND PREVIOUS WORKS

variation	Variable	This work	Trad.	Ref. [6]	Ref. [8]	Ref. [9]	Ref. [10]	Ref. [11]
σ_{Vth}= 1% μ_{Vth}	Power (μW)	**86.8**	**104.3**	**174.2**	**94.9**	**90.1**	**100.5**	**98.2**
	μ_{Delay} (ps)	**0.2**	**1.0**	**3.1**	**0.6**	**0.9**	**12.3**	**1.1**
	σ_{Delay} (ps)	**18.9**	**24.2**	**10.2**	**33.1**	**17.7**	**34.1**	**22.1**
σ_{Vth}= 3% μ_{Vth}	Power (μW)	**87.7**	**104.4**	**174.5**	**94.9**	**90.2**	**100.3**	**98.3**
	μ_{Delay} (ps)	**0.9**	**3.1**	**9.4**	**1.8**	**2.8**	**10.4**	**3.4**
	σ_{Delay} (ps)	**19.7**	**24.2**	**10.4**	**33.2**	**16.2**	**34.5**	**22.3**
σ_{Vth}= 5% μ_{Vth}	Power (μW)	**88.7**	**104.4**	**175.1**	**94.9**	**90.3**	**100.1**	**98.3**
	μ_{Delay} (ps)	**1.6**	**5.1**	**15.7**	**3.0**	**4.8**	**8.6**	**5.6**
	σ_{Delay} (ps)	**20.8**	**24.2**	**10.7**	**33.2**	**18.1**	**35.0**	**22.5**
σ_{Vth}= 7% μ_{Vth}	Power (μW)	**89.6**	**104.6**	**176.0**	**94.9**	**90.6**	**100.0**	**98.3**
	μ_{Delay} (ps)	**2.1**	**7.2**	**22.1**	**4.3**	**6.7**	**6.7**	**7.8**
	σ_{Delay} (ps)	**21.8**	**24.2**	**11.0**	**33.3**	**18.4**	**35.5**	**22.7**
σ_{Vth}= 10% μ_{Vth}	Power(μW)	**90.4**	**104.9**	**177.9**	**95.1**	**91.1**	**99.7**	**98.4**
	μ_{Delay} (ps)	**3.5**	**10.4**	**32.1**	**6.5**	**9.8**	**3.9**	**10.9**
	σ_{Delay} (ps)	**22.8**	**24.1**	**11.6**	**33.5**	**19.0**	**36.2**	**22.9**

comparison where it can be observed that the proposed keeper in this paper has only ≈14.6% area overhead. In aforementioned calculations, both for our work and the approach in [11], it is assumed that the bias circuitry is shared among five dynamic gates, because, as discussed previously, the bias circuitry can be used jointly for several dynamic gates. Although the proposed approach has slightly higher area overhead than those approaches in [9] and [11], it should be noted that for dynamic gates, more important concerns are noise margin and switching delay, and hence, higher area overhead is easily justified if the reliability and performance gains are substantial (as in case of the proposed keeper).

In order to capture the impact of increasing process variation, we have simulated five different dynamic OR gates under different levels of the variations. The results are shown in Table II where threshold variations are set to be $\sigma_{V_{\rm th}} = 1\%$, 3%, 5%, 7%, and 10% $\mu_{V_{\rm th}}$. The mean value and standard deviation of delay along with power consumption values are shown in this table. It can be observed that the mean value of delay for the proposed design is the smallest for variation levels higher than $\sigma_{V_{\rm th}} = 5\%\ \mu_{V_{\rm th}}$. The proposed architecture is also superior in terms of power consumption compared to all other circuits except for the one proposed in [6], which also has low performance. More importantly, the fluctuation (standard deviation)

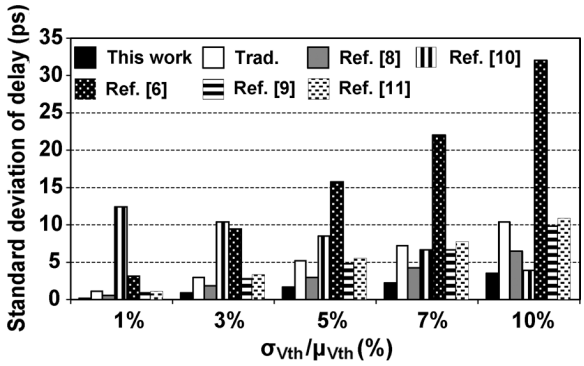

Fig. 17. Standard deviation of delay of the proposed architecture compared to other keeper circuits under different levels of process variation.

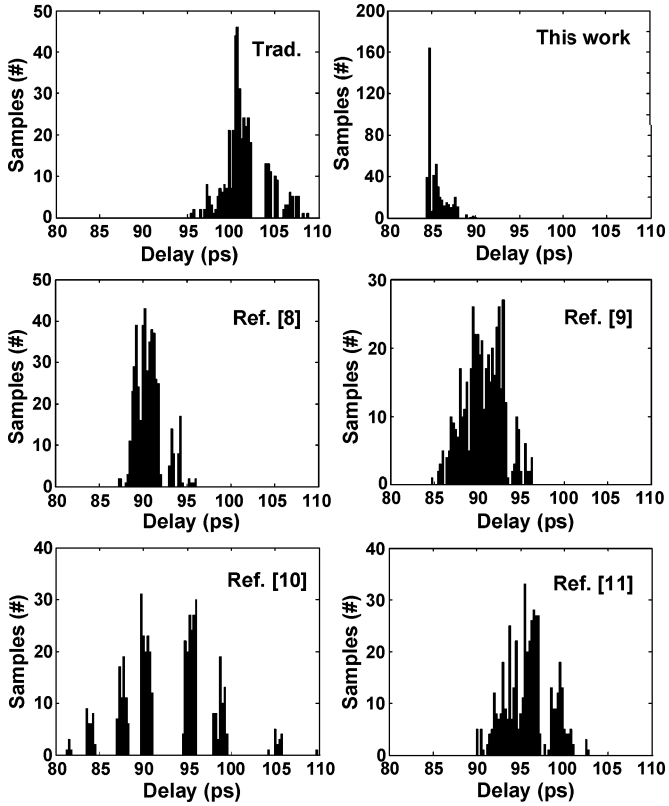

Fig. 18. Delay distribution for traditional, proposed and four previous works, obtained from Monte Carlo simulations.

of delay is the lowest for the new keeper architecture, which essentially shows that the proposed circuit is more robust against the impact of process variations. From Table II, we have plotted the data related to standard deviation, as shown in Fig. 17. As it can be observed from this figure, standard deviation of delay of the proposed keeper is extremely low under all levels of process variations. Therefore, one can conclude that the proposed keeper is the most variation tolerant among all simulated circuits. This is also shown in Fig. 18 through a delay distribution obtained from Monte Carlo simulations of 500 samples. As can be observed, distribution of delay for the new keeper is both shifted to the left (lower delay) and is narrower (lower deviation).

V. Conclusion

A novel variation-tolerant keeper architecture is proposed for wide fan-in dynamic OR gates that achieves higher performance and as well as lower power consumption compared to traditional approaches. The motivation for the new design is derived from a graphical representation of the tradeoff between noise margin and performance of dynamic gates. Using this representation, it is demonstrated that the conventional keeper circuit generates unnecessary excess contention, which results in high power consumption and performance penalty. A novel two-stage keeper is proposed to lower this excess contention. Using HSPICE simulation, it has been shown that in presence of 15% $V_{\rm th}$ fluctuations, the proposed architecture can achieve 20%, 15%, and more than 40% reduction in power consumption, mean delay, and standard deviation of delay, respectively, compared to the traditional keeper. More importantly, it is shown that the advantage of the proposed circuit increases with width of OR gate. This architecture also offers the smallest delay deviation for the entire $V_{\rm th}$ range considered in this study, compared to all existing works in the literature, and hence, it is the most variation tolerant among the proposed architectures. Also, among high-performance designs, its power consumption is the lowest. Results of Monte Carlo simulations suggest that delay distribution for gates that employ the proposed keeper have both lower mean delay and deviation. Hence, the proposed keeper architecture could be very effective in increasing the robustness of dynamic gates to process variations.

Appendix

In this Appendix, we show that the bias voltage ($V_{\rm Bias}$) in Fig. 10 is independent of process variation. We assume that both transistors M_A and M_B are biased using the current source $I_{\rm REF}$ such that both of them operate in the subthreshold region. Therefore, subthreshold leakage current of these devices can be modeled as [15]

$$I_{\rm Bias} = \mu_n C_{\rm ox}\left(\frac{W}{L}\right)_A V_T^2 e^{\frac{V_{gs_A}-\left(V_{\rm th}-\eta V_{ds_A}\right)}{nV_T}} = \mu_n C_{ox}\left(\frac{W}{L}\right)_B V_T^2 e^{\frac{V_{gs_B}-\left(V_{\rm th}-\eta V_{ds_B}\right)}{nV_T}} \quad (10)$$

where μ_n is the effective mobility, $C_{\rm ox}$ is the gate-oxide capacitance, V_T is the thermal voltage, $V_{\rm th}$ is the threshold voltage of devices, and η is the DIBL constant. Also, $(W/L)_A, (W/L)_B$; V_{gsA}, V_{gsB}; and V_{DSA}, V_{DSB} pairs represent sizing ratio, gate–source, and drain–source voltage differences of M_A and M_B, respectively. Ignoring the DIBL effect ($\eta = 0$) for simplicity, one can get

$$\left(\frac{W}{L}\right)_A e^{\frac{V_{gs_A}-V_{\rm th}}{nV_T}} = \left(\frac{W}{L}\right)_B e^{\frac{V_{gs_B}-V_{\rm th}}{nV_T}} \quad (11)$$

or

$$e^{\frac{V_{gs_A}-V_{\rm th}}{nV_T}-\frac{V_{gs_B}-V_{\rm th}}{nV_T}} = \frac{(W/L)_B}{(W/L)_A}. \quad (12)$$

Taking natural logarithm and knowing that $L_A = L_B$

$$\frac{V_{gs_A} - V_{gs_B}}{nV_T} = \ln\left(\frac{(W/L)_B}{(W/L)_A}\right) = \ln(W_B/W_A). \quad (13)$$

Also, from circuit schematic (Fig. 10), we have

$$V_{gs_A} + V_{ds_B} = V_{gs_B} \Rightarrow V_{gs_A} - V_{gs_B} = -V_{ds_B} = -V_{\text{Bias}}. \quad (14)$$

Substituting this result into (13), we get

$$\frac{-V_{\text{Bias}}}{nV_T} = \ln(W_B/W_A) \Rightarrow V_{\text{Bias}} = nV_T \times \ln(W_A/W_B). \quad (15)$$

Therefore, V_{Bias} is independent of the I_{Bias} value and is equal to $nV_T \times ln(W_A/W_B)$, where W_A/W_B is only a function of the sizing of M_A and M_B.

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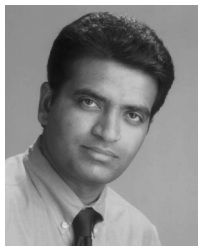

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