A New Paradigm in the Design of Energy-Efficient Digital Circuits Using Laterally-Actuated Double-Gate NEMS

Hamed F. Dadgour, Muhammad M. Hussain* and Kaustav Banerjee
Department of Electrical and Computer Engineering, University of California, Santa Barbara,
{hamed, kaustav}@ece.ucsb.edu
*King Abdullah University of Science and Technology, Thuwal, Saudi Arabia,
muhammad.hussain@kaust.edu.sa

ABSTRACT

Nano-Electro-Mechanical Switches (NEMS) offer the prospect of improved energy-efficiency in digital circuits due to their near-zero subthreshold leakage and extremely low subthreshold swing values. Among the different approaches of implementing NEMS, laterally-actuated double-gate NEMS devices have attracted much attention as they provide unique and exciting circuit design opportunities. For instance, this paper demonstrates that compact XOR/XNOR gates can be implemented using only two such NEMS transistors. While this in itself is a major improvement, its implications for minimizing Boolean functions using Karnaugh maps (K-maps) are even more significant. In the standard K-map technique, which is used in digital circuit design, adjacent "1s" (minterms) are grouped only in horizontal and/or vertical directions; the diagonal (or zig-zag) grouping of adjacent "1s" is not an option due to the absence of compact XOR/XNOR gates. However, this work demonstrates, for the first time ever, that in lateral double-gate NEMS-based circuits, grouping of minterms is possible in horizontal and vertical as well as diagonal fashions. This is because the diagonal groupings of minterms require XOR/XNOR operations, which are available in such NEMS-based circuits at minimal costs. This novel design paradigm facilitates more compact implementations of Boolean functions and thus, considerably improves their energy-efficiency. For example, a lateral NEMS-based full-adder is implemented using less than half the number of transistors, which is required by a CMOS-based full-adder. Furthermore, circuit simulations are performed to evaluate the energy-efficiencies of the NEMS-based 32-bit carry-save adders compared to their standard CMOS-based counterparts.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced technologies*.

General Terms: Performance, Design and Reliability.

Keywords: Boolean Logic Minimization, Energy-efficient Electronics, Laterally-Actuated NEMS, Nanoelectromechanical Switches, XOR gates.

1. INTRODUCTION

A significant increase in the subthreshold leakage current of devices has emerged as one of the most difficult challenges facing CMOS scaling [1]. Attempts to improve the subthreshold performance (lowering the subthreshold swing) of CMOS devices has been overshadowed by the fact that the subthreshold swing of bulk CMOS transistors has a fundamental lower limit of 60mV/decade [2]. As a result, non-classical semiconductor devices, which are capable of offering steeper subthreshold slopes have been explored in the recent years. Among these emerging devices are NEMS transistors that can exhibit an incredibly low subthreshold swing of 2mV/decade [3]. NEMS have generated a great amount of interest for their extraordinary subthreshold characteristics and have been considered for energy-efficient circuit design [4]-[9]. Co-integration of NEMS and CMOS devices on the same die, a hybrid NEMS-CMOS approach, has been proposed in [7], [10] and implemented in [11]. Moreover, several groups have performed scaling analysis to identify key challenges of MEMS integration in the future ultra low-power IC design applications [12]-[14].

While there are several approaches to implement NEMS devices [15]-[19], laterally-actuated double-electrode NEMS offer certain advantages over other existing NEMS structures [8]. For instance, vertical NEMS switches suffer from impact bouncing and a long settling time due to release vibrations [20]. These shortcomings can be significantly overcome by using lateral devices as will be discussed later. Additionally, the existence of two gate terminals that can be controlled independently makes double-gate structures attractive choices for the implementation of compact logic gates. Therefore, in this work, laterally-actuated double-gate NEMS are considered for the design of various digital circuits.

In the recent years, numerous NEMS devices have been simulated [19]-[22], and fabricated [23]-[25] by various groups. However, circuit design opportunities using such devices have not been fully explored. Since NEMS transistors operate quite differently from CMOS devices, it is important to investigate the circuit-level implications of employing such transistors. For example, this paper demonstrates the implementation of compact XOR/XNOR gates by utilizing the exclusive properties of laterally-actuated double-gate NEMS. More importantly, this work demonstrates, for the first time ever, that the availability of such compact XOR/XNOR gates has significant implications for minimizing Boolean functions.

Traditionally, Boolean functions (up to six variables) can be easily simplified using K-maps where adjacent "1s" are grouped together only in horizontal and/or vertical directions. In the standard K-map approach, the diagonal (zig-zag) grouping of "1s" is not an option because the hardware implementation of such a grouping requires an XOR or XNOR function. Since CMOS-based XOR/XNOR gates are power- and area- expensive, the diagonal grouping of minterms is not an energy-optimal choice in this case. In contrast, XOR/XNOR gates can be efficiently implemented using lateral NEMS devices and as a result, diagonal (zig-zag) as well as horizontal and vertical groupings of "1s" are possible. This additional "degree of freedom" introduces a new design paradigm where logic functions can be implemented using fewer transistors. For instance, as shown in this paper, a NEMS-based full-adder can be implemented using less than half the number of transistors required by its CMOS counterpart.

In summary, this paper contributes to the literature by introducing a new logic minimization paradigm for NEMS-based digital circuits. The proposed approach utilizes the availability of compact XOR/XNOR gates to perform diagonal as well as vertical and horizontal groupings of "1s" in K-maps. Using this method, Boolean functions can be implemented with fewer devices.

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Therefore, the combined effect of fewer required devices and the inherent low-power properties of NEMS transistors improves the energy-efficiency of NEMS-based logic circuits. Note that the reliability issues associated with the operation of scaled NEMS are currently under investigation; however, they are beyond the scope of this work.

This paper is organized as follows. Section 2 provides an overview on the device structure and its operation. Section 3 introduces the novel XOR/XNOR designs, which are used in Section 4 to develop the new logic minimization paradigm proposed in this work. Section 5 presents circuit simulations to evaluate the energy-efficiency gains achieved by employing the proposed method and the last section concludes this paper.

2. LATERALLY-ACTUATED DOUBLE-GATE NEMS

2.1 Device Structure and Operation Principle

The SEM picture of a fabricated transistor along with the schematics of a lateral NEMS device is shown in **Fig. 1**. The CMOS compatible process steps, which are employed for fabrication of these devices are reported in [8]. The top-view schematic of the device (**Fig. 1 (b)**) corresponds to the SEM picture shown in **Fig. 1 (a)**. Similarly, the sketch shown in **Fig. 1 (c)** provides a cross-sectional view of the transistor. This device has two gate terminals (Gate A & Gate B in **Fig. 1 (a)**), which are controlled independently. The basic operation of the device is illustrated in **Fig. 2** where, by applying a bias voltage between one of the gates (for example, Gate A) and the source (Gate B is biased at the same voltage as the source), opposite charges appear on the beam and the corresponding gate terminal, generating an electrostatic force. If the gate voltage is smaller than a threshold value ($V_{pull\text{-}in}$), as shown in **Fig. 2 (a)**, the beam bends slightly, but does not touch the drain terminal. However, if the bias voltage is larger than $V_{pull\text{-}in}$, the beam deflects sufficiently to touch the drain and hence, creates a conduction path from the source to the drain as shown in **Fig. 2 (b)**.

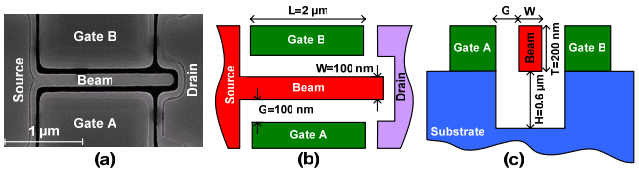

Fig. 1. A laterally-actuated double-gate NEMS device [8]: (a) SEM picture of the fabricated device, (b) schematic of the top-view and (c) the side-view schematic. Typical values of the different dimensions of the structure are also shown here.

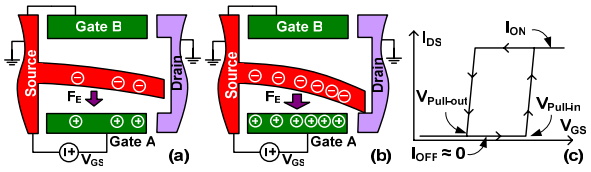

Fig. 2. The basic operation of laterally-actuated NEMS: (a) when $V_{GS} < V_{pull\text{-}in}$, (b) when $V_{GS} > V_{pull\text{-}in}$, and (c) I_{DS}-V_{GS} characteristics of the device.

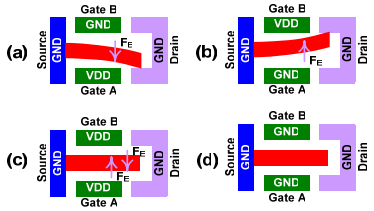

Fig. 3. The operation of a NEMS for various bias conditions: (a) Gate A = VDD and Gate B = GND, (b) Gate A = GND and Gate B = VDD, (c) Gate A = VDD and Gate B = VDD and (d) Gate A = GND and Gate B = GND.

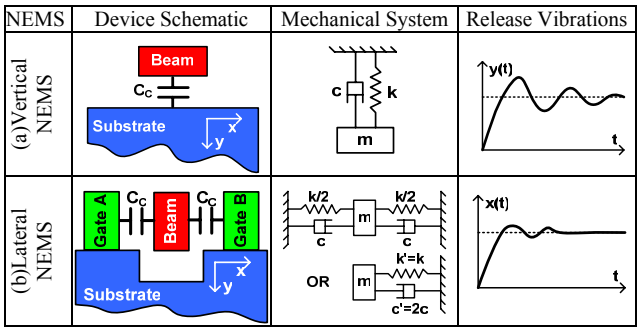

Fig. 4. Switching behavior of (a) vertically- and (b) laterally-actuated NEMS. Cc is the coupling capacitance between the gate and the beam.

A sketch of the typical I_{DS}-V_{GS} characteristics of such a device is presented in **Fig. 2 (c)** where I_{DS} denotes the source-drain current and V_{GS} refers to the gate-source voltage difference. It can be observed that the device exhibits a hysteresis behavior, which is because of the existence of surface forces that prevent the beam from being restored to its original position once it is pulled down [26]. As a result of this hysteresis, if V_{GS} is increased gradually from zero, there is virtually zero OFF current for $V_{GS} < V_{pull\text{-}in}$ and the device turns ON when $V_{GS} > V_{pull\text{-}in}$. In contrast, while decreasing V_{GS} value from $V_{pull\text{-}in}$, for $V_{GS} > V_{pull\text{-}out}$, the device remains ON and it only turns OFF for $V_{GS} < V_{pull\text{-}out}$. The operation of a NEMS device under all possible input combinations are illustrated in **Fig. 3** (details of $V_{pull\text{-}in}$ and $V_{pull\text{-}out}$ model can be found in [8]) where it is assumed that the source terminal is always connected to the ground. It is also assumed that VDD is larger than $V_{pull\text{-}in}$. When Gate A is connected to the power supply (Gate A = VDD) and Gate B is tied to the ground (Gate B = GND), there will be an attractive electrostatic force (F_E) between the beam and Gate A (**Fig. 3 (a)**). Hence, the source and the drain will be connected (Note that since the source and Gate B are at the same voltage (GND), there is no attractive force between them. A similar scenario occurs when Gate A = GND and Gate B = VDD (**Fig. 3 (b)**); the only difference is that in this case the attractive force is created between Gate B and the beam. If Gate A and Gate B are connected to VDD, both gate terminals create equally strong electrostatic forces. Since these two forces are in the opposite directions, the beam will not be deflected (**Fig. 3 (c)**). Finally, when Gate A = GND and Gate B = GND, the beam will not be bent due to the absence of any electrostatic force between the terminals.

2.2 Comparison between Lateral and Vertical Devices

The vertically-actuated cantilever switches are among the most common structures used for the implementation of NEMS [27]-[30]. However, it has been shown that the vertical NEM switches with single actuation electrode (gate) suffer from impact bouncing and a long settling time due to release vibrations [31] as illustrated in **Fig. 4 (a)**. The reason can be explained by considering the equivalent mechanical models of such devices, which consist of the beam's mass (m), a damping factor (c) and a spring constant (k). Note that the damping factor represents the viscosity of the air molecules that reside between the beam and the substrate/gate and the spring constant stands for the elasticity of the beam. The settling time of the vertical NEMS is longer due to the smaller damping factor (c) compared to that of the lateral NEMS (2c). This is because the vibrations of the lateral beam are dampened twice as fast by the air molecules that exist in between the beam and the two gates. Another advantage of the laterally-actuated NEMS is the availability of two gate terminals. Such a structure provides one more degree of freedom, which can be exploited for the design of compact logic circuits as will be discussed in the subsequent sections.

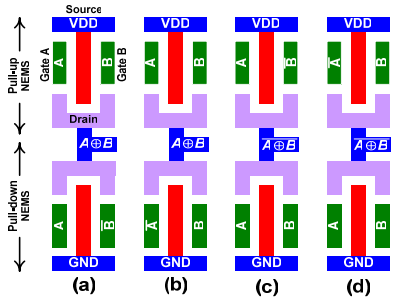

Fig. 5. Two equivalent designs for NEMS-based (a)-(b) XOR and (c)-(d) XNOR gates.

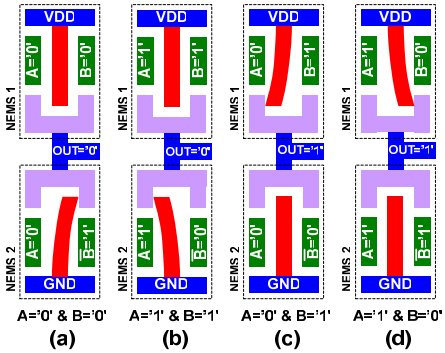

Fig. 6. The operation of the XOR gate shown in **Fig. 3(a)** under various input combinations.

3. COMPACT XOR/XNOR GATES USING NEMS

The existence of two gate terminals, which can be controlled independently offers higher flexibility and provides the prospects of designing interesting structures using NEMS devices. For instance, as shown in **Fig. 5**, an XOR/XNOR logic gate can be implemented using only two NEMS transistors. Note that the CMOS implementations of XOR/XNOR gates require at least eight transistors. The circuits shown in **Fig. 5 (a)-(b)** represent two alternative implementations of XOR gates while **Fig. 5 (c)-(d)** depict two possible XNOR architectures. In these figures, A and B denote the input signals and the output nodes are identified by their corresponding Boolean symbols (e.g., $A \oplus B$). Here, the output nodes are formed by connecting the drain terminals of pull-up and pull-down NEMS. Furthermore, the source terminal of the pull-up/pull-down NEMS is connected to VDD/GND. Note that the only difference between the two XOR designs is that in **Fig. 5 (a)**, the gate terminals of the pull-down NEMS are connected to A and B while in **Fig. 5 (b)**, they are tied to B and A . Also, in the XNOR implementation shown in **Fig. 5 (c)**, the gate terminals of the pull-up NEMS are connected to A and B while in **Fig. 5 (d)**, they are tied to B and A .

Fig. 6 illustrates the basic operation of the XOR gate proposed in **Fig. 5 (a)** considering all possible input combinations. In this circuit, NEMS1 remains OFF when AB="00" or AB="11", whereas NEMS2 turns ON and connects the output to GND as shown in **Fig. 6 (a)** and **Fig. 6 (b)**, respectively. Such an operation can be expected according to the description presented in **Fig. 3**. When A=B='0', both gate terminals generate equally strong electrostatic forces, but in the opposite directions and thus, NEMS1 remains OFF. On the other hand, when A=B='1', NEMS1 is OFF, because there is no electrostatic attraction between NEMS1's beam and its two gates. However, when AB="01" or AB="10", NEMS1 becomes ON and NEMS2 turns OFF. Therefore, OUT is connected to VDD as shown in **Fig. 6 (c)** and **Fig. 6 (d)**, respectively.

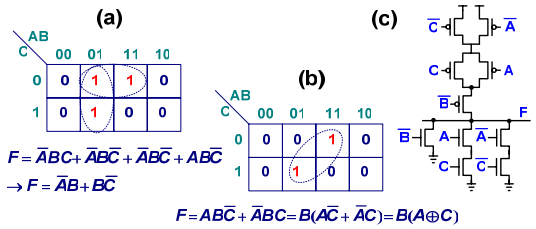

Fig. 7. Grouping of "1s" in: (a) a standard K-map, (b) a Boolean function requiring diagonal grouping and its (c) transistor-level implementation.

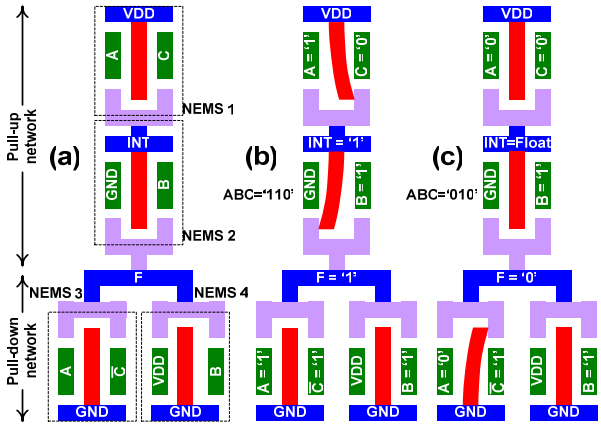

Fig. 8. (a) NEMS-based design of the K-map shown in **Fig. 7 (b)** and its operation assuming (b) ABC="110" and (c) ABC="010".

4. NEW DESIGN PARADIGM FOR NEMS-BASED DIGITAL CIRCUITS

4.1 Logic Minimization Using Standard K-Map Technique

The availability of compact XOR/XNOR gates has significant implications for minimizing Boolean functions using K-maps as will be shown here. In order to appreciate such implications, one should first consider the standard K-map approach. In the conventional K-map technique, "1s" are grouped only in the horizontal and/or vertical fashion. For instance, a simple example is shown in **Fig. 7 (a)**, where three minterms ("1s") are organized as a horizontal and a vertical pair. This simplification results in a Boolean function of the form $F = \bar{A}B + B\bar{C}$. On the other hand, the K-map presented in **Fig. 7 (b)** can not be simplified using the standard K-map approach. The reason is that such a simplification results in a Boolean function of the form $F = B(A \oplus C)$, which requires an XOR operation. Since CMOS-based XOR implementation are not power- and area-efficient, here, the optimal approach is to implement such a Boolean function without any simplification as shown **Fig. 7 (c).**

4.2 New Paradigm: Diagonal Grouping of "1s" in K-Maps

The diagonal grouping of "1s" (as shown in **Fig. 7 (b))** is possible, if circuits are designed using laterally-actuated double-gate NEMS devices due to the availability of power- and area-efficient XOR/XNOR gates. This unique approach can significantly reduce the number of transistors required to implement Boolean functions. For instance, the Boolean function $F = B(A \oplus C)$ can be successfully designed using only four NEMS devices as illustrated in **Fig. 8 (a)**. In this circuit, the pull-up network is composed of NEMS1 and NEMS2, which are in series, therefore, the pull-up network connects the output (F) to VDD only when B and $(A \oplus C)$ are simultaneously "1". NEMS1 connects the internal node (INT) to VDD when "AC" is either equal to "10" or

"01" (XOR function). Then, assuming that *INT* is already connected to VDD, NEMS2 connects *INT* to *F* only when B="1". This is because when B="0", the beam of NEMS2 is attracted by two equal, yet opposing electrostatic forces generated by the gate terminals. However, when B="1", the beam is only attracted by the gate terminal that is connected to the ground (GND). Note that in **Fig. 8 (a)**, the pull-down network is the dual of the pull-up network to connect the output node to GND when it is not tied to VDD.

Fig. 8 (b)-(c) illustrates the operation of the circuit shown in **Fig. 8 (a)** when inputs (ABC) are "110" and "010", respectively. When ABC = "110", only NEMS1 and NEMS2 turn ON and thus, F becomes connected to VDD. In contrast, when ABC = "010", only NEMS3 turns ON and F will be connected to GND. A comparison between the NEMS-based design (**Fig. 8 (a)**) and the CMOS-based circuit (**Fig. 7 (c)**) reveals that the former requires less number of devices for the implementation of an identical Boolean function.

The K-map shown in **Fig. 9 (a)** is another example where four "1s" can be grouped in a zig-zag fashion. Such a grouping results in a Boolean function in the form of $F = B((A \oplus C) \oplus D)$ that requires two XOR and one AND operations as illustrated in **Fig. 9 (b)**. A NEMS-based implementation of this Boolean function is presented in **Fig. 9 (c).** In this figure, NEMS1 and NEMS2 generate $C \oplus D$, which in turn is connected to the inputs of NEMS3 and NEMS5. The rest of this circuit is similar to the one presented in **Fig. 8 (a)**. Note that for this Boolean function, the standard K-map technique (which is used for CMOS-based designs) results in no improvement since there are no pairs of "1s", which can be grouped in either horizontal or vertical fashion.

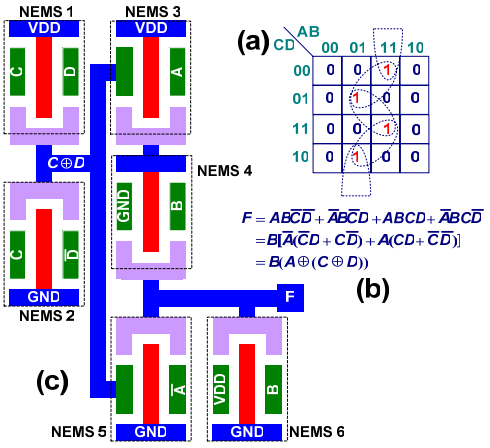

Fig. 9. Diagonal grouping of four "1s" in a zig-zag fashion results in two XOR operators: (a) the K-map, (b) the Boolean function simplification and (c) the NEMS-based implementation.

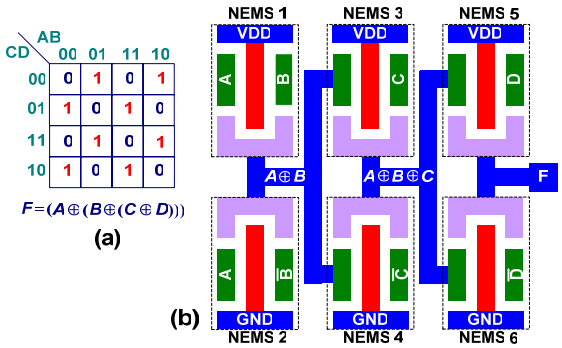

Fig. 10. (a) A four-variable Boolean function which can be implemented using three XOR gates and (b) its NEMS-based design.

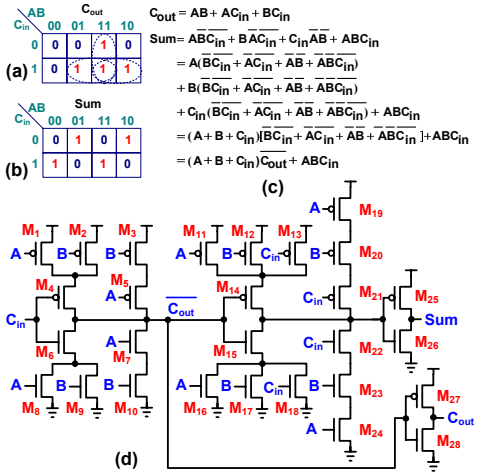

Fig. 11. CMOS-based full-adder: (a)-(b) K-maps for Cout and Sum, (c) Boolean functions and (d) the transistor-level implementation.

The four-variable K-map depicted in **Fig. 10 (a)** is the most extreme case where NEMS-based designs can offer the maximum advantage over their standard CMOS-based counterparts. The implementation of such a K-map requires three XOR operations ($F = ((A \oplus B) \oplus C) \oplus D$). This Boolean function can be implemented using three cascaded NEMS-based XOR gates as shown in **Fig. 10 (b)**. In this design, NEMS1 and NEMS2 generate $A \oplus B$, which is used by NEMS3 and NEMS4 to create $(A \oplus B) \oplus C$. Finally, NEMS5 and NEMS6 are employed at the last stage to generate the desired Boolean function ($F = ((A \oplus B) \oplus C) \oplus D$). Note that, in this case, the NEMS-counterpart needs at least 44 transistors.

Therefore, an improvement of more than 600% is achieved in terms of the number of devices required to implement this particular Boolean function. It should be noted that the advantage of employing the diagonal grouping varies for different Boolean functions. Therefore, the actual benefits of the proposed approach can only be identified if a practical design problem such as the implementation of a full-adder is investigated.

4.3 NEMS-Based Full Adder Design

Full-adder circuits are the building blocks of arithmetic modules in advanced microprocessors. In order to illustrate the effectiveness of the proposed design paradigm, the implementation of a NEMS-based full-adder circuit is compared to its "standard CMOS" counterpart. Note that a full-adder can be implemented using fewer CMOS devices using pass transistors approaches. However, such implementations suffer from reliability issues. In order to facilitate the comparison, the standard CMOS implementation of a full-adder, which requires at least 28 transistors, is shown in **Fig. 11**. The K-maps corresponding to carry-out (C_{out}) and sum (Sum) outputs of the full-adder are shown in **Fig. 11 (a)** and **Fig. 11(b)**, respectively. Here, A and B are the input bits and C_{in} denotes the carry-in signal. The transistor-level implementation of C_{out} (depicted in **Fig. 11 (d)**) is based on the grouping of "1s" in horizontal and vertical pairs as illustrated in **Fig. 11 (a)**. Note that the K-map corresponding to Sum suggests that no minimization is applicable since it is not possible to group "1s" in the horizontal or vertical fashion. However, the Boolean function corresponding to Sum can be re-arranged as shown in **Fig. 11 (c)** in order to obtain a function that includes C_{in} in its expression. This allows re-using some of the logic circuits employed to generate C_{out} and thus, reduces the number of required transistors. The transistor-level implementation of Sum is also presented in **Fig. 11 (d)** where C_{out} is generated and re-used to produce Sum.

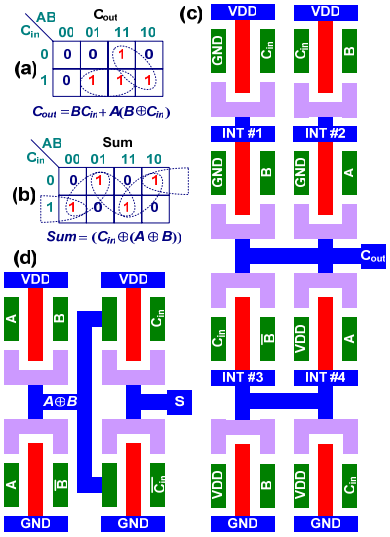

Fig. 12. NEMS-based full-adder: (a)-(b) K-maps for C_{out} and *Sum* and (c)-(d) NEMS-based implementations.

The novel design paradigm proposed in this work allows the design of NEMS-based full-adders using less number of devices due to possibility of the diagonal grouping of "1s". The K-maps associated with carry-out (C_{out}) and sum (Sum) of the full-adder are shown once more in **Fig. 12 (a)** and **Fig. 12 (b)**, respectively. The K-map corresponding to C_{out} is simplified as shown in **Fig. 12 (a),** which results in $C_{out} = BC_{in} + A(B \oplus C_{in})$. Here, the first term is a result of the horizontal grouping of minterms ABC="011" and ABC="111" while the second term represents the diagonal grouping of minterms ABC="110" and ABC="101". Similarly, **Fig. 12 (b)** represents the K-map for Sum, which is simplified as $Sum = C_{in} \oplus (A \oplus B)$.

The transistor-level implementations of C_{out} and Sum are demonstrated in **Fig. 12 (c)** and **Fig. 12 (d)**, respectively. The pull-up network associated with C_{out} is composed of two parallel branches: the one on the left implements BC_{in} and the other one to produce $A(B \oplus C_{in})$, which is similar to **Fig. 8 (a)**. Naturally, the pull-down network is designed to be the dual of the pull-up network. **Fig. 12 (d)** represents the circuit implementation of Sum (S), which is composed of two cascaded NEMS-based XOR gates. The output of the first XOR gate (denoted as $A \oplus B$ in the figure) is connected to the inputs of the second XOR to generate $Sum = A \oplus (B \oplus C_{in})$ at its output. Note that the NEMS-based design requires only 12 devices compared to 28 transistors needed by its CMOS counterpart.

5. POWER/PERFORMANCE COMPARISON USING CIRCUIT SIMULATIONS

5.1 Energy-Efficiency Enhancement

Using the proposed design paradigm, extremely energy-efficient logic circuits can be implemented. There are two main reasons for such an improvement. First, NEMS devices are inherently low-power due to their steep subthreshold slopes as shown in previous reports [3]. This means that the power consumption of a NEMS-based circuit due to subthreshold leakage is negligible compared to that of its CMOS counterpart. Therefore, assuming an identical level of dynamic power consumption, the NEMS-based circuit will offer superior energy-efficiency. Second, the proposed design methodology enables circuit designers to implement various Boolean functions in a more compact fashion. By reducing the number of devices, the dynamic power consumption also decreases due to fewer internal nodes that must be charged or discharged.

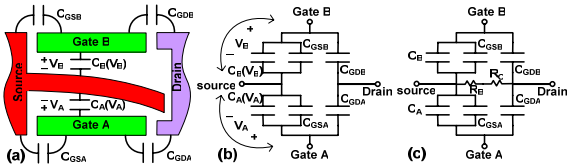

Fig. 13. Compact circuit models for laterally-actuated double-gate NEMS: (a) the schematic of the device in the OFF state along with all capacitances, the compact model of the device in (b) the OFF state and (c) the ON state.

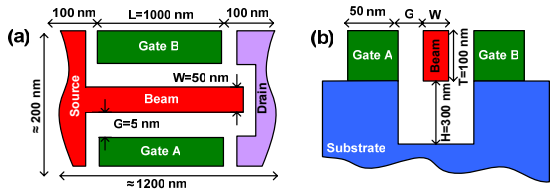

Fig. 14. The laterally-actuated double-gate NEMS device used in the circuit simulations: (a) schematic of the top-view and (b) the side-view schematic. The different dimensions of the structure are indicated here.

5.2 Compact Circuit Models

In order to investigate the performance/power of the NEMS-based full-adders, compact circuit models are used in this work. These compact models are illustrated in **Fig. 13** where the coupling capacitances between the beam and the Gate A and Gate B are denoted as C_A and C_B, respectively. Furthermore, the voltage difference between Gate A and Gate B are labeled as V_A and V_B, correspondingly. If the device is in the OFF state, the value of CA and C_B depend on V_A and V_B as indicated in Fig. 13 (a)-(b) because the curvature of the beam (and hence, the coupling capacitance) is a function of the gate bias. Using the models proposed in [8], one can take into account the dependency of C_A and C_B on V_A and V_B. While both C_A and C_B are functions of the gate bias in the OFF state, these variables are independent of the gate voltage when the device is ON. This is because, in the ON state, the shape of the bended beam is invariant; therefore, the values of C_A and C_B are independent of the gate biases (as indicated in **Fig. 13 (c)**).

The parasitic capacitances between the gate and the source (C_{GSA} and C_{GSB}) and the gate and the drain (C_{GDA} and C_{GDB}) are also included in these compact models. Since these parasitic capacitances exist between stationary parts of the device, their values can be easily calculated using the parallel plate capacitance model. The source and the drain terminals are electrically isolated when the transistor is OFF (**Fig. 13** (b)), a conduction path is formed once the device turns ON (**Fig. 13** (c)). Note that there will be a contact resistance at the interface of the beam and the drain terminal when they come into contact. Therefore, this electrical connection can be modeled with a series combination of the beam resistance (R_B) and the contact resistance (R_C). The values of R_B and R_C can be calculated using existing models [32]-[33] in the literature or extracted from the I_{DS} -V_{GS} characteristics of devices.

5.3 Power-Performance Comparison

The power-performance of the proposed full-adder is compared to its CMOS counterpart at 65 nm technology node. Assuming a power supply of 1V, the physical dimensions of the NEMS devices are designed to result in $V_{pull\text{-}in} = 0.5V$. Such dimensions are shown in **Fig. 14** (it is assumed that reliable methods are available for the fabrication of small gap sizes). Assuming that the cantilever beam is made of titanium (resistivity (ρ) =0.42μΩ.m), the resistance of the beam is calculated as $R_B \approx 210\Omega$. Using a methodology proposed in [32]-[33], which is based on the contact theory, the contact resistance (R_C) is estimated to be ≈ 2.2kΩ. Moreover, the gate capacitances, C_A and C_B, vary in the range of 0.2~1fF

depending on the gate bias. Other parasitic capacitances (C_{GSA}, C_{GSB}, C_{GDA} and C_{GDB}) are estimated to be ≈ 0.05fF.

Note that the delay of a NEMS device consist of two components: (1) mechanical delay: the time that is needed to deflect the beam and form a contact and (2) electrical delay: the time which is required to charge/discharge the output load. The mechanical delay of NEMS devices can also be integrated in the circuit model (though not shown in **Fig. 13**) using available analytical models [8]. The electrical delay of the NEMS transistors/circuits can be determined using commercial circuit simulators and the model proposed in **Fig. 13**.

A NEMS-based 32-bit carry-save adder [1] is simulated using the developed model [8] and its average delay is determined to be ≈ 1.92ns. This means that the circuit can reach a maximum performance of 200MOPS (Million Operations Per Second) at a clock rate of 500MHz. This adder consumes 0.92mW under the full-load condition (activity factor = 100%) dominantly due to its dynamic power consumption. The power consumption caused by the mechanical movement of the beam is estimated to be as low as ~6% of the total power [8]. When the adder is idle (activity factor = 0%), the adder consumes negligible leakage power as a result of the near-zero subthreshold leakage of its NEMS devices.

A 32-bit CMOS adder is also designed to serve as a reference for power-performance comparison. Assuming an identical silicon area for both NEMS and CMOS-based adders, the size of CMOS devices are estimated to be 750nm × 65nm (all transistors are sized equally, for simplicity). Considering these dimensions, the 32-bit CMOS adder is simulated using BPTM models [34] and its average delay is measured to be ≈ 975ps. This means that the circuit can perform 1000MOPS at a clock rate of 1GHz. This adder consumes 1.98mW under the full-load condition (activity factor = 100%) mainly because of its dynamic power dissipation. When the adder is idle (activity factor = 0%), the adder consumes 11.6mW as a result of the subthreshold leakage of its CMOS devices.

The power-performance comparison of these two adders is summarized in **Fig. 15**. In this figure, the horizontal axis represents the total power consumption of the 32-bit adders and the vertical axis denotes the logarithms of their performance (throughputs) in terms of MOPS. For medium levels of performance (<134MOPS), NEMS-based adder can offer matching performances with superior energy-efficiency (region A). This is because the CMOS-based adder always consumes power even when it is not performing any calculations. As a result, in this region, NEMS-based adder can offer the same level of performance with higher energy-efficiency. For higher performances (134 ~ 205MOPS), the CMOS adder becomes more power-efficient (region B and C). Note that NEMS adder is not able to offer very high performance values (> 205MOPS) due to the combined effect of high mechanical delays and charge/discharge delays (region C). Therefore, **Fig. 15** indicates that the NEMS-base adder is a more energy-efficient choice for the medium levels of performance.

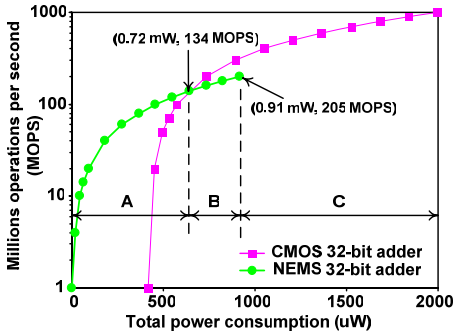

Fig. 15. The power-performance analysis for CMOS- and NEMS-based 32-bit adders.

6. CONCLUSIONS

This work illustrates the implementation of compact XOR/XNOR gates using only two laterally-actuated double-gate nano-electro-mechanical switches (NEMS). More interestingly, it is shown that the availability of such compact XOR/XNOR gates has profound implications for simplifying Boolean functions using Karnaugh maps (K-maps). The reason is that in standard K-maps, adjacent "1s" are grouped only in horizontal and/or vertical directions. However, for the first time ever, this paper demonstrates that in lateral NEMS-based circuits, the diagonal grouping of adjacent "1s" is also possible as a result of the availability of the proposed compact XOR/XNOR gates. This enables circuit designers to implement energy-efficient logic functions using significantly fewer transistors. For instance, a NEMS-based full-adder is implemented using less than half the number of transistors required by its static CMOS equivalent. Furthermore, it is shown that for the medium-range performances, the NEMS adders offer higher energy-efficiencies compare to their CMOS counterparts.

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