Design Optimization of FinFET Domino Logic Considering the Width Quantization Property

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***Abstract*—Design optimization of FinFET domino logic is particularly challenging due to the unique width quantization property of FinFET devices. Since the keeper device in domino logic is sized based on the leakage current of the pull-down network (PDN) (to meet the noise margin constraint), a reliable statistical framework is required to accurately estimate the domino gate leakage current. Considering the width quantization property, this paper presents such a statistical framework, which provides a reliable design window for keeper sizing to meet the noise margin constraint (for the practical range of threshold voltage variation in sub-32-nm technology nodes). On the other hand, the width quantization property restricts the design optimization (including power/performance characteristics) typically achieved via continuous keeper sizing in planar-CMOS domino logic designs. To cope with this restriction, this paper also introduces a novel methodology for FinFET-based keeper design, which exploits the exclusive property of FinFET devices (capacitive coupling between the front gate and the back gate in a four-terminal FinFET) to simultaneously achieve higher performance and lower power consumption. Using this new methodology, the keeper device is made weaker at the beginning of the evaluation phase to reduce its contention with the PDN, but gradually becomes stronger to provide a higher noise margin.**

***Index Terms*—Design optimization, Domino logic, FinFET, leakage estimation, width quantization.**

I. Introduction

FinFET devices have been proposed as the most likely candidate to substitute bulk MOSFETs for ultimate scaling [1]. The FinFET devices can be employed either with two gates tied together [a three-terminal (3T) structure] or with two independently biased gates [a four-terminal (4T) structure] [2] (Fig. 1). The main difference between bulk-CMOS and FinFET technologies appears when larger devices are required. As shown in Fig. 2(a) and (b), in bulk-CMOS technology, the width of the device is a continuous parameter, while in FinFET, to maintain the mechanical stability, a larger device (multifin device) is built with several fins [Fig. 2(c)]. The width of the multifin FinFET device is given by

$$\text{Width} = 2 \times n \times H \tag{1}$$

where H is the height of the fin, and n is the number of fins in a multifin device. This property (width quantization) restricts the design (including performance/power characteristics) optimization that is typically achieved via continuous device sizing (as shown in Fig. 2, the width of the device in bulk technology is not quantized) in planar CMOS technologies. In the first part of this paper, we study the effect of width quantization on the leakage characteristics of FinFET-based domino logic gates and provide a reliable design window for FinFET domino gates.

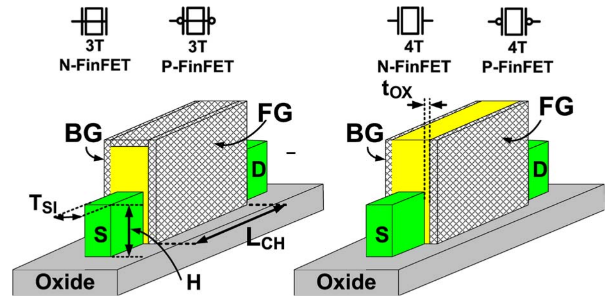

Fig. 1. In a 3T FinFET, the front gate (FG) and back gate (BG) are connected to each other, while in a 4T FinFET, FG and BG are separated. T_{SI} and t_{OX} are the fin thickness and oxide thickness, respectively. H is the fin height, and L_{CH} is the channel length.

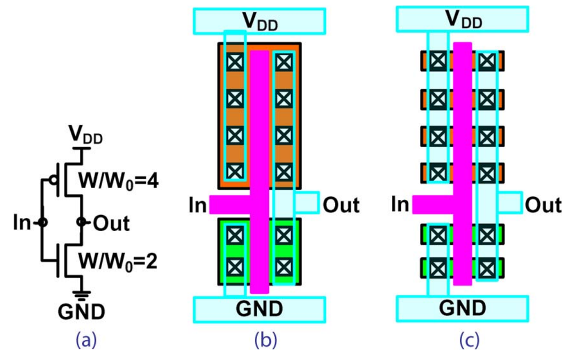

Fig. 2. (a) Circuit schematic of an inverter. The width of PMOS and NMOS devices are four times and twice the minimum device width (W_0), respectively. (b) Layout of the inverter in bulk-CMOS technology, where the width of the device is a continuous parameter. (c) Layout of the inverter in FinFET technology, where the width of the device is quantized. The p-type and n-type devices are multifin structures with four and two fins, respectively.

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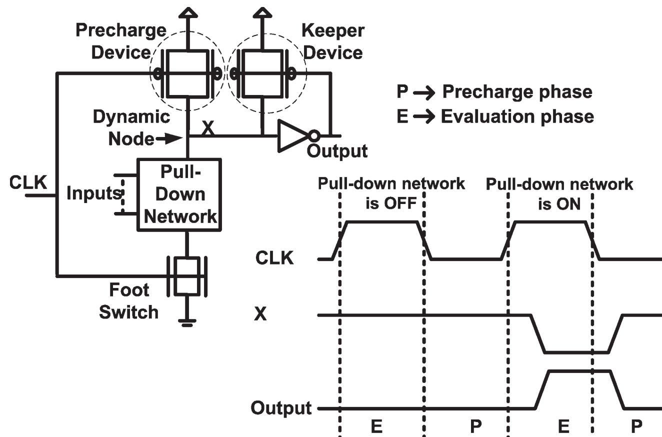

Fig. 3. Standard domino logic consists of a precharge block, a keeper device, a PDN, and an inverter. In the precharge phase, the dynamic node charges to $V_{\rm DD}$, and the output is "0." In the evaluation phase, the dynamic node is discharged or kept at "1," depending on the input signals.

A. Domino Logic

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of dynamic CMOS circuits as compared to static CMOS circuits [3]. The structure of standard 3T FinFET domino logic gates are similar to the bulk-CMOS domino logic gates, except that all the bulk devices are replaced by 3T FinFET devices (Fig. 3). A domino gate consists of a precharge (PMOS device), a pull-down network (PDN), a PMOS keeper, an NMOS footer device, and an inverter. During the precharge phase, the clock (CLK) is low; hence, the precharge transistor is "ON", and the dynamic node ("X") is charged to $V_{\rm DD}$, driving the output to the ground and turning on the "keeper" device. When the clock makes a "0" $\rightarrow$ "1" transition, the circuit enters the evaluation phase. During the evaluation phase, the footer NMOS is "ON," and the dynamic node is discharged to the ground or kept at $V_{\rm DD}$, depending on the input signals.

B. Keeper Sizing

In domino logic circuits, a weak keeper is required to reduce the power consumption and increase the performance of the domino logic (since the inverter's output is connected to the gate of the keeper device). On the other hand, a strong keeper is preferred to compensate the PDN leakage current and provide the required noise margin. Therefore, there is a tradeoff among the achievable noise margin, performance, and power consumption of the domino gates [3], [4]. As a result, the size of the keeper device should be determined such that a sufficient amount of current is supplied to the dynamic node (to compensate for the PDN leakage current and provide a sufficient noise margin) without penalty in terms of performance and power consumption. Therefore, it is crucial to accurately estimate the PDN leakage current. On the other hand, in FinFET domino logic gates, to accurately evaluate the PDN leakage current, the width quantization property must be considered [5].

The rest of this paper is organized as follows. Considering the width quantization property, in Section II, a new statistical framework is proposed to accurately predict the PDN leakage current, which provides a reliable design window for keeper sizing. This methodology guarantees that the noise margin constraint is met, since the keeper is sized based on the accurate estimation of the PDN leakage current. Moreover, to optimize the performance and power consumption, Section III presents the new methodology for keeper design of FinFET domino logic gates, which exploits the exclusive property of 4T FinFETs to reduce the contention between the keeper and the PDN at the beginning of the evaluation phase. This methodology alleviates the problem of adjusting the strength of the keeper device (due to the width quantization property) and provides flexibility in keeper sizing of the FinFET domino logic circuits. Finally, concluding remarks are made in Section IV.

II. Accurate Estimation of the PDN Leakage Current

As mentioned earlier, in domino logic gates, the keeper is sized based on the PDN leakage current. On the other hand, generally, in FinFET-based circuits, a single-fin device cannot provide sufficient current to meet the performance constraints; hence, wider devices should be employed. In FinFET technology, the width of the device is proportional to the height of the fin [see (1)]. To maintain the mechanical stability, the height of the devices, however, is limited to several times the fin thickness. Therefore, to increase the size of the FinFET devices, multifin devices are used, which are built with several individual fins [Fig. 2(c)]. As shown in Fig. 4(a) and (b), due to process variation, individual fins can have different threshold voltages. The gate work function, channel length, and fin thickness variation are the most important sources of variations in FinFET devices [6]. However, it is not the goal of this paper to discuss the effect of the different sources of threshold voltage variation. In our simulations, we include the effect of all sources of variation by assuming a Gaussian distribution for threshold voltages of the individual fins in multifin devices. One can expect the standard deviation of threshold voltages to increase with scaling. Our goal is to accurately estimate the leakage current of a multifin device (and hence, the PDN leakage current) in the presence of process variation. In the following sections, we first explain the conventional approach [7], [8] and the Fenton–Wilkinson (FW) approach (employed in [5]) and then, present the Schwartz–Yeh (SY) approach (employed in this paper) to accurately estimate the leakage current of a multifin device.

A. Conventional and FW Approaches

Conventional leakage estimation approaches [7], [8] do not consider the width quantization property of FinFETs and extend the variation for an individual device to multifin devices by simple scaling as prevalent in bulk-CMOS devices. As shown in Fig. 4(c), in this method, the mean value of the threshold voltage of the multifin device $(\mu(V'_T))$ is identical to the mean value of the threshold voltage of the individual fins $(\mu_{V_{\rm TX}})$. Moreover, the standard deviation of the threshold voltage is inversely proportional to the square root of the number of fins in a multifin device. This method underestimates the average

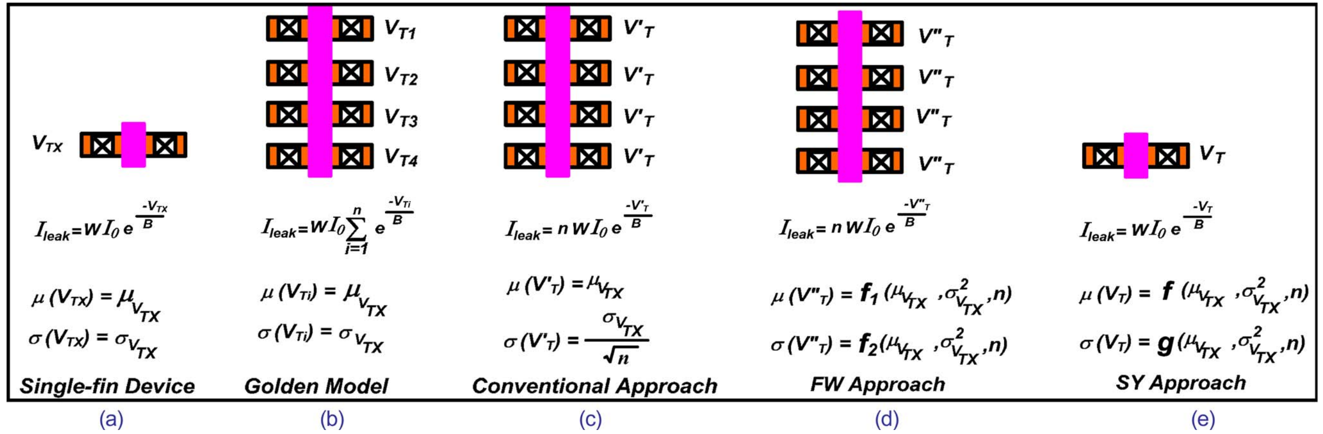

Fig. 4. (a) Threshold voltage (V_{TX}) of an individual fin is assumed to have a Gaussian (normal) distribution with a mean value of $\mu_{V_{\mathrm{TX}}}$ and a standard deviation of $\sigma_{V_{\mathrm{TX}}}$. (b) In a multifin device built with four fins, due to process variations, fins can have different threshold voltages (V_{T1}, V_{T2}, V_{T3}, and V_{T4}). (c) In the conventional approach, in a multifin device, the threshold voltage (V_T') has an identical mean value to that of the individual fins and standard deviation of the threshold voltage, which is inversely proportional to the square root of the number of fins (n) in the multifin device. (d) In the FW method, the mean value and standard deviation of the threshold voltage (V_T'') are functions of the mean value and standard deviation of the threshold voltage of individual fins, as well as the number of fins in a multifin device (n). (e) In the SY method (proposed in this paper), for a multifin device, we find an equivalent single-fin device with equivalent threshold voltage (V_T). The mean value and standard deviation of V_T are functions of $\mu_{V_{\mathrm{TX}}}$, $\sigma_{V_{\mathrm{TX}}}$, and n.

leakage current of a multifin device (and hence, the PDN leakage current) by as much as 40% [5].

To accurately estimate the leakage current, let us first examine the leakage current of the individual fins. Assuming that the threshold voltage of an individual fin has a normal (Gaussian) distribution $(N(\mu_{V_{\mathrm{TX}}}, \sigma_{V_{\mathrm{TX}}}))$, its leakage current has a lognormal distribution, as given by the following (a lognormal random variable is characterized by the property that its logarithm has a normal distribution):

$$I_{\mathrm{Leakage}} = W I_0 e^{-\frac{V_{\mathrm{TX}}}{B}} \quad B = m\frac{kT}{q} \tag{2}$$

where V_{TX} is the threshold voltage of an individual fin, m is the body factor, I_0 is a technology-dependent parameter, and W is the width of the single-fin FinFET $(2 \times H)$. kT/q is the thermal voltage (≅26 mV at the room temperature), and mkT/q is referred to as constant B for simplicity. The leakage current of a multifin device with four fins [Fig. 4(b)] is the sum of the leakage currents of the individual fins, as given by the following (golden model):

$$I_{\mathrm{Leakage}} = W I_0 \left\{ e^{-\frac{V_{T1}}{B}} + e^{-\frac{V_{T2}}{B}} + e^{-\frac{V_{T3}}{B}} + e^{-\frac{V_{T4}}{B}} \right\} \tag{3}$$

where V_{T1}, V_{T2}, V_{T3}, and V_{T4} are the threshold voltages of individual fins in the multifin device.

In the general case, the leakage current of a multifin device is a sum of n lognormal variables, where n is the number of the fins in a multifin device. If L_i is a lognormal random variable (which represents the leakage current of an individual fin), we are interested in finding the mean and variance of L (the leakage current of a multifin device with n fins: $L = L_1 + L_2 + \cdots + L_n$). Unfortunately, there is no exact mathematical solution for the sum of lognormal variables. However, there exist two widely accepted approximation methods [9]. The first method is the FW approximation [10] and the second method is the SY approximation [11]. Both methods assume that the sum of lognormal components has a lognormal distribution with a mean and a variance that can directly be calculated in terms of the mean and the variance of each individual component.

As detailed in [5], the FW method approximates the leakage current of a PDN in a domino logic based on the mean value and standard deviation of the threshold voltage of individual fins, as well as the number of fins in a multifin device [Fig. 4(d)]. It is known from the literature that the FW approximation is applicable with good accuracy when the standard deviation of lognormal components is less than 4 dB [9]. Hence, the FW method can accurately predict the leakage current profile when the threshold voltage variation is less than 30 mV as derived from

$$\frac{\sigma_{V_{\mathrm{TX}}}}{m\frac{kT}{q}} \times \frac{10}{\ln 10} < 4 \Rightarrow \sigma_{V_{\mathrm{TX}}} < 0.92 \times m\frac{kT}{q}. \tag{4}$$

The coefficient $10/\ln(10)$ comes from converting a logarithm with base 10 to a natural logarithm. Since FinFETs have near-ideal subthreshold swing, m (body factor) is approximately one; therefore, the FW method is accurate when the threshold voltage variation is less than 30 mV. However, for the 32-nm technology node and for minimum-size devices, the threshold voltage variation can be more than 40 mV [12]–[14]. Moreover, the threshold voltage variation increases with device scaling. Hence, we use the SY method, which is more accurate in the practical range of threshold voltage variations for sub-32-nm technology nodes. In this paper, for each multifin device, we find an equivalent single-fin device, which has an identical leakage profile to that of the multifin device [Fig. 4(e)]. The mean and standard deviation of the threshold voltage of this equivalent single-fin device are functions of the mean and variance of threshold voltage of the individual fins, as well as the number of fins in the multifin device, as explained below.

B. SY Approach

In the SY method, exact expressions for the first two moments of the sum of two lognormal random variables are

calculated. By assuming that this sum is also a lognormal random variable [11], a recursive technique is used to find the first two moments of the sum of $n > 2$ lognormal random variables . The calculation method in the original paper of Schwartz and Yeh is complex and prone to round-off errors during the calculation. Therefore, for the first time, we used a modified version of the SY method presented by Ho [15], which is more accurate than the original SY method. The exact mean and variance of the sum of two lognormal random variables $z = \ln(e^{Y_1} + e^{Y_2})$ are calculated, as summarized by

$$w = Y_2 - Y_1 \tag{5}$$

$$\mu_w = \mu_{Y_2} - \mu_{Y_1} \tag{6}$$

$$\sigma_w^2 = \sigma_{Y_1}^2 + \sigma_{Y_2}^2 \tag{7}$$

$$\mu_z = \mu_{Y_1} + G_1 \tag{8}$$

$$\sigma_z^2 = \sigma_{Y_1}^2 - G_1^2 - 2\frac{\sigma_{Y_1}^2}{\sigma_w^2} G_3 + G_2 \tag{9}$$

$$G_1 = E\left[\ln(1 + e^w)\right] \tag{10}$$

$$G_2 = E\left[\ln^2(1 + e^w)\right] \tag{11}$$

$$G_3 = E\left[(w - \mu_w)\ln(1 + e^w)\right]. \tag{12}$$

For simplicity, the SY method is explained for independent variables (corresponds to random variation); however, simulation results include correlated variables, which represent both systematic and random variations.

A new variable w is defined in (5), with mean (μ_w) and standard deviation (σ_w), by which the mean and standard deviation of z are given by (8) and (9). Details of this method can be found in [15]. $E[X]$ denotes the expected value of the random variable X. G_1, G_2, and G_3 are auxiliary functions to calculate the mean and standard deviation of z.

It is worth noting that there are also several nonlognormal approximation methods, which are generally believed to be more accurate than the SY method [16]. However, with nonlognormal approximation, the mean and variance of the total leakage current cannot be directly calculated from the mean and variance of threshold voltage of the individual fins. Moreover, for standard cells with a relatively small number of inputs (such as a four-input domino OR gate), the accuracy of the SY method is similar to that of these nonlognormal approaches.

To compare the accuracy of these methods, rigorous simulations were performed using the FinFET model [17]. The channel length, oxide thickness (SiO_2), fin thickness, and fin height are assumed to be 32, 1, 10, and 50 nm, respectively. To have a comprehensive comparison between the FW and SY methods, we explore the effect of three parameters (namely, the number of fins in the PDN, the standard deviation of the threshold voltage, and the correlation factor among the threshold voltages of the individual fins) on the leakage prediction by these methods.

Fig. 5(a) and (b) show the distribution of the leakage current of three-input and four-input domino OR gates, respectively, where each input signal is connected to a multifin device with two fins. It can be observed that the error of the FW method increases for a higher number of fins in the PDN.

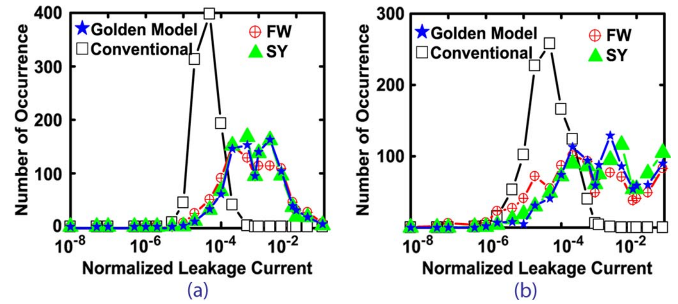

Fig. 5. (a) Normalized leakage current of the PDN in a three-input domino OR gate. (b) Normalized leakage current of the PDN in a four-input domino OR gate. In both gates, each input is connected to a multifin device with two fins. To consider the effect of systematic variations, the correlation factor (ρ) among the threshold voltages of fins is assumed to be 0.4. Monte Carlo simulations were performed with 1000 samples, with $(\sigma/\mu = 10\%)$.

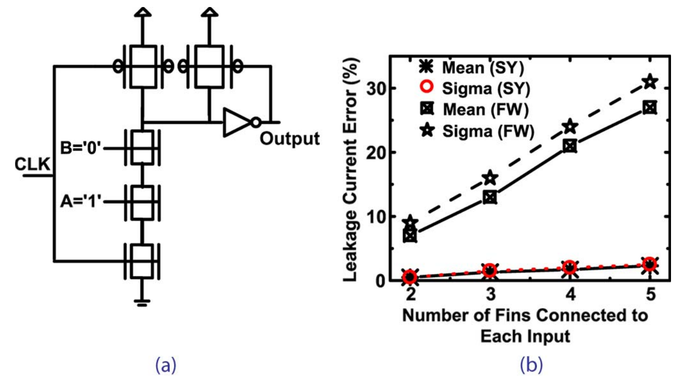

Fig. 6. (a) Circuit schematic of a two-input domino AND gate. (b) Errors of FW and SY methods in approximating the mean and standard deviation of the leakage current of the PDN with different numbers of fins (connected to each input) (correlation factor $(\rho) = 0.1$). Monte Carlo simulations were performed with 1000 samples, with $(\sigma/\mu = 10\%)$.

Fig. 6(a) shows the schematic of a two-input domino AND gate, where inputs A and B are assumed to have a “1” and “0” logic values in the evaluation phase. This input combination leads to the worst-case scenario in the subthreshold leakage current of the PDN for a two-input domino AND gate. Fig. 6(b) presents the error in the mean value and standard deviation of the PDN leakage current for different numbers of fins (which are connected to each input). It can be observed that the error of the FW method is much higher than that of the SY method, particularly, for a higher number of fins in the PDN. Moreover, a comparison between Figs. 5 and 6(b) reveals that the lower correlation factor among the threshold voltages of the individual fins results in a higher error for the FW method. In other words, the SY method is much more effective than the FW method when the effect of random variation is higher than the systematic variation.

Fig. 7(a) shows the normalized probability density function (PDF) of the normalized leakage current of the PDN in a four-input domino OR gate, where multifin devices with three fins are employed in the PDN. Fig. 7(b) shows the normalized PDF of the PDN leakage current in an eight-input domino OR gate, where multifin devices with two fins are employed in the PDN. A comparison between Figs. 5 and 7 shows that the error of the FW method increases for a higher standard deviation of the threshold voltage (which is the case for shorter channel length technologies).

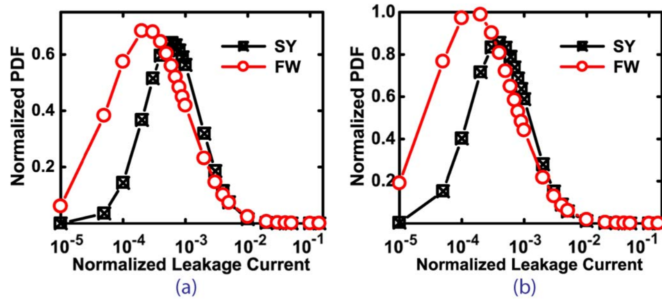

Fig. 7. (a) Normalized PDF of the PDN in a four-input domino OR gate. Each input is connected to a multifin device with three fins. (b) Normalized leakage current of the PDN in an eight-input OR gate domino logic. Each input is connected to a multifin device with two fins. For both gates, to consider the effect of systematic variations, a correlation factor of $\rho = 0.4$ is assumed among the threshold voltages of individual fins. Monte Carlo simulations were performed with 1000 samples ($\sigma/\mu = 20\%$).

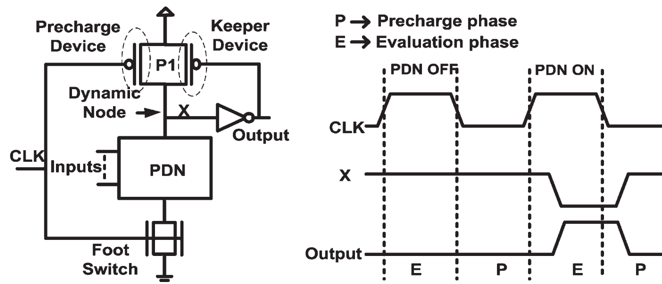

Fig. 8. FinFET domino logic with a dual-purpose 4T FinFET used as precharge and keeper blocks [18].

Using the proposed statistical method, a sufficient noise margin of FinFET domino logic is guaranteed, since the keeper is sized based on an accurate estimation of the PDN leakage current. Furthermore, to optimize the performance and power consumption of FinFET domino logic gates, in Section III, we propose a new methodology for keeper design. This new methodology exploits the exclusive property of 4T FinFET (capacitive coupling between the front and the back gate) to reduce the contention between the keeper and the PDN at the beginning of the evaluation phase.

III. New Keeper Design to Optimize the Power/Performance of the FinFET Domino Logic

A. Previous Works

In bulk-CMOS technology, several studies have been reported on keeper design to achieve high performance and high reliability. However, keeper design for FinFET domino gates is particularly challenging due to the width quantization property of the FinFET structures that prevents simultaneously achieving good performance and reliability by continuous keeper sizing. Existing FinFET-based domino logic designs in [18] (Fig. 8) and [19] use a dual-purpose 4T device to function as both the keeper and precharge blocks, which reduces the dynamic power consumption by the reduction of the clock load capacitance. However, the performance and power consumption in the evaluation phase cannot be optimized, since the keeper strength is fixed during the evaluation phase.

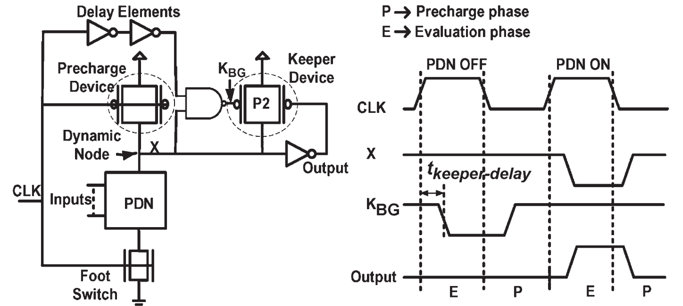

Fig. 9. FinFET domino logic with a 4T FinFET as keeper blocks [20].

The domino logic proposed in [20] (Fig. 9) reduces the contention between the keeper and PDN by modulating the threshold voltage of keeper. A p-type device, which operates in single-gate mode (only one gate has a "0" logic value and the other gate has a "1" logic value), has a high threshold voltage. On the other hand, a p-type device, which operates in double-gate mode (both gates have "0" logic values), has a low threshold voltage. The strength of the device in the single-gate mode is approximately 1/3 of the strength of the device in the double-gate mode. In [20], at the beginning of the evaluation phase, the keeper device operates in the single-gate mode (high threshold voltage) to reduce the contention between the keeper and the PDN. After a time-period equal to the latency produced by the delay elements ($t_{\mathrm{keeper-delay}}$ in Fig. 9), the keeper operates in the double-gate mode (low threshold voltage) to increase the noise margin.

It is worth noting that, in all previous work, at the beginning of the evaluation phase, the keeper device is fully turned ON (the gate–source voltage of the keeper equals V_{DD}), even in the case where the keeper operates in the single-gate mode.

B. Modulating Keeper Strength by Its Gate–Source Voltage

In this paper, instead of modulating the keeper threshold voltage, the strength of the keeper is controlled by its gate–source voltage. This approach provides a wider design space compared to the case when the strength of the device is adjusted by modulating its threshold voltage. The proposed method alleviates the impact of the restriction in adjusting the strength of the keeper due to the width quantization property of the FinFET devices.

To optimize the performance and power consumption, in our method, a low gate–source voltage is needed at the beginning of the evaluation phase, while a high gate–source voltage is required during the rest of the time. Assume a p-type device as the keeper in a domino gate, where the source of the keeper is connected to V_{DD} and its drain is connected to the dynamic node [Fig. 10(a)]. If a differential waveform is applied to the gate of the keeper, at the beginning of the evaluation phase, a low gate–source voltage weakens the keeper, while a high gate–source voltage provides a strong keeper for the rest of the time. Such a gate–source voltage modulation can be realized using an RC circuit and a clock signal [Fig. 10(b)]. The challenge is how to implement an RC circuit using FinFET devices [Fig. 11(a) and (b)]. In the following paragraph, we describe how that can be achieved.

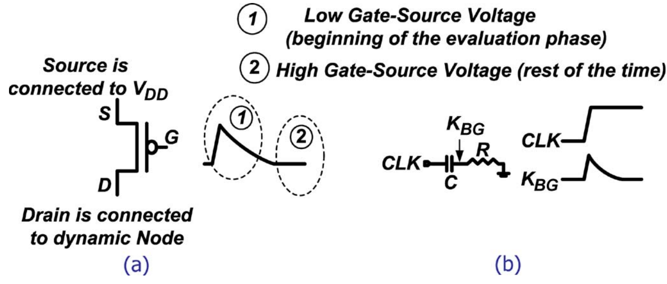

Fig. 10. (a) Application of a differential voltage to the gate of the keeper results in a weak keeper at the beginning of the evaluation phase and a strong keeper during the rest of the time. (b) Required differential waveform can be generated by an RC circuit and clock signal. As the *clock* signal makes a 0→1 transition, a differential waveform appears at the K_{BG} node.

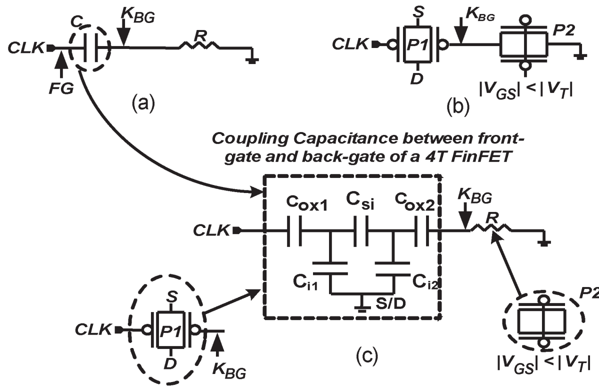

Fig. 11. (a) Required RC circuit for generating the differential waveform. (b) This circuit can be implemented by a 4T FinFET (P1) and a 3T FinFET (P2), which is referred to as a resistive-gate FinFET. (c) Coupling capacitance between the front- and the back- gates of a 4T FinFET can be used as capacitor in an RC circuit. A 3T FinFET, which operates in subthreshold regime, can be used as a resistor in an RC circuit.

A resistor can easily be implemented by a 3T FinFET (P2) operating in the subthreshold regime. We solve the problem of implementing the capacitor by exploiting the exclusive property of 4T FinFETs, namely, the coupling capacitance between the front gate and the back gate (P1), as shown in Fig. 11(b) (we refer to this circuit as a resistive-gate FinFET). The coupling capacitance between the two gates of the 4T FinFET is shown in Fig. 11(c), where C_{OX1} and C_{OX2} are the gate oxide capacitance of the front and back gates, respectively. C_{si} is the fin capacitance, while C_{i1} and C_{i2} are the inversion capacitances. Note that the coupling capacitance is shown in the equilibrium condition, i.e., no current flow between the source and the drain is assumed [21]. As a result, a differential voltage waveform appears on the back gate (K_{BG}) due to the transition in the front gate (FG) (which is connected to the clock), which can be estimated from

$$V_{\mathrm{BG}} = \alpha V_{\mathrm{FG}} e^{-\frac{t}{RC}} \tag{13}$$

where R is the resistance, and C is the coupling capacitance between the front and back gates. t is time and α is a constant, which depends on the value of the capacitances in Fig. 11(c). The values of C_{i1} and C_{i2} are negligible compared to those of the other capacitances in Fig. 11(c) for a low gate voltage, which is desirable to have a higher pulse on the resistor side (a higher value of α). The equivalent capacitance between the two gates in this case is a series combination of C_{OX1}, C_{OX2}, and C_{si}. C_{i1} and C_{i2} rapidly increase with the gate voltage and quickly dominate other capacitances [20]. In the meantime, C_{si} decreases and becomes negligible because of the screening of the gate field by the inversion channels near the front gate and the back gate [20].

In terms of fabrication, it has been demonstrated that 3T and 4T FinFET devices can be co-fabricated [2], [22]. The value of the resistor and capacitor and, hence, the differential waveform peak and the time constant can be controlled by the threshold voltage of P2 and P1. MEDICI [23] is used in this paper to study the effects of different parameters on the characteristics of a resistive-gate FinFET. Fig. 12(a) shows the peak value of the differential waveform at the back gate of P1 [K_{BG} in Fig. 11(b)] for various values of the fin and gate oxide thickness of P1. As it can be observed, the peak value of the differential waveform is high enough to guarantee the low gate–source voltage (and hence, a weak keeper), even in the presence of the process variation. Note that the process variation has negligible effect on the required resistor for the RC circuit, since P2 at the beginning of the evaluation phase is OFF. Fig. 12(b) shows the differential waveform for different fin thickness values of P1. Both the peak value and the time constant of the differential waveform increase for thinner fins. This differential voltage pulse reduces the drive current of the resistive-gate FinFET, which is desirable at the beginning of the evaluation phase to reduce the contention between the keeper and the PDN. On the other hand, the input capacitance of the resistive-gate FinFET is smaller than that of the 3T FinFET. Hence, the switching power can be reduced if a resistive-gate FinFET is used instead of a 3T FinFET. In the following section, we explain the FinFET domino logic design using a resistive-gate FinFET.

C. Proposed FinFET Domino Logic

The circuit-level schematic of the proposed FinFET domino logic is shown in Fig. 13(a), where a 4T p-type device (P1) is used as both the precharge and the keeper device. The front gate of P1 (which is connected to the *clock* (CLK)) acts as a precharge device, while the back gate of P1 (which is connected to K_{BG}) plays the role of the keeper device. In the precharge phase, CLK is low; the dynamic node and the output have “1” and “0” logic values, respectively. In the evaluation phase, when the PDN is OFF, the dynamic node remains at V_{DD}, and the output is connected to the ground. As explained before, at the beginning of the evaluation phase, P1 and P2 form a resistive-gate FinFET. Consequently, a “0” → “1” transition of the clock creates a differential waveform at K_{BG} (Figs. 13(b) and 14). After a short time, K_{BG} becomes connected to the output through N1, and the dynamic node is connected to V_{DD} via the back gate of P1 [dashed circle #1 in Fig. 13(b)]. The advantage of using the resistive-gate FinFET appears when the PDN is ON during the evaluation phase. At the beginning of the evaluation phase, the keeper is weak [dashed circle #2 in Fig. 13(b)]; therefore, the dynamic node is easily discharged, and the output makes a “0” → “1” transition. K_{BG} is connected to the output through P2 (which is ON, since dynamic node has “0” logic

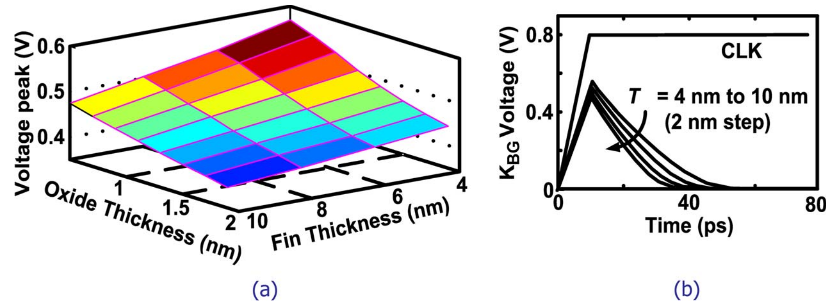

Fig. 12. (a) Peak value of the differential waveform at the back gate of a resistive-gate FinFET [K_{BG} in Fig. 11(b)] for 0 → 0.8 V transition in the front gate (CLK). (b) Differential waveform at the back gate (K_{BG}) of P1 in a resistive-gate FinFET [Fig. 11(b)], for 0 → 0.8 V transition in the front gate (*clock*) for various fin thicknesses of P1.

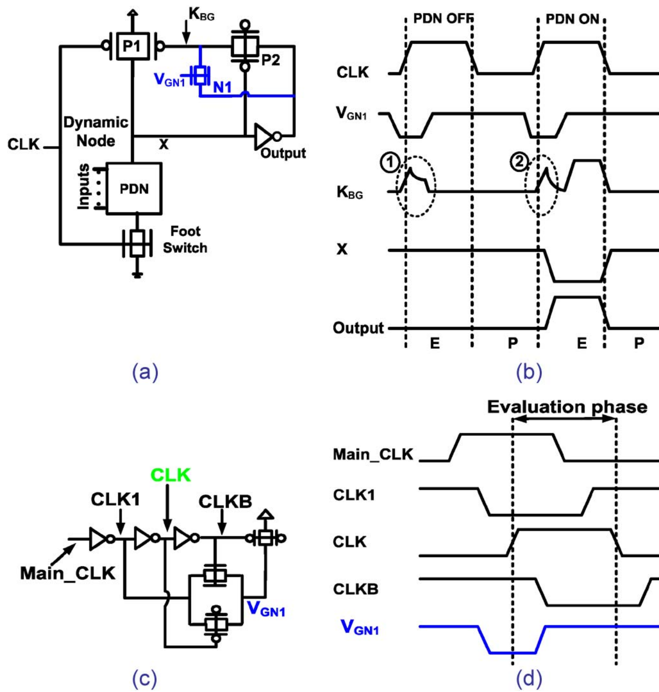

Fig. 13. (a) Structure of the proposed domino logic. (b) Signal waveforms of the proposed domino logic. (c) Schematic of the circuit for generating the gate bias of N1 (V_{GN1}). (d) The signal waveforms of the proposed circuit for generating the gate bias of N1 (V_{GN1}).

value). The proposed circuit for generating the gate bias of N1 (V_{GN1}) and corresponding signal waveforms are shown in Fig. 13(c) and (d). The circuits for generating the gate bias of N1 (V_{GN1}) can be shared among several domino gates, and hence, its power/area penalty is negligible. As an example, consider an eight-input domino OR gate where each input is connected to two fins. Assuming that the bias-generating circuit is shared among five gates, the area overhead is as low as 9%. For a 16-input domino OR gate, the area overhead is 5%, while the improvement in the delay and power is around 50% (Table I). In the following simulations, HfO_2 $(\mathrm{k} = 25)$ is assumed as the gate oxide material. The oxide thickness, fin thickness, channel length, and fin height are considered to be 4, 10, 25, and 50 nm, respectively. Gate work functions of the p-type and n-type devices are assumed to be 4.5 and 4.6 eV, respectively.

Since the parasitic capacitance and resistance significantly affect the characteristics of ultrascaled FinFET devices [24], [25], their effects are considered in our simulations. As shown in Fig. 14, the gate–source voltage of the keeper device, at the beginning of the evaluation phase, changes from 0.4 to 0.65 V (for $V_{\mathrm{DD}} = 0.8$ V), while in all previous works, the gate–source voltage of the keeper device is fixed at V_{DD}. To compare the keeper strength at the beginning of the evaluation phase in previous work and the proposed method, we assume an identical noise margin for all domino logic gates. It is also assumed that the discharging process of the dynamic node has been started and that the dynamic node voltage is reduced from 0.8 to 0.6 V; hence, the V_{DS} of the keeper is 0.2 V [Fig. 15(a)]. Fig. 15(b) shows the drive capability of the keeper device at the beginning of the evaluation phase in the proposed structure and in previous work for the same noise margin. The strength of the keeper in [18] is adjusted to be identical to that of the keeper in standard domino logic. The keeper in [20] operates in the single-gate mode, and its drive capability is lower than that of the keeper in standard domino logic gates. In the proposed structure, however, the drive capability of the keeper is approximately ten times lower than that of the keeper proposed in [19], which significantly reduces the contention between the keeper and the PDN. The proposed domino logic can also be implemented using asymmetric 4T FinFETs [26]; however, co-fabrication of symmetric and asymmetric 4T FinFETs is challenging.

It is worth noting that the resistive-gate FinFET with a fixed resistor [27] [a fixed resistor is used instead of P2 in Fig. 13(a)] cannot be used in keeper design. The reason is that, in this case, the back gate of P1 [in Fig. 13(a)] will be charged very slowly (Fig. 16) (through a low-pass filter consisting of the fixed resistor and gate capacitance of P1) and increase the short-circuit power consumption. However, this is not the case for the proposed domino logic, since the back gate of P1 is charged through P2 with a negligible delay (Fig. 16).

Table I compares the delay and power consumption of the different FinFET domino gates for the same noise margin and a clock frequency of 2.5 GHz with a V_{DD} of 0.8 V. It can be concluded that the proposed domino logic has higher performance compared to that of the previous work, since contention between the keeper and the PDN is reduced by using the resistive-gate keeper. The improvement in power and performance characteristics is higher in high fan-in gates, since a larger keeper is required in these gates to compensate for the leakage current of the PDN. A larger keeper results in a larger

TABLE I

COMPARISON BETWEEN THE DELAY AND POWER OF DIFFERENT DOMINO GATES FOR AN IDENTICAL NOISE MARGIN. n IS THE NUMBER OF FINS IN MULTIFIN DEVICES, WHICH ARE EMPLOYED IN THE PDN OF EACH GATE. $\sigma_{V_{\mathrm{TX}}}$ AND $\mu_{V_{\mathrm{TX}}}$ ARE THE MEAN VALUE AND STANDARD DEVIATION OF THE THRESHOLD VOLTAGE OF INDIVIDUAL FINS, RESPECTIVELY. THE STRENGTH OF THE KEEPER IN [19] IS ADJUSTED TO PROVIDE AN IDENTICAL NOISE MARGIN TO THAT OF THE STANDARD DOMINO LOGIC

		Delay (ps)						Power (μW)					
		This work		Ref. [20]		Ref. [18] (same as standard domino logic)		This work		Ref. [20]		Ref. [18] (same as standard domino logic)	
$\sigma_{V_{TX}}/\mu_{V_{TX}}$		10%	20%	10%	20%	10%	20%	10%	20%	10%	20%	10%	20%
Gate	n												
AND2	2	22	26	33	53	28	42	13.6	18	16	24	18	26
AND4	2	31	33	51	71	42	48	21	25	24	32	23	29
OR2	2	21	25	27	33	26	30	13.3	15	13.7	16	16	17
OR4	2	27	29	39	62	35	42	17	23	19.2	27	19.6	23
OR8	2	38	43	68	97	54	75	28	33	36	42	30	39
OR16	2	45	58	54	87	60	110	16	26	20	32	25	38
OR32	2	55	90	75	134	85	160	28	51	37	62	43	70
OR32	4	50	83	62	117	70	135	42	75	53	84	62	91

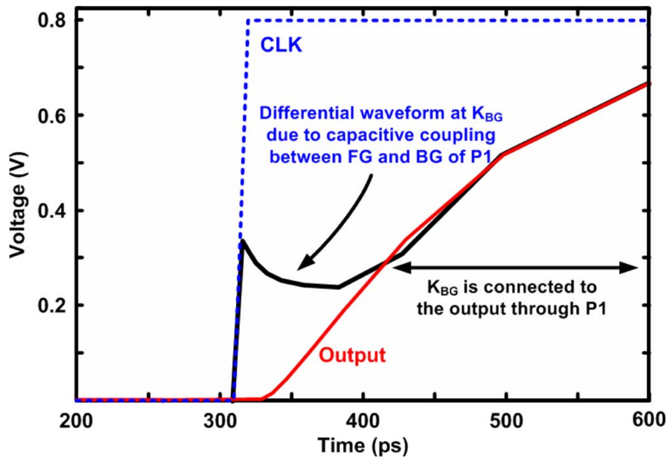

Fig. 14. Differential waveform at the back gate of P1 (due to the low-to-high transition of the clock), at the beginning of the evaluation phase, makes the keeper weaker and reduces the contention between the keeper and the PDN. If the dynamic node is discharged through PDN, the output makes a "0" → "1" transition. In this case, P2 instantly connects the back gate of P1 (K_{BG}) to the output. In this simulation, to clearly demonstrate the differential waveform, the load capacitance is assumed to be 300 fF.

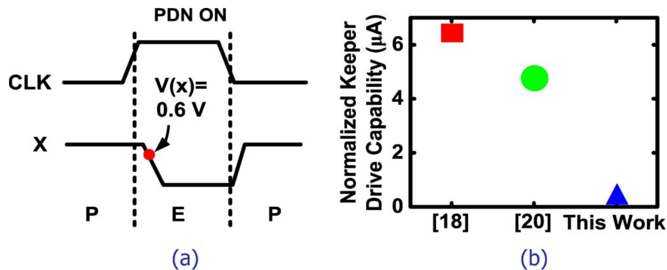

Fig. 15. (a) To compare the drive capability of the keeper in different domino logic gates, it is assumed that we are at the beginning of the evaluation phase, and the dynamic node voltage is reduced from 0.8 to 0.6 V (the V_{DS} of the keeper is 0.2 V). (b) Drive capability of the keeper at the beginning of the evaluation phase in different domino logic.

coupling capacitance and hence, a higher differential waveform at the gate of the keeper. As shown in Fig. 17, for identical performance or power constraints, the proposed structure has a better noise margin compared to previous FinFET domino gates.

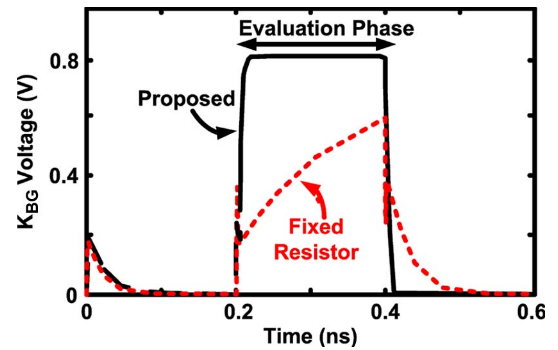

Fig. 16. MEDICI-predicted waveform at the back gate of P1 (in Fig. 11) for the 0 → 0.8 V transition in the front gate, when the resistive gate with a fixed resistor is used in the keeper design. In this case, the voltage of the back gate of P1 goes very slowly to "1," resulting in a high short-circuit current.

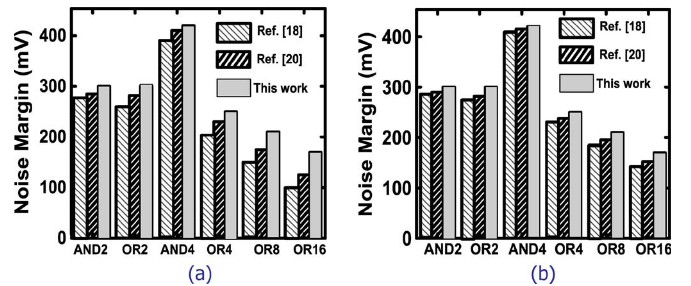

Fig. 17. Comparison among the different domino logic gates in terms of the noise margin. (a) Proposed domino logic provides a higher noise margin compared to previous work (in this simulation, the delay of the domino logic gates are set to be identical). (b) Assuming identical power consumption for different domino logic gates, the proposed domino logic provides a higher noise margin. The reason is that, for identical delay or identical power consumption, the keeper in the proposed domino logic can be stronger than those of the previous works.

IV. CONCLUSION

FinFET domino logic design is particularly challenging due to the width quantization property of the FinFET devices. In this paper, a new statistical framework is presented to provide a reliable design window in terms of the noise margin while considering the width quantization property. The keeper is sized based on an accurate estimation of the PDN leakage current that

is obtained using the modified SY method. Simulation results clearly indicate that the proposed method is more accurate than the most recently proposed method (FW method) for the practical range of threshold voltage variations in sub-32-nm technology nodes. Hence, the required noise margin is guaranteed. Moreover, to optimize the performance and power characteristics of domino logic gates under the sizing constraint arising due to width quantization, a new keeper (employing a resistive-gate FinFET) is proposed, which exploits the exclusive property of 4T FinFETs, namely, the capacitive coupling between the front gate and the back gate. In previous work, the keeper at the beginning of the evaluation phase is fully turned ON and is made weaker through modulating its threshold voltage. The proposed keeper in this paper, however, is made weaker through applying a differential waveform to its gate. Hence, at the beginning of the evaluation phase, the keeper is not fully turned ON, which makes the keeper more than ten times weaker than the keepers proposed in previous works. Therefore, contention between the keeper and the PDN is significantly reduced leading to higher performance and lower power consumption.

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