Name: **SOLUTIONS**

ECE 124A–Fall 2011
Prof. K. Banerjee

Perm No. _____

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

MIDTERM EXAMINATION-ECE124A

Room: ESB-Cooper Lab, November 8, 3:30-5:00 PM

READ CAREFULLY:

- **This is a CLOSED BOOK Exam. Any form of notes is not allowed. Calculators OK.**

- **READ the questions carefully before answering. Include all your answers in locations specified on these pages. Show ALL WORKING used to arrive at answers. Use space provided for all working. Use the back sides if necessary. There are 8 pages including the cover page. Be sure to write Your NAME/Perm No. on EVERY PAGE.**

Question	Scores
#1	/ 35
#2	/ 30
#3	/ 35
TOTAL	/ 100

Good Luck!

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1. Part I: (17 pts) (2 pts each for a-d) ***(suggested time: 10 minutes)***

a) Consider a long-channel NMOS transistor. Which of the following gate-to-source voltage conditions can be used to obtain a constant-current source?

(A) Vgs<Vds+Vt & Vgs>Vt (B) Vgs < Vt
(C) Vgs>Vds+Vt & Vgs>Vt (D) Vgs < 0.5Vds & Vgs>Vt

b) Which of the following operating regions in a MOSFET results in largest gate capacitance?

(A) saturation (B) linear (C) cut-off (D) A and C **(E)** B and C (F) A and B

c) Which of the following parameters scale identically according to both constant-Vdd and constant-Electric field scaling theories?

(A) active power (B) intrinsic gate delay (C) energy-delay product
(D) gate capacitance/unit area (E) A and B **(F)** B and D (G) C and D

d) Applying a forward body bias to the PMOS transistor of a CMOS inverter may result in:

(A) higher gate delay (B) reduced sub-threshold leakage **(C)** lower gate delay
(D) lower NM (E) only B and C (F) only A and B (G) B, C and D (H) B and D

e) Consider an inverter with fanout of three. Ignore interconnect and diffusion capacitances for now. If a gate dielectric with higher k value (but same thickness) is used, then the inverter delay (ignoring any change in threshold voltage and mobility): **(3 pts)**

(A) decreases, since the drive current increases
(B) increases, since the gate capacitance increases
(C) does not change, since the drive current and capacitance both increase
(D) decreases, since increase in drive current is more than that of capacitance
(E) increases, since increase in capacitance is more than that of drive current

f) For the inverter in part (e), assume that the total capacitance is the sum of gate, interconnect and diffusion capacitance. If the gate oxide is thinned, then which of the following statement is most accurate? **(3 pts)**

(A) since the drive current increases, delay reduces
(B) since the total capacitance increases, delay increases
(C) since the drive current and total capacitance both increase, delay does not change
(D) increase in drive current is > the increase in total capacitance, hence delay reduces
(E) increase in total capacitance is > that of drive current, hence the delay increases

g) Typically a ratio of 2 for PMOS to NMOS transistor widths is used for an inverter, which gives a trip (switching) point of Vdd/2. If the NMOS channel length reduces due to process variations, which of the following statement is most accurate? **(3 pts)**

(A) trip point increases, and one of the noise margins increases
(B) trip point decreases, and one of the NMs increases while other decreases
(C) trip point increases, and one of the NMs increases while other decreases
(D) trip point doesn't change, and one of the NMs increases while other decreases
(E) trip point does not change, and noise margins do not change

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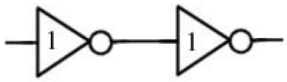
1. **Part II: (8 pts)** ***(suggested time: 8 minutes)*** As we know, the propagation delay of a CMOS inverter is:

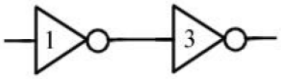
$$t_p = t_{p\,\mathrm{intrinsic}} + t_{pload} = t_{po}(1+\frac{f}{\gamma})$$

where f is effective fanout and γ is intrinsic output capacitance over input (gate) capacitance of the inverter.

If the delay of a chain of two minimum sized inverter, $t_{p1} = 5\ ns$,



and the delay of a chain of two inverters where the first is minimum sized and the second one is 3 times minimum, equals $t_{p2} = 7\ ns$.



Calculate t_{p0} and γ.

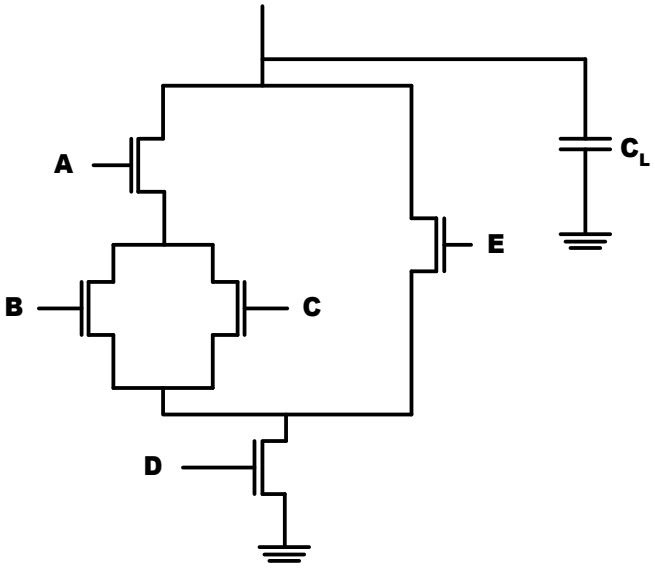
For the case of two minimum sized inverters, f =1 and $t_{p1} = t_{p0}$ (1+ 1/γ) = 5 ns……(1)

For the second case, f = 3, and $t_{p2} = t_{p0}$ (1+ 3/γ) = 7 ns……..(2)

Solving (1) and (2): t_{p1}/ t_{p2} = (1+1/ γ)/(1+3/ γ) = 5/7, which gives γ = 4

Substituting value of γ in (1) or (2) gives t_{p0}=4ns

1. **Part III: (10 pts)** ***(suggested time: 8 minutes)*** All transistors in the NMOS pull-down network below have a (W/L) ratio of α. Determine the best-case τ_{pHL}, if the worst-case τ_{pHL} is *9 ns*.



Worst case path (ABD) or (ACD):

Then worst-case $\tau_{pHL} \propto (\frac{L}{W})_{ABD} or (\frac{L}{W})_{ACD} = 3\times(\frac{L}{W})_A = 3\alpha^{-1}$

Best case when all transistors are ON:

Therefore equivalent

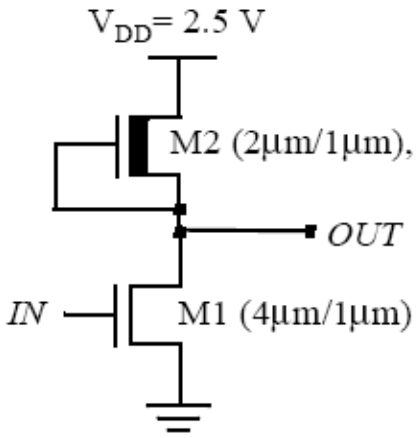
$$(\frac{L}{W})_{NMOS} = \alpha^{-1} + (\alpha^{-1} // (\alpha^{-1} + \alpha^{-1} // \alpha^{-1})) = \alpha^{-1} + (\alpha^{-1} // (\alpha^{-1} + 0.5\alpha^{-1}))$$

$$= \alpha^{-1} + (\alpha^{-1} // 1.5\alpha^{-1}) = \alpha^{-1} + \frac{3}{5}\alpha^{-1} = 1.6\alpha^{-1}$$

Since $\frac{\tau_{pHL\_best-case}}{\tau_{pHL\_worst-case}} = \frac{1.6}{3}$ therefore $\tau_{pHL\_best-case} = 9ns\times(\frac{1.6}{3}) = 4.8ns$

2. **(30 pts)** ***(suggested time: 20 minutes***) Consider the circuit shown below. Device M1 is a standard NMOS device. Device M2 has all the properties identical to M1, except that its device threshold voltage is negative and has a value of -0.5V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Also, assume that the input IN has a 0V to 2.5V swing.

Note: $I_{ds} = k_n \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$, where $k_n = \mu_n C_{ox} = 115\mu A/V^2$



i) Device M2 has its gate terminal connected to its source terminal. If VIN = 0V, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input? **(10 pts)**

When V_{IN} = 0V then M1 is off. M2 is on since V_{GS}=0 > V_{Tn2}. Since there is no current through M2, the drain to source voltage of M2 is 0 (linear mode). This means that V_{OUT}=2.5V.

ii) Compute the output voltage for V_{IN} = 2.5V. You may assume that V_{OUT} is small to simplify your calculation and V_{Dsat} = 0.265 V. In steady state, what is the mode of operation of device M2 for this input? **(10 pts)**

We assume that M1 is in the linear mode and M2 is velocity saturated. This means:

$$k_{n1}\frac{W_1}{L_1}\left[(2.5-0.5)V_{out} - \frac{V_{out}^2}{2}\right] = k_{n2}\frac{W_2}{L_2}\left[(0+0.5)V_{Dsat} - \frac{V_{Dsat}^2}{2}\right]$$

Since Vout is small we can neglect $V_{out}^2/2$ term and the previous equation becomes

$$V_{out} = \frac{k_{n2}}{k_{n1}}\frac{W_2/L_2}{W_1/L_1}\frac{(0+0.5)*0.265 - 0.265^2/2}{2.5-0.5}V = \frac{1}{2}\frac{0.1325-0.0351}{2}V = 24.35mV$$

Which gives *Vout* = 24.35 mV.
So our assumption is valid.

iii) Assuming the probability that (IN =0) = 0.4, what is the static power dissipation of this circuit? **(10 pts)**

There is static power dissipation when both transistors are on. This happens when V_{IN}=1. Then the static power dissipation is given by:

$$P_{static} = Pin = V_{DD} I_D$$

$$P_{static} = (1-0.4)2.5\left[\frac{115\mu A}{V^2}\frac{2}{1}\left(0.5\times V_{Dsat} - \frac{V_{Dsat}{}^2}{2}\right)\right]$$

$$= 0.6*2.5*115*2*(0.5*0.265 - 0.265^2/2)\mu W$$

$$= 33.6\ \mu W$$

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3. (35 pts) (suggested time: 25 minutes)

(a) Minimize the following switching function and implement in static CMOS style. You may assume that inverted inputs are available without skew. **(10 pts)**
$F(v, w, x, y, z) = \sum (1, 2, 6, 7, 9, 13, 14, 15, 17, 22, 23, 25, 29, 30, 31)$

Number locations on K-map:

v=0				
yz \ wx	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

v=1				
yz \ wx	00	01	11	10
00	16	20	28	24
01	17	21	29	25
11	19	23	31	27
10	18	22	30	26

Fill the K-map and circle common terms:

v=0				
yz \ wx	00	01	11	10
00	0	0	0	0
01	1	0	1	1
11	0	1	1	0
10	1	1	1	0

v=1				
yz \ wx	00	01	11	10
00	0	0	0	0
01	1	0	1	1
11	0	1	1	0
10	0	1	1	0

$F = \overline{x}\,\overline{y}z + wxz + xy + v\overline{w}\,\overline{y}\,\overline{z}$

Result: $F(v, w, x, y, z) = x'y'z + wxz + xy + v'w'yz'$

or $F(v, w, x, y, z) = [(x+y+z')\,(w'+x'+z')\,(x'+y')\,(v+w+y'+z)]'$

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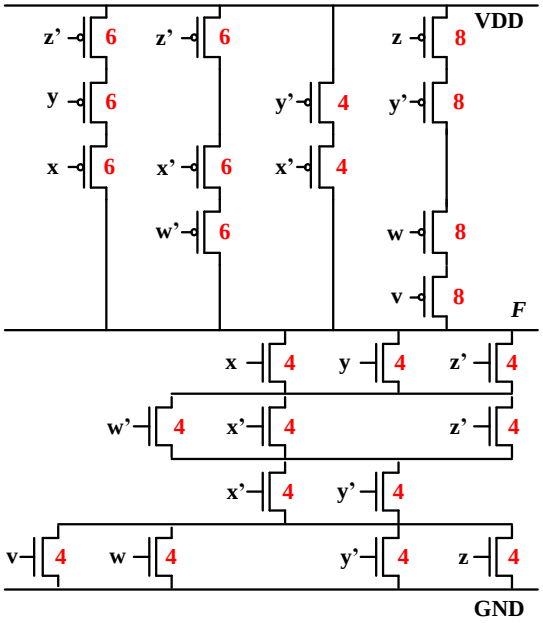
(b) Size the pull-up and pull-down transistors so that each stage is equivalent to a 2:1 inverter. **(12 pts)**

(c) Calculate the logical effort of the gate (for each input). **(7 pts)**



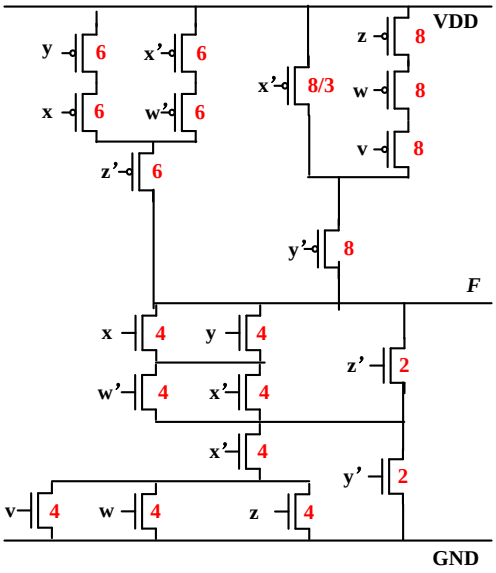
logical efforts			
input	**g**	**input**	**g**
v	**12/3**	**v'**	**0/3**
w	**12/3**	**w'**	**10/3**
x	**10/3**	**x'**	**18/3**
y	**10/3**	**y'**	**20/3**
z	**12/3**	**z'**	**20/3**

Note: This design is not the only solution. However, full points will be awarded for this answer.

Note that the function *F* can be further simplified as:

$$F(v, w, x, y, z) = [(z'+(x+y)*(w'+x'))*(y'+ x'*(v+w+z))]'$$

Hence, a better version of the circuit will be:



(d) Derive an expression for the worst-case pull-down delay of the gate in terms of the resistance of the minimum size NMOS (=R_0) and corresponding internal node capacitance (C_0) when driving an external load C_L. **(6 pts)**

The worst-case is varied by the design in (c). But the expression for the worst-case pull-down delay is always: ($4 R_0 C_L + 3R_0 C_0 + 2R_0 C_0 + R_0 C_0$)