Name: _____ **ECE 124A–Fall 2012**
Prof. K. Banerjee

Perm No. _____

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

MIDTERM EXAMINATION-ECE124A

Room: ESB-1003, November 9, 4:00-6:00 PM

READ CAREFULLY:

- **This is a CLOSED BOOK Exam. Any form of notes is not allowed. Calculators OK.**

- **READ the questions carefully before answering. Include all your answers in locations specified on these pages. Show ALL WORKING used to arrive at answers. Use space provided for all working. Use the back sides if necessary. There are 9 pages including the cover page. Be sure to write Your NAME/Perm No. on EVERY PAGE.**

Question	Scores
#1	/50
#2	/25
#3	/25
TOTAL	/100

Good Luck!

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1. Part I: (30 pts) (3 pts each) (suggested time: 25 minutes)

For each question, choose ALL the CORRECT statements among the four. Fill the table below with your answers:

Question	1	2	3	4	5	6	7	8	9	10
Answer	ACD	BD	AC	BD	BC	ABD	AD	B	ACD	C

(Completely correct: 3pts; Partially Correct: 1pt; Any wrong options chosen: 0 pt)

1) (Moore's law) Select the right statement(s): ACD

A. Transistors on Lead Microprocessors double every 2 years.
Correct. **Reference: Lecture 2, p. 14**

B. Die size grows by 2X every 2 years to satisfy Moore's Law.
Wrong. Die size grows much slower (7% every year), because when transistor number doubles, transistor size also reduces. **Reference: Lecture 2, p. 15**

C. Lead Microprocessor frequency doubles every 2 years.
Correct. **Reference: Lecture 2, p. 16**

D. Technology shrinks by 0.7/generation.
Correct. Think about Intel's "90nm","65nm","45nm",… **Reference: Lecture 2, p. 20**

2) (CMOS processing and layout) Select the right statement(s): BD

A. NMOS transistors are fabricated on n-type substrate.
Wrong. NMOS transistors are fabricated on p-type substrate. **Reference: Lecture 2, p. 25**

B. PMOS transistors have p^+-type source and drain.
Correct. **Reference: Lecture 2, p. 25**

C. Uninterrupted diffusion strips are possible only if there exists a common Euler path in the logic graph.
Wrong. An uninterrupted diffusion strip is possible only if there exists an Euler path in the logic graph. **Reference: Lecture 5, p. 22**

D. Gate of a transistor can be connected by a metal-to-poly via.
Correct. **Reference: Lecture 5, p. 7 and Lab 1**

3) (Semiconductor physics) Select the right statement(s): AC

A. A material is metallic if it has a half-filled energy band.
Correct. **Reference: Lecture 6, p. 9**

B. If the concentrations of donors and acceptors in a silicon sample are N_D and N_A, respectively, then the electron density is $n_0 \approx N_D - N_A$ at room temperature.
Wrong. It works only when $N_D > N_A$. When $N_D < N_A$, $p_0 \approx N_D - N_A$ at 300K and $n_0 = n_i^2 / p_0$
Reference: Lecture 6, p. 30 and Homework 3, prob. 2

C. The probability $F(E)$ of occupation of a state of energy E is less than 0.5 ($F(E)<0.5$) if $E>E_F$.
Correct. **Reference: Lecture 6, p. 17**

D. Drift current arises from electron motion due to differences in carrier concentration.
Wrong.
Drift current: Electron motion due to electric field
Diffusion current: Electron motion due to differences in carrier concentration
Reference: Lecture 6, p. 33

4) (Device physics, P-N Junction) Select the right statement(s): BD

A. In a P-N junction, the charges in the depletion region on p-side are due to positive fixed ions.
Wrong. The charges in the depletion region on p-side are due to negative fixed ions.
Reference: Lecture 7, p. 7

B. In a P-N junction in equilibrium, electron diffusion current and hole drift current are in the same direction.
Correct. **Reference: Lecture 7, p. 12**

C. The width of the depletion region is increased if the P-N junction is under forward bias.
Wrong. The width of depletion region is reduced under forward bias.
Reference: Lecture 7, p. 14

D. P-N junction capacitance reduces with reverse bias.
Correct. **Reference: Lecture 7, p. 18**

5) (Device physics, MOS) Select the right statement(s): BC

A. Work function of a semiconductor is the energy required to take electron from conduction band level to free space.
Wrong. It describes electron affinity. Work function of a semiconductor is the energy required to take electron from Fermi level to free space.
Reference: Lecture 7, p. 26

B. At equilibrium, Fermi levels line up in a MOS structure.
Correct. **Reference: Lecture 7, p. 26**

C. When inversion happens in NMOS, density of electrons on surface equal the density of holes in bulk.
Correct. **Reference: Lecture 7, p. 36**

D. Holes "accumulate" on Si surface if PMOS is in accumulation region.
Wrong. Holes "accumulate" on Si surface if NMOS is in accumulation region, or electrons "accumulate" on Si surface if PMOS is in accumulation region.
Reference: Lecture 7, p. 30

6) (Threshold voltage of MOSFET) Select the right statement(s): ABD

A. Increasing of fixed positive charged ions at boundary between oxide and substrate will increase the absolute value of threshold voltage of PMOS.
Correct. **Reference: Lectures 7-8**

B. For NMOS, V_T can be increased by adding acceptor ions in the channel.
Correct. **Reference: Lecture 8, p. 6**

C. the absolute value of PMOS threshold voltage increases as V_{SB} increases.
Wrong. For PMOS, threshold voltage (negative) increases as V_{SB} increases, while the absolute value decreases. **Reference: V_T formula in Lectures 7-8**

D. For NMOS, if t_{ox} increases, V_T will increase (assuming Q_{ox} is zero).
Correct. C_{ox} decrease, so V_T increases. **Reference: V_T formula in Lectures 7-8**

7) (MOSFET currents) Select the right statement(s): AD

A. MOSFET current is mainly due to motion of majority carrier.
Correct. It is one of the main differences compared with BJT.
Reference: Lecture 2, p. 2

B. Velocity saturation current varies quadratically with V_{GS}.
Wrong. For velocity saturation in short channel device, saturation current is in linear relationship with Vgs.
Reference: Lecture 8, p. 22

C. In short channel transistors, the mechanism of current saturation is velocity saturation.
Wrong. $\{V_{DS}>V_{DSAT}$, $V_{DSAT}<V_{GS}-V_T\}$ is velocity saturation region while $\{V_{DS}<V_{DSAT}$, $V_{DS}<V_{GS}-V_T\}$ is normal saturation in short channel device.
Reference: Lecture 8, p. 23

D. In linear region, drain current increases almost linearly with V_{GS}.
Correct. In linear region, drain current increasing almost linearly with V_{GS} or V_{DS}.
Reference: I_{DS} formula in Lecture 8, p. 17

8) (MOSFET capacitance) Select the right statement(s): B

A. Gate capacitance is due to diffusion capacitance.
Wrong. Gate capacitance is mainly oxide capacitance. **Reference: Lecture 9, p. 2**

B. Gate capacitance in saturation region is smaller than that in linear region.
Correct. It is one third smaller than that in linear region. **Reference: Lecture 9, p. 8**

C. In NMOS, drain diffusion capacitance increases if drain to body (V_{DB}) voltage increases.
Wrong. Drain diffusion capacitance increase if body to drain (V_{BD}) voltage (the forward bias of the junction) increases. **Reference: Lecture 9, p. 10**

D. The diffusion capacitances are parasitic capacitances, so they do not affect circuit performance.
Wrong. They do impact circuit performance. **Reference: Lecture 9, p. 13**

9) (MOSFET Leakage) Select the right statement(s): ACD

A. Gate leakage is independent of temperature (T).
Correct. It mainly arises from quantum tunneling.
Reference: Lecture 9, p. 16

B. Subthreshold swing (S) of MOSFET cannot be greater than 60 mV/decade.
Wrong. S cannot be lower than 60 mV/decade, which is a limitation of CMOS.
Reference: Lecture 9, p. 15

C. Electron mobility decreases with increase in T, hence, I_{DSAT} of NMOS decreases as T increases.
Correct. **Reference: Lecture 9, p. 19**

D. Junction leakage is less significant than gate and subthreshold leakage.
Correct. **Reference: Lecture 9, p. 17**

10) (CMOS Inverter) Select the right statement(s): C

A. Switching threshold (V_M) decreases if NMOS channel width reduces.
Wrong. NMOS becomes weaker; weaker pull-down shifts VTC to right
Reference: Lecture 10, p. 10

B. VTC shifts to left if PMOS oxide thickness reduces.
Wrong. PMOS becomes stronger; stronger pull-up shifts VTC to right
Reference: Lecture 10, p. 10

C. V_{IL} increases if PMOS is at a lower temperature than NMOS.
Correct. PMOS mobility increases; PMOS becomes stronger; stronger pull-up shifts VTC to right. V_{IL} increases.
Reference: Lectures 9-10

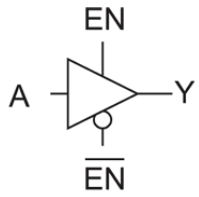
D. For a CMOS inverter in highest-gain region, both NMOS and PMOS are in resistive region.
Wrong. In highest-gain region (near V_M), both NMOS and PMOS are in saturation.
Reference: Lecture 10, p.5

1. Part II: (10 pts) (suggested time: 10 minutes)

What is a Tristate Buffer? Draw a schematic of the gate and the truth table. Using transistor level schematic, illustrate how this gate can be used to build i) an inverter and ii) a 2:1 Multiplexer.

Solution:

Tristate buffer consists of an NMOS and a PMOS with separate gate connections and common source and drain. Control signal S is applied to the gate of NMOS and its complimentary is applied to PMOS gate. When S=0, output is in tristate (Z is not driven by V_{in}) and when S=1, output Y= A.

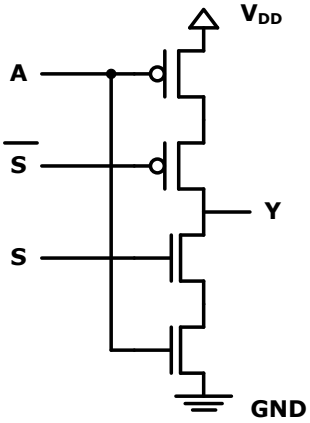


(2 pts)

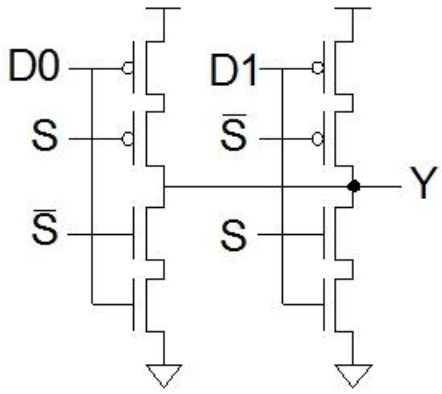
EN / $\overline{EN}$	A	Y
0/1	0	Z
0/1	1	Z
1/0	0	0
1/0	1	1

(2 pts)

Inverter **(3 pts)**



Multiplexer: **(3 pts)**



$\overline{Y} = D1S + D0\overline{S}$ (inverting MUX)

Reference: Lecture 3, pp.15-22

1. Part III: (10 pts) (suggested time: 10 minutes)

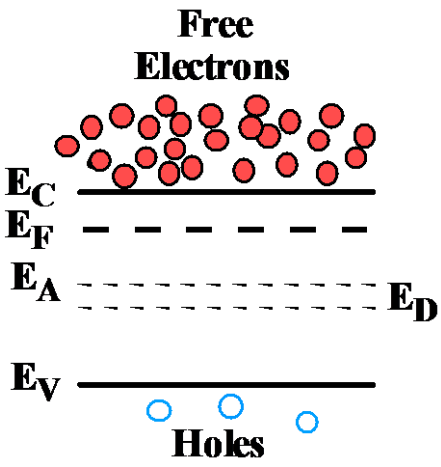
An unknown element X has been discovered in the planet of *Tatooine*. When an X atom sits on a lattice site in a Germanium crystal, it can act as either a donor or an acceptor. E_D and E_A levels both exist for the atom X and both are close to the middle of the Germanium bandgap. If a small concentration of X is placed in an n-type Germanium crystal, will the X behave as a donor or an acceptor? Explain with band diagrams.

Solution:

In n-type Germanium, the Fermi level will be in the upper half of the bandgap as shown in the band diagram below. Allowed energy levels below E_F will in general be occupied by electrons. Thus the E_D and E_A levels for X will have electrons filling them. This means the donor level will not have donated its electron whereas the acceptor level will have accepted an electron. **(3 pts)**

Thus the X atoms will act as ACCEPTORS in n-type Ge. **(2 pts)**

Reference: Lecture 6, pp. 22-32

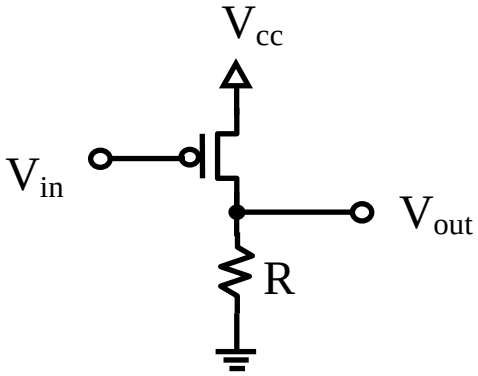


(Band diagram 5 pts)

2. (25 pts) (suggested time: 30 minutes)

Consider the PMOS resistive-load inverter shown below.

Vcc = 2.5V
V_{Tp} = -0.8 V
λ = 0
k_p' = 74 μA/V^2
R = 25 kΩ
L = 2 μm
W = 25 μm



For PMOS in linear region: $I_D = k_p'(\frac{W}{L})[(V_{GS} - V_{TP})V_{DS} - \frac{1}{2}V_{DS}^2]$

For PMOS in saturation region: $I_D = \frac{1}{2}k_p'(\frac{W}{L})(V_{GS} - V_{TP})^2$

(a) Find the values of V_{OL} (=V_{out} when V_{IN} =2.5V), V_{OH} (=V_{out} when V_{IN} =0 V) **(8 pts)**
Hint: Magnitude of the currents in PMOS and the resistor should be same.

Solution:

When input is logic 1, PMOS is in cutoff. Therefore V_{OL}=0V **(1 pt)**

When Vin=0V, PMOS in linear mode

$$I_D = k_p'(\frac{W}{L})[(V_{GS} - V_{TP})V_{DS} - \frac{1}{2}V_{DS}^2] \quad \textbf{(3 pt)}$$

$$= 74\frac{\mu A}{V^2}(\frac{25\mu m}{2\mu m})[(0V - 2.5V + 0.8V)(V_{OH} - 2.5V) - \frac{1}{2}(V_{OH} - 2.5V)^2]$$

$$= 925\frac{\mu A}{V^2}[-1.7V_{OH} + 4.25V - \frac{1}{2}V_{OH}^2 + 2.5V_{OH} - 3.125V] \text{----------(1)}$$

Also $V_{OH} = I_D R$ **i.e.** $I_D = \frac{V_{OH}}{R} = \frac{V_{OH}}{25000}$ ----------(2) **(3 pts)**

By solving equation 1 and 2, $V_{OH} = 2.44V$ **(1 pts)**

Reference: Lecture 10, pp. 18-19

(b) Find the values of V_M. **(9 pts)**

Solution:

When Vin=Vout=V_M , PMOS in saturation mode. **(2 pts)**
Reference: Lecture 10, p. 5

$$I_D = \frac{1}{2}k_p'(\frac{W}{L})(V_{GS}-V_{TP})^2 = \frac{1}{2}k_p'(\frac{W}{L})(V_M - V_{CC} - V_{TP})^2$$
$$= \frac{1}{2}74\frac{\mu A}{V^2}(\frac{25\mu m}{2\mu m})(V_M - 2.5V + 0.8V)^2$$

----------(1) **(3 pts)**

Also $V_M = I_D R$ **i.e.** $I_D = \frac{V_M}{R} = \frac{V_M}{25000}$ ----------(2) **(2 pts)**

By solving equation 1 and 2, $V_M = 1.36V$ **(2 pts)**

(c) Find a new value for R such that V_{OH} = 2.0V. **(8 pts)**

Solution:

From part (a)

$$I_D = k_p'(\frac{W}{L})[(V_{GS}-V_{TP})V_{DS} - \frac{1}{2}V_{DS}^2]$$
$$= 925\frac{\mu A}{V^2}[-1.7V_{OH} + 4.25V - \frac{1}{2}V_{OH}^2 + 2.5V_{OH} - 3.125V]$$

----------(1) **(3 pts)**

Also

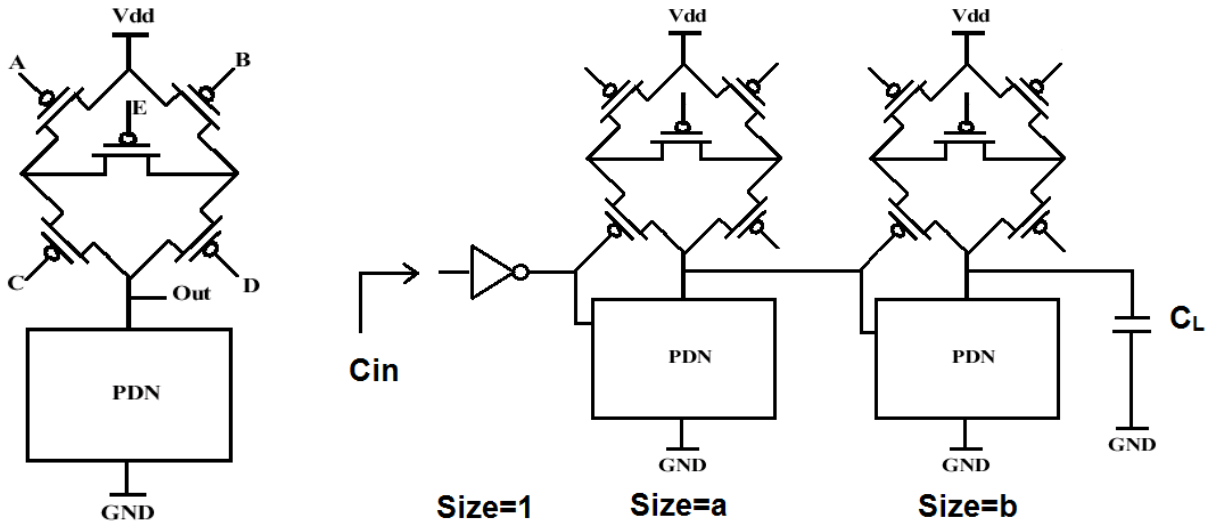
$V_{OH} = I_D R$ **i.e.** $I_D = \frac{V_{OH}}{R}$ ----------(2) **(2 pts)**

Let $V_{OH} = 2V$ then $R = 2.98k\Omega$ **(3 pts)**

3. (25 pts) (suggested time: 30 minutes)

Consider the CMOS logic gate shown below.

a) Determine the logic function of the gate.
b) Draw the pull-down network (ensure that you use a **minimum** number of **equal size** transistors).
c) What is the logical effort of this gate?
d) Two gates and a unit size inverter are in a circuit path as shown in the figure in the next page (no branching). Find the gate sizes a and b to achieve the minimum delay, assuming $C_L/C_{in}=10$.



Solution:

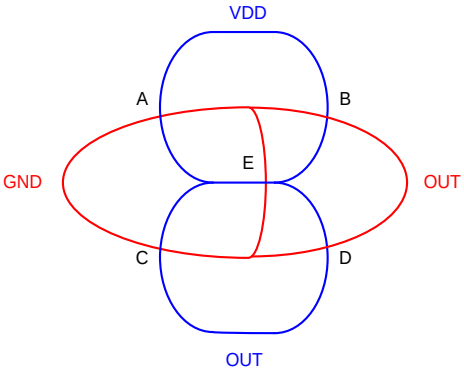
a) Logic function of the gate: **(4 pts)**

Out =

$$\overline{\overline{A}\overline{C}+\overline{B}\overline{D}+\overline{A}\overline{D}\overline{E}+\overline{B}\overline{C}\overline{E}}=\overline{(A+C)(B+D)(A+D+E)(B+C+E)}=AB+CD+ADE+BCE$$

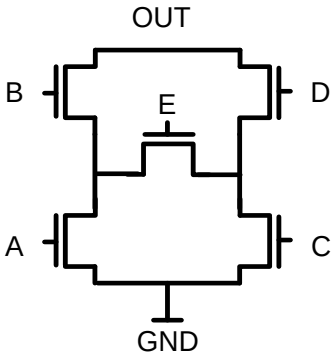
Reference: Lecture 3, pp. 2-9

b) Pull-down network (with a **minimum** number of equal-size transistors): **(6 pts)**
Logic diagram is as follows:

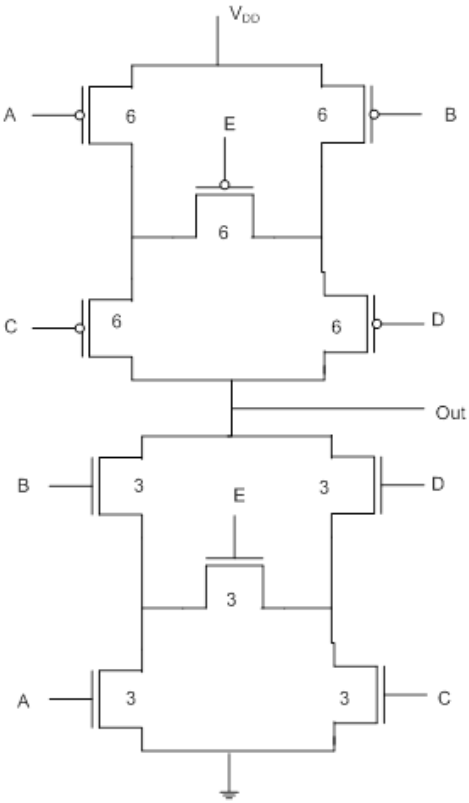


Reference: Lecture 5, pp. 18-20

PDN is then:



c) To calculate the logical effort, first size the PDN and PUN to achieve a 2:1 equivalent inverter. **(4 pts)**
Note: we have used equal size transistors for both the PUN and PDN.



Logical effort of this gate: (4 pts)
g = (6+3) / 3 = 3
Reference: Lecture 11, pp. 38

d) **Reference: Lecture 11, pp. 45-49**

Path electrical effort: $F = C_L/C_{in}=10$
Path logical effort: G = 1 x 3 x 3 = 9
Path branching effort: B=1 (no branching)

Path effort: H = GFB = 90 **(2 pts)**
Optimal gate effort: $h = H^{1/3} =4.5$ **(1pts)**

$h=g_if_i$ **(2pts)**
$f_1=h/g_1=4.5$
$f_2=h/g_2=1.5$
$f_3=h/g_3=1.5$

Hence, **(2pts)**
$a= f_1g_1/g_2 =1.5$
$b= f_1 f_2 g_1/g_3 =4.5 \times 1.5 \times 1 /3 = 2.25$

or (in different definition version)
$a=1.5 \times g_2=4.5$
$b= 2.25 \times g_3 = 6.75$