Name: __________________________

ECE 124A–Fall 2012
Prof. K. Banerjee

Perm No. ________________________

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

MIDTERM EXAMINATION-ECE124A

Room: ESB-1003, November 9, 4:00-6:00 PM

READ CAREFULLY:

- **This is a CLOSED BOOK Exam. Any form of notes is not allowed. Calculators OK.**

- **READ the questions carefully before answering. Include all your answers in locations specified on these pages. Show ALL WORKING used to arrive at answers. Use space provided for all working. Use the back sides if necessary. There are 9 pages including the cover page. Be sure to write Your NAME/Perm No. on EVERY PAGE.**

Question	Scores
#1	/50
#2	/25
#3	/25
TOTAL	/100

Good Luck!

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1. Part I: (30 pts) (3 pts each) (suggested time: 25 minutes)

For each question, choose ALL the CORRECT statements among the four. Fill the table below with your answers:

Question	1	2	3	4	5	6	7	8	9	10
Answer										

(Completely correct: 3pts; Partially Correct: 1pt; Any wrong options chosen: 0 pt)

1) (Moore's law) Select the right statement(s):

A. Transistors on Lead Microprocessors double every 2 years.
B. Die size grows by 2X every 2 years to satisfy Moore's Law.
C. Lead Microprocessor frequency doubles every 2 years.
D. Technology shrinks by 0.7/generation.

2) (CMOS processing and layout) Select the right statement(s):

A. NMOS transistors are fabricated on n-type substrate.
B. PMOS transistors have p^+-type source and drain.
C. Uninterrupted diffusion strips are possible only if there exists a common Euler path in the logic graph.
D. Gate of a transistor can be connected by a metal-to-poly via.

3) (Semiconductor physics) Select the right statement(s):

A. A material is metallic if it has a half-filled energy band.
B. If the concentrations of donors and acceptors in a silicon sample are N_D and N_A, respectively, then the electron density is $n_0 \approx N_D - N_A$ at room temperature.
C. The probability $F(E)$ of occupation of a state of energy E is less than 0.5 ($F(E)<0.5$) if $E>E_F$.
D. Drift current arises from electron motion due to differences in carrier concentration.

4) (Device physics, P-N Junction) Select the right statement(s):

A. In a P-N junction, the charges in the depletion region on p-side are due to positive fixed ions.
B. In a P-N junction in equilibrium, electron diffusion current and hole drift current are in the same direction.
C. The width of the depletion region is increased if the P-N junction is under forward bias.
D. P-N junction capacitance reduces with reverse bias.

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5) (Device physics, MOS) Select the right statement(s):

A. Work function of a semiconductor is the energy required to take electron from conduction band level to free space.
B. At equilibrium, Fermi levels line up in a MOS structure.
C. When inversion happens in NMOS, density of electrons on surface equal the density of holes in bulk.
D. Holes “accumulate” on Si surface if PMOS is in accumulation region.

6) (Threshold voltage of MOSFET) Select the right statement(s):

A. Increasing of fixed positive charged ions at boundary between oxide and substrate will increase the absolute value of threshold voltage of PMOS.
B. For NMOS, V_T can be increased by adding acceptor ions in the channel.
C. the absolute value of PMOS threshold voltage increases as V_{SB} increases.
D. For NMOS, if t_{ox} increases, V_T will increase (assuming Q_{ox} is zero).

7) (MOSFET currents) Select the right statement(s):

A. MOSFET current is mainly due to motion of majority carrier.
B. Velocity saturation current varies quadratically with V_{GS}.
C. In short channel transistors, the mechanism of current saturation is velocity saturation.
D. In linear region, drain current increases almost linearly with V_{GS}.

8) (MOSFET capacitance) Select the right statement(s):

A. Gate capacitance is due to diffusion capacitance.
B. Gate capacitance in saturation region is smaller than that in linear region.
C. In NMOS, drain diffusion capacitance increases if drain to body (V_{DB}) voltage increases.
D. The diffusion capacitances are parasitic capacitances, so they do not affect circuit performance.

9) (MOSFET Leakage) Select the right statement(s):

A. Gate leakage is independent of temperature (T).
B. Subthreshold swing (S) of MOSFET cannot be greater than 60 mV/decade.
C. Electron mobility decreases with increase in T, hence, I_{DSAT} of NMOS decreases as T increases.
D. Junction leakage is less significant than gate and subthreshold leakage.

10) (CMOS Inverter) Select the right statement(s):

A. Switching threshold (V_M) decreases if NMOS channel width reduces.
B. VTC shifts to left if PMOS oxide thickness reduces.
C. V_{IL} increases if PMOS is at a lower temperature than NMOS.
D. For a CMOS inverter in highest-gain region, both NMOS and PMOS are in resistive region.

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1. Part II: (10 pts) (suggested time: 10 minutes)

What is a Tristate Buffer? Draw a schematic of the gate and the truth table. Using transistor level schematic, illustrate how this gate can be used to build i) an inverter and ii) a 2:1 Multiplexer.

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1. Part III: (10 pts) (suggested time: 10 minutes)

An unknown element X has been discovered in the planet of *Tatooine*. When an X atom sits on a lattice site in a Germanium crystal, it can act as either a donor or an acceptor. E_D and E_A levels both exist for the atom X and both are close to the middle of the Germanium bandgap. If a small concentration of X is placed in an n-type Germanium crystal, will the X behave as a donor or an acceptor? Explain with band diagrams.

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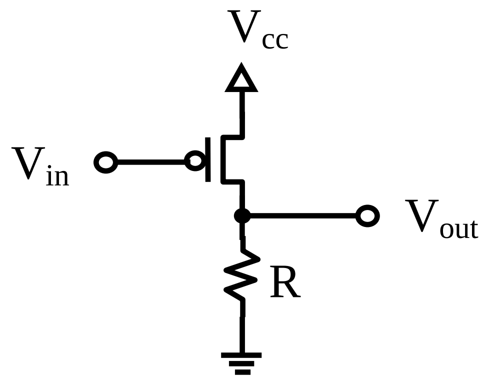
2. (25 pts) (suggested time: 30 minutes)

Consider the PMOS resistive-load inverter shown below.

Vcc = 2.5V
V_{T0p} = -0.8 V
$\lambda = 0$
k_p' = 74 $\mu A/V^2$
R = 25 kΩ
L = 2 μm
W = 25 μm



For PMOS in linear region: $I_D = k_p'(\frac{W}{L})[(V_{GS} - V_{TP})V_{DS} - \frac{1}{2}V_{DS}^2]$

For PMOS in saturation region: $I_D = k_p'(\frac{W}{L})(V_{GS} - V_{TP})^2 = k_p'(\frac{W}{L})(V_M - V_{CC} - V_{TP})^2$

(a) Find the values of V_{OL} (=V_{out} when V_{IN} =2.5V), V_{OH} (=V_{out} when V_{IN} =0 V) **(8 pts)**
Hint: Magnitude of the currents in PMOS and the resistor should be same.

(b) Find the values of V_M. **(9 pts)**

(c) Find a new value for R such that $V_{OH} = 2.0V$. **(8 pts)**

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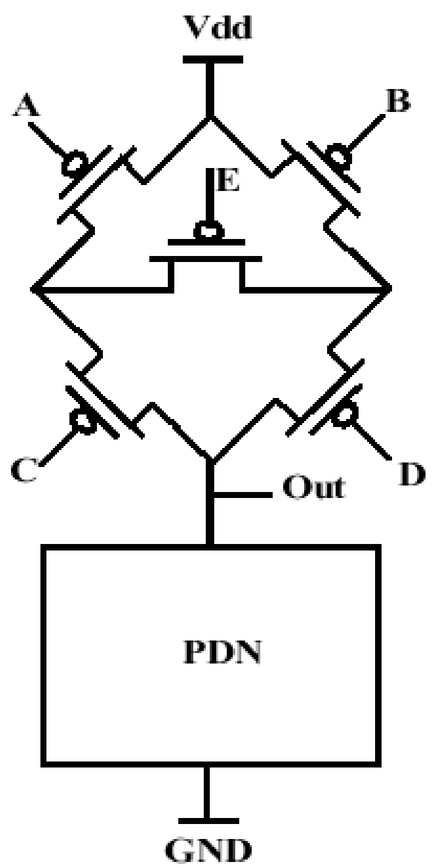
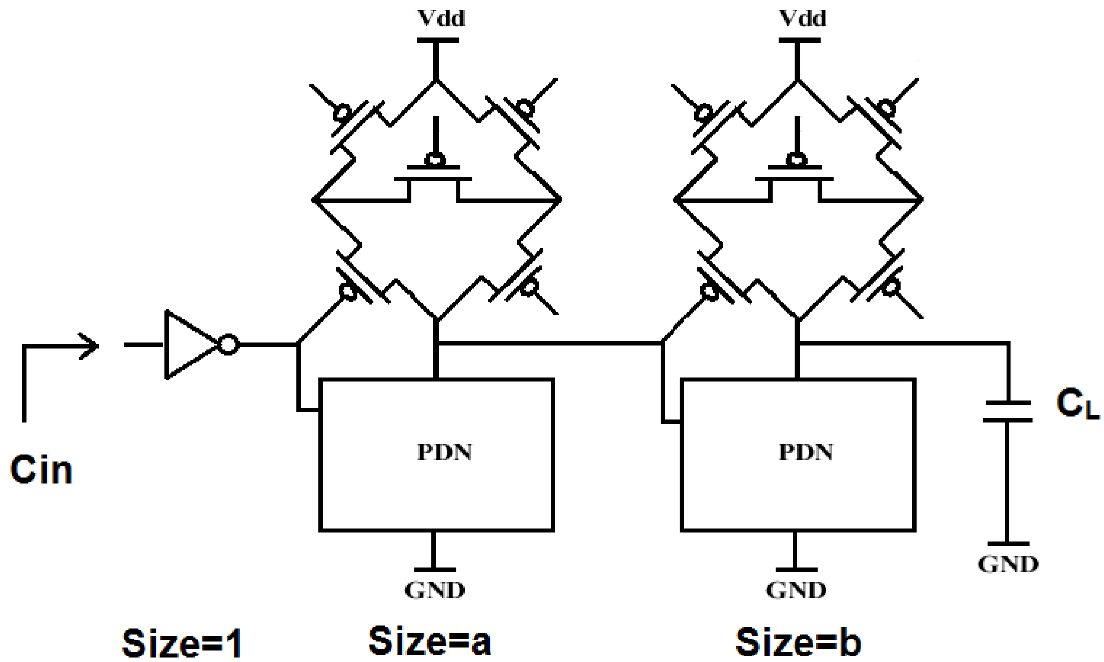
3. (25 pts) (suggested time: 30 minutes)

Consider the CMOS logic gate shown below.

a) Determine the logic function of the gate.
b) Draw the pull-down network (ensure that you use a **minimum** number of **equal size** transistors).
c) What is the logical effort of this gate?
d) Two gates and a unit size inverter are in a circuit path as shown in the figure in the next page (no branching). Find the gate sizes a and b to achieve the minimum delay, assuming C_L/C_{in}=10.




Vdd
Vdd
PDN
PDN
CL
Cin
GND
GND
GND
Size=1
Size=a
Size=b