## **HSPICE Simulation Example**

## Jiahao Kang

| <pre>* Tutorial: An Simulation Example using HSPICE     # By Jiahao Kang * F=(A+B)'+(CD)'</pre>  | First line in a SPICE deck is always a comment (with or without *). |
|--|---|
| .TITLE Example   |   |
| **************************************   |   |
| .INCLUDE '65nm_bulk.pm'  | Define parameters with .param                                       |
| **************************************   | Can define parameter based on other parameters or expressions.      |
| • PARAM VDD=1<br>+ LMOS =65n   | Use '+' to continue long lines on                                   |
| + WN =65n<br>+ WP ='2*WN'  | the proceeding line.  |
| **************************************   | Here's how you can do arithmetic on your parameters.                |
| VA A 0 pulse 0 VDD 0.2n 0.2n 0.2n 1n 2n<br>VB B 0 pulse 0 VDD 0.2n 0.2n 0.2n 1n 2n<br>VC C 0 pulse 0 VDD 0.2n 0.2n 0.2n 1n 2n<br>VD D 0 pulse 0 VDD 0.2n 0.2n 0.2n 1n 2n |   |
|  | First vdd is the voltage source.<br>Second vdd is the node.         |
| ***** Define global nodes for use in subcircuits *****   | Third vdd is the parameter  |
| .GLOBAL VDD  |   |
| ************* Define subcircuits (modules) *************   | Subcircuits are SPICE's way of                                      |
| .SUBCKT INV X Y<br>M1 Y X O O NMOS L=LMOS W=WN<br>M2 Y X VDD VDD PMOS L=LMOS W=WP<br>.ENDS   | defining modules repeated in your design.                           |
| .SUBCKT NAND2 A B Y<br>M1 1 B 0 0 NMOS L=LMOS W=WN<br>M2 Y A 1 0 NMOS L=LMOS W=WN<br>M3 Y A VDD VDD PMOS L=LMOS W=WP<br>M4 Y B VDD VDD PMOS L=LMOS W=WP<br>.ENDS         |   |
| .SUBCKT NOR2 A B Y<br>M1 Y B O O NMOS L=LMOS W=WN<br>M2 Y A O O NMOS L=LMOS W=WN<br>M3 Y A 1 VDD PMOS L=LMOS W=WP<br>M4 1 B VDD VDD PMOS L=LMOS W=WP<br>.ENDS            |   |
| ******************** Define main circuit ************************************  |   |
| * F=(A+B)'+(CD)'<br>X1 A B 1 NOR2  |   |
| X2 C D 2 NAND2<br>X3 1 2 xF NOR2<br>X4 xF F INV<br>* Load capacitance<br>CL F 0 0.1p   | Instantiate modules like so.  |

| ****************************** Anlysis Options ********************   | Power measurements   |
|---|--|
| .TRAN 0.1p 2n<br>.MEAS TRAN avgpower AVG power FROM=Ons TO=2ns<br>.MEAS TRAN tdlay TRIG V(A) VAL='VDD/2' RISE=1<br>+ TARG V(F) VAL='VDD/2' FALL=1<br>****** Alter the parameters and run again ********** | Measure propagation delays<br>accurately using the '.meas'<br>statement. Outputs are written<br>to .lis file.  |
| ALTER CASE 2: WP=WN<br>PARAM WP = '1*WN'<br>ALTER CASE 3: Increase Vdd by 10%<br>PARAM VDD = 1.1  | Here we trigger when the voltage<br>at node 'A' crosses vdd/2, and<br>measure the time until the output<br>crosses vdd/2   |
| ALTER CASE 4: Change load capacitance<br>CL F 0 0.01p<br>.ALTER CASE 5: Change temperature<br>.TEMP 70<br>.ALTER CASE 6: Change stimulii<br>VA A 0 DC 0   | .ALTER statements allows us to<br>modify the circuit and run again.<br>They must be before the final .end<br>statement. Note: ALTER blocks are<br>incremental!!! |
| VD D O DC VDD<br>.END   |  |