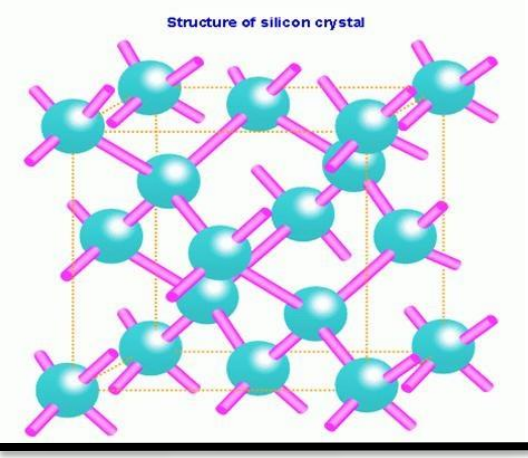
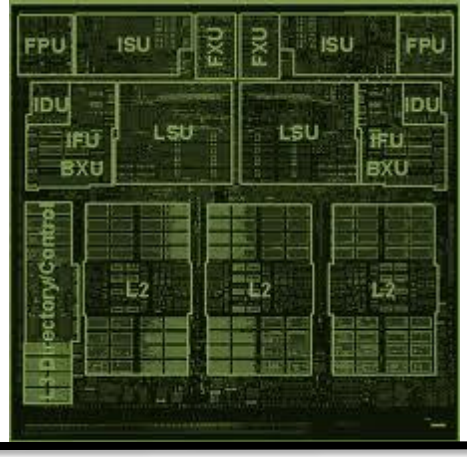
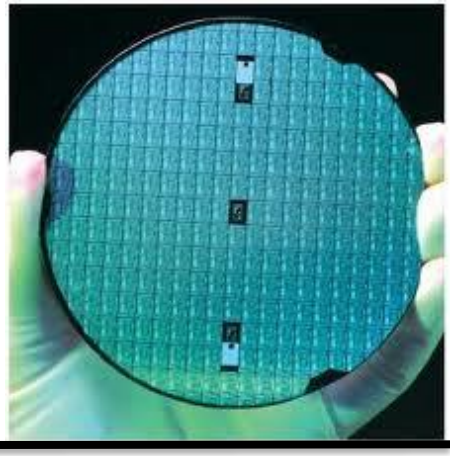






ECE 122A

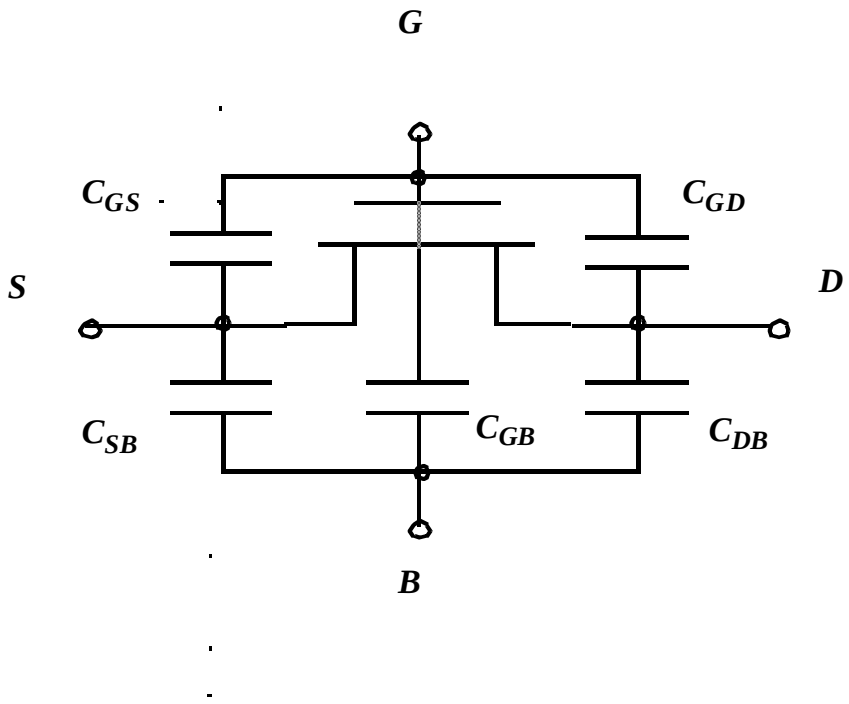
VLSI Principles

Lecture 8

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

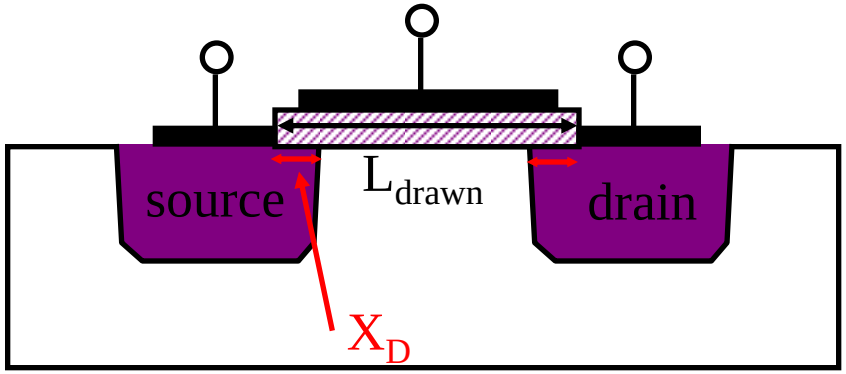
Dynamic Behavior of MOS Transistor

- Oxide Capacitance
  - Gate to Source overlap
  - Gate to Drain overlap
  - Gate to Channel/Bulk
- Junction Capacitance
  - Source to Bulk junction
  - Drain to Bulk junction



Oxide capacitances

Overlap

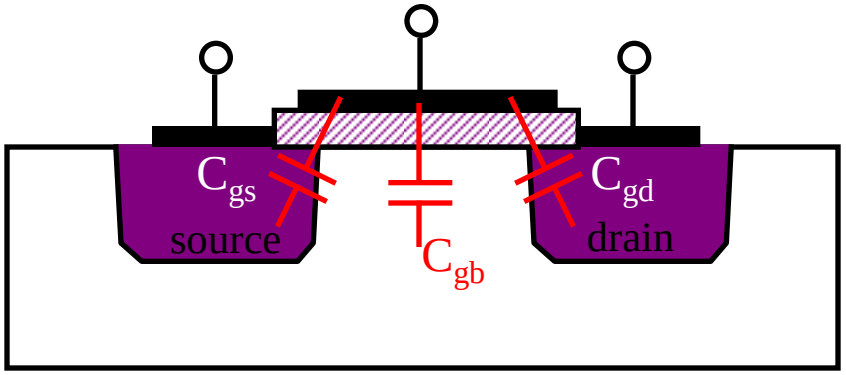


- Overlap capacitances
  - gate electrode overlaps source and drain regions
  - X_D is overlap length on each side of channel
  - $L_{eff} = L_d - 2X_D$
  - Total overlap capacitance:

$$C_{overlap} = C_{GSO} + C_{GDO} = 2C_{ox}WX_D$$

Oxide capacitances

Channel



- Channel capacitances
  - Gate-to-source: C_{gs}
  - Gate-to-drain: C_{gd}
  - Gate-to-bulk: C_{gb}

- Cutoff:
  - No channel connecting source and drain
  - $C_{gs} = C_{gd} = 0$
  - $C_{gb} = C_{ox}WL_{eff}$
  - Total channel capacitance $C_{GC} = C_{ox}WL_{eff}$

Oxide capacitances

Channel

- Linear mode
  - Channel spans from source to drain
  - Capacitance split equally between S and D

$$C_{GS} = \frac{1}{2} C_{ox} W L_{eff} \qquad C_{GD} = \frac{1}{2} C_{ox} W L_{eff} \qquad C_{GB} = 0$$

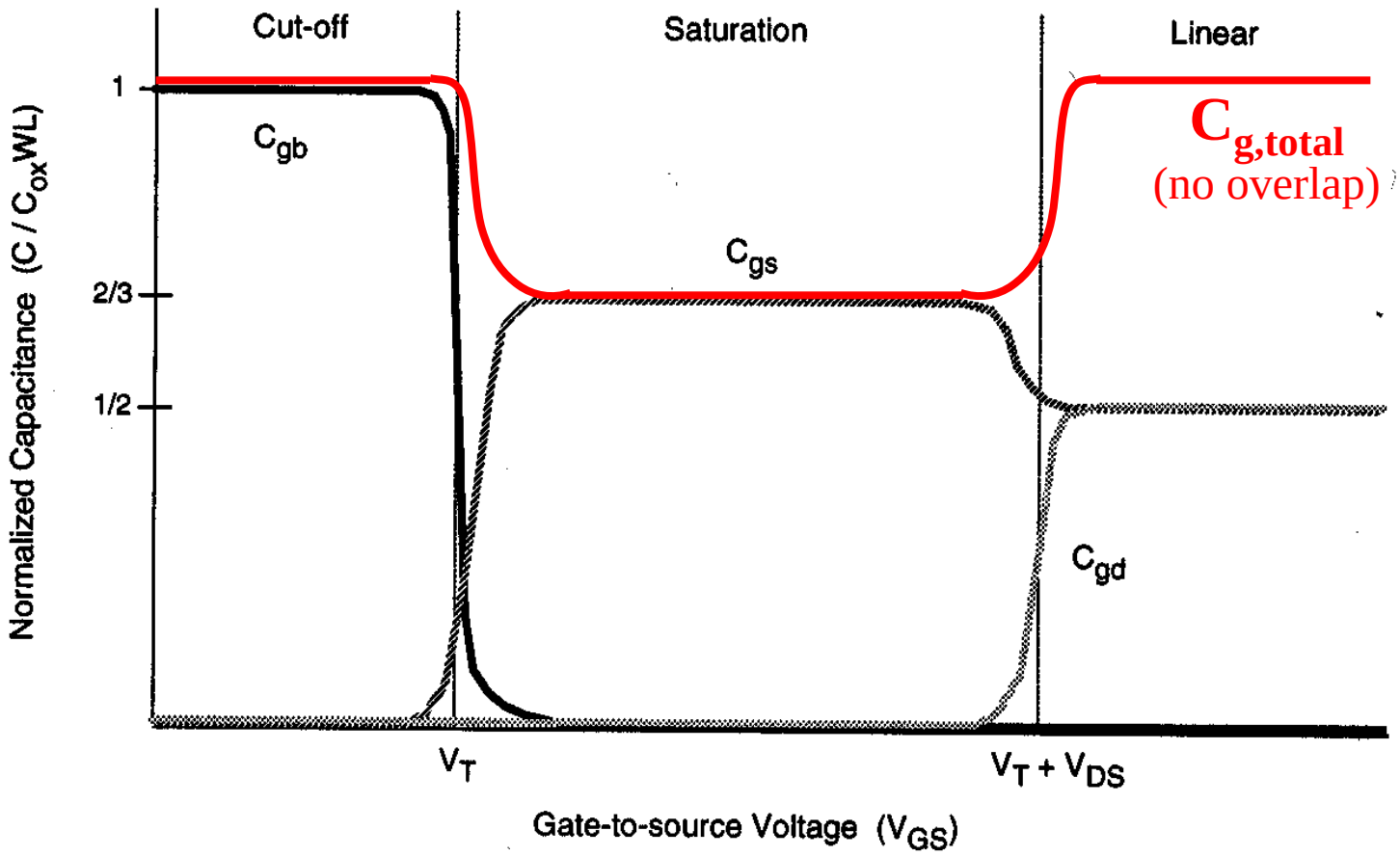
  - Total channel capacitance $C_{GC} = C_{ox} W L_{eff}$
- Saturation mode
  - Channel is pinched off:

$$C_{GD} = 0 \qquad C_{GS} = \frac{2}{3} C_{ox} W L_{eff} \qquad C_{GB} = 0$$

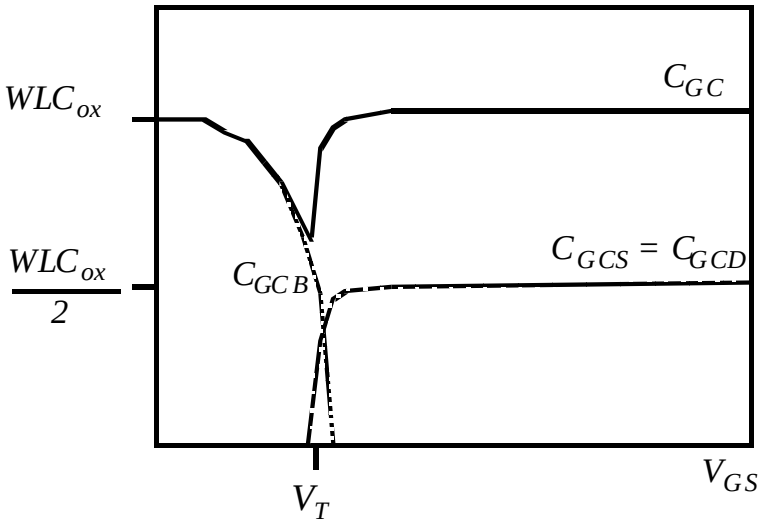
  - Total channel capacitance $C_{GC} = 2/3\ C_{ox} W L_{eff}$

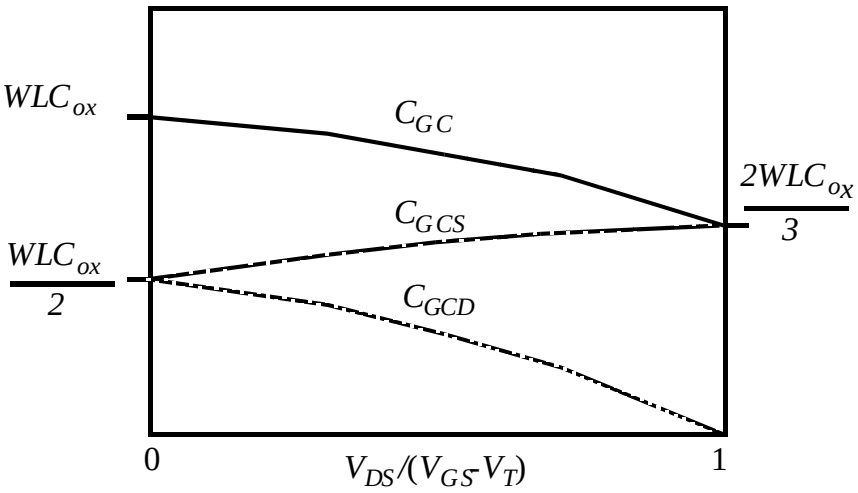
Oxide capacitances

Channel



Gate-to-Channel Capacitance



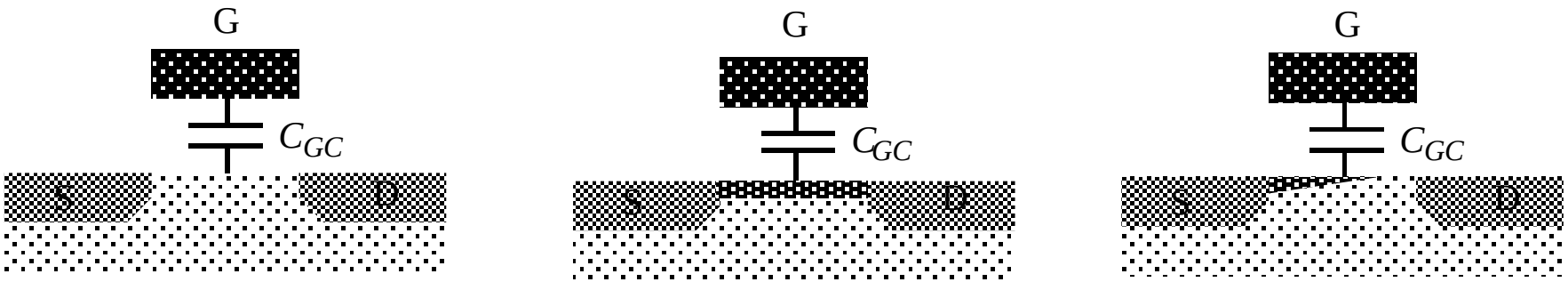


Capacitance as a function of V_{GS} (with $V_{DS} = 0$)

Capacitance as a function of the degree of saturation

Bottom Line: Cap. components are non-linear

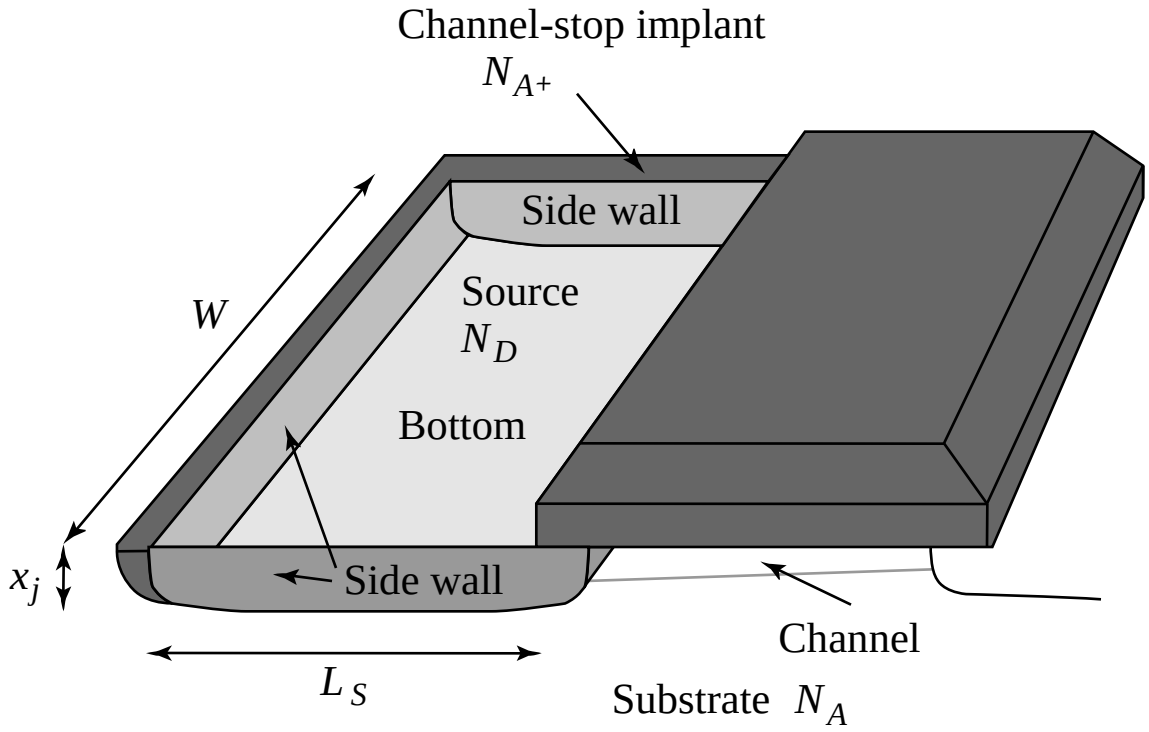
Gate-to-Channel Capacitance (summary)



$$C_{GC} = C_{gb} + C_{gs} + C_{gd}$$

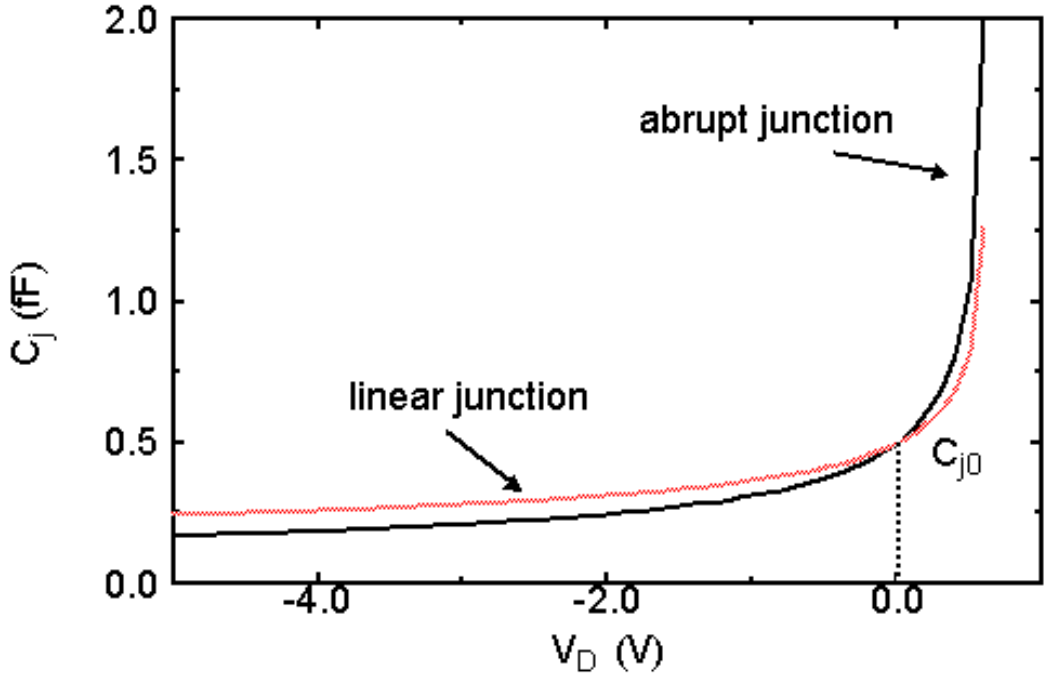
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Resistive	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Capacitances in 0.25 μm CMOS Process

	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MOS Cap. Summary

In general, these capacitances are non-linear and voltage dependent….

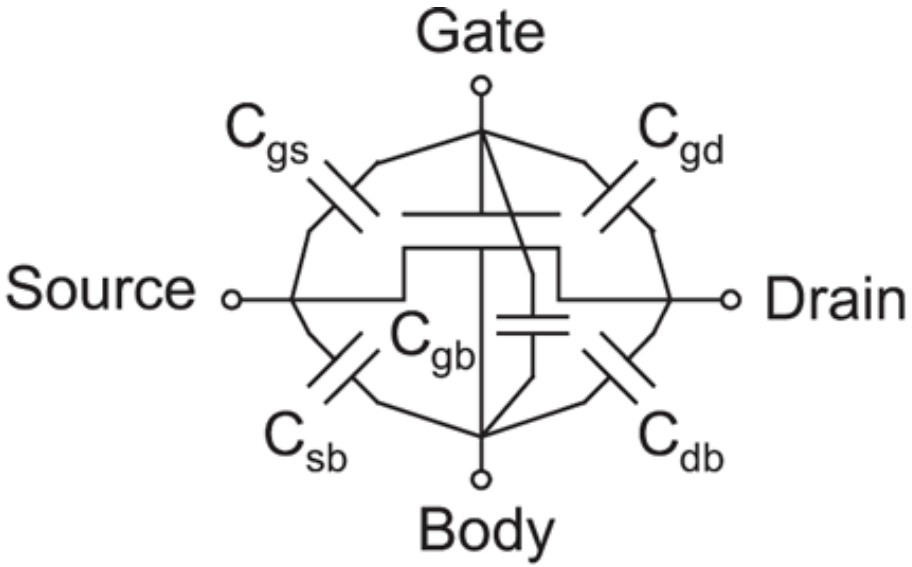


FIG 2.14 Capacitances of an MOS transistor

Note: The diffusion capacitances, C_{sb} and C_{db} are parasitic capacitances….but they do impact circuit performance

Data Dependency

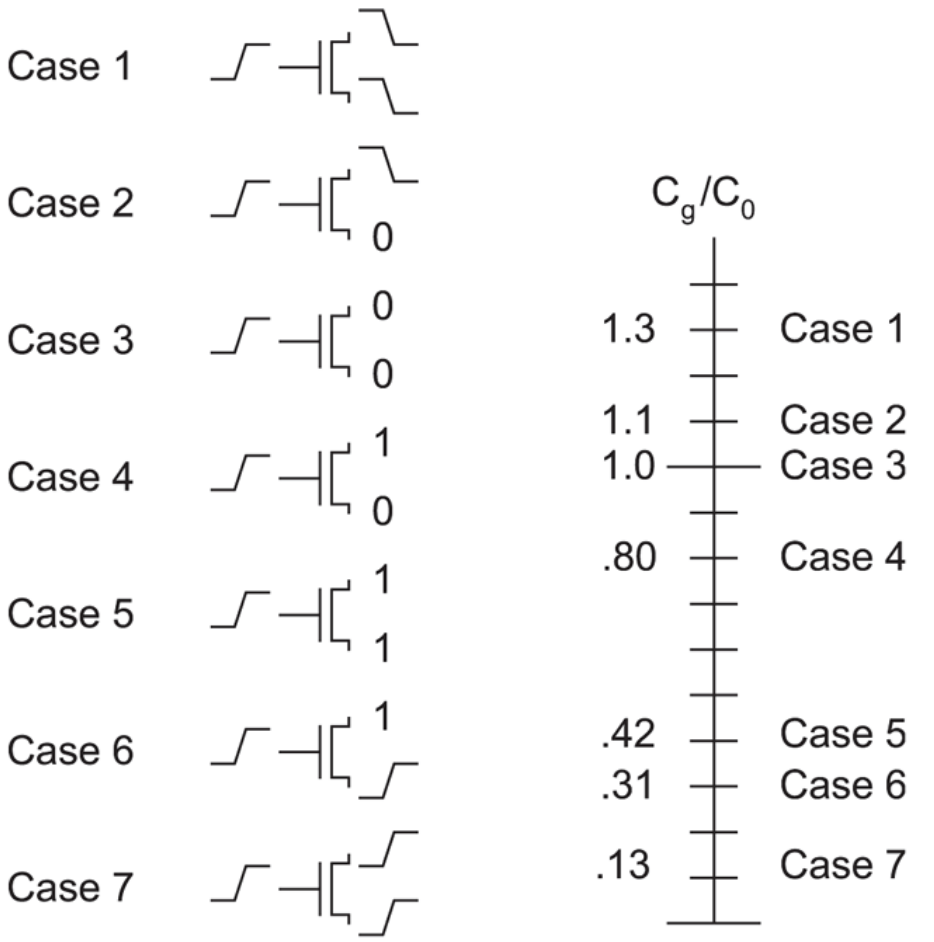
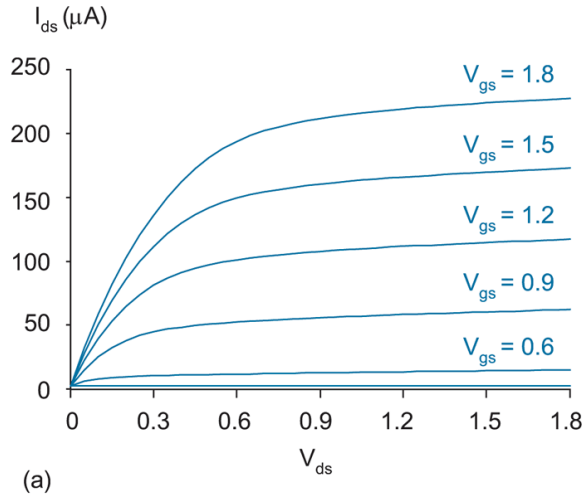


FIG 2.12 Data-dependent gate capacitance

Effective gate capacitance (C_g) varies with the switching activity of the source and drain….

Think about a parallel plate capacitor…with the each electrode tied to the same voltage or different voltages…

Subthreshold Leakage



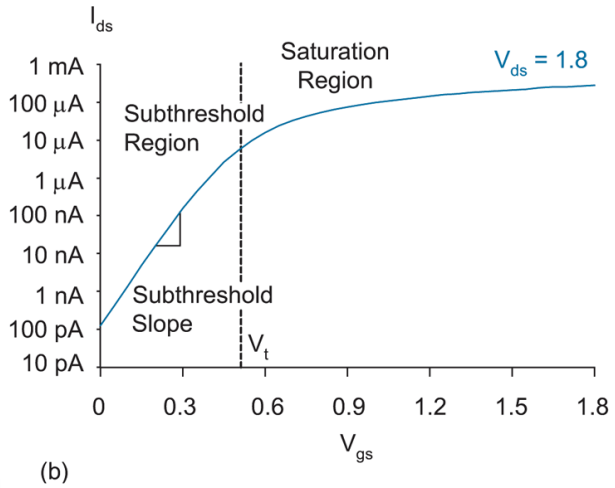


FIG 2.15 Simulated I-V characteristics

- Dominant leakage mechanism
- Function of both V_{GS} and V_{DS}
- Increases exponentially as temperature increases or Vt decreases…..

How much do we need to reduce V_{GS} for Ids to drop by a factor of 10…..

Subthreshold swing (S) = (subthreshold slope)$^{-1}$

$$S = n\,(kT/q)\,\ln(10)$$

For ideal transistor with sharpest possible roll-off, n=1 and S=60 mV/decade

…a fundamental limit for MOSFETs!!!

Gate Leakage (Direct Tunneling)

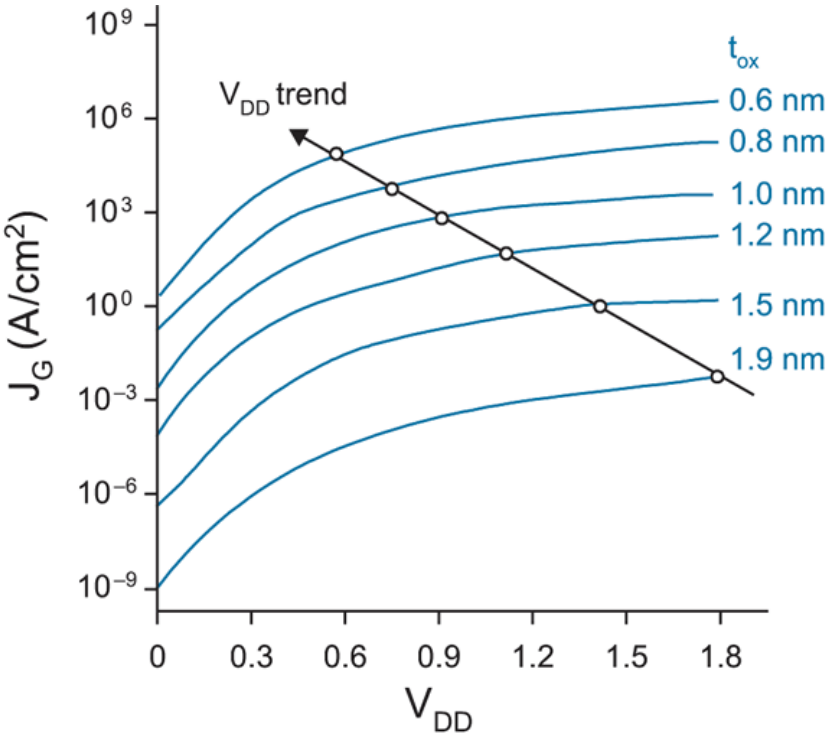


FIG 2.20 Gate leakage current from [Song01]

- *Increases with gate oxide (SiO2) scaling*
- *High-k gate oxides can be used to lower gate leakage*
- *Independent of temperature*

Junction Leakage

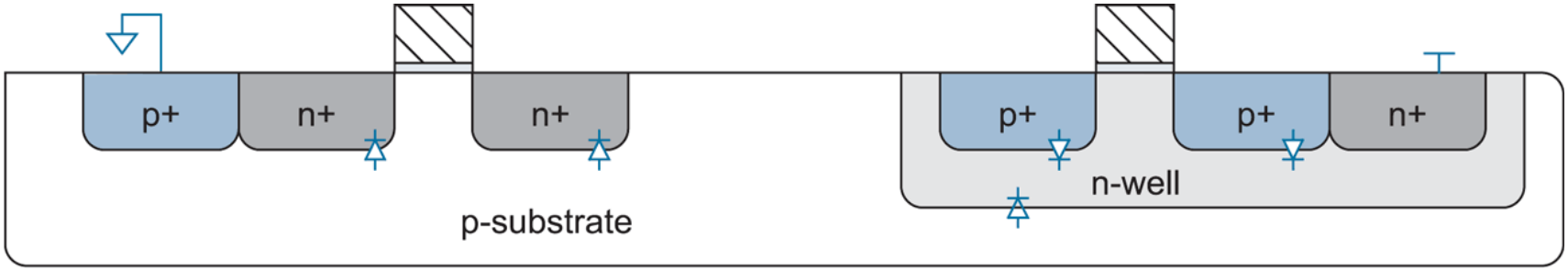


FIG 2.19 Reverse-biased diodes in CMOS circuits

- *Less significant than gate and subthreshold leakage*
- *Increases with temperature*

Temperature Effects

- *Mobility decreases with increase in T*
- *V_t decreases linearly with T*

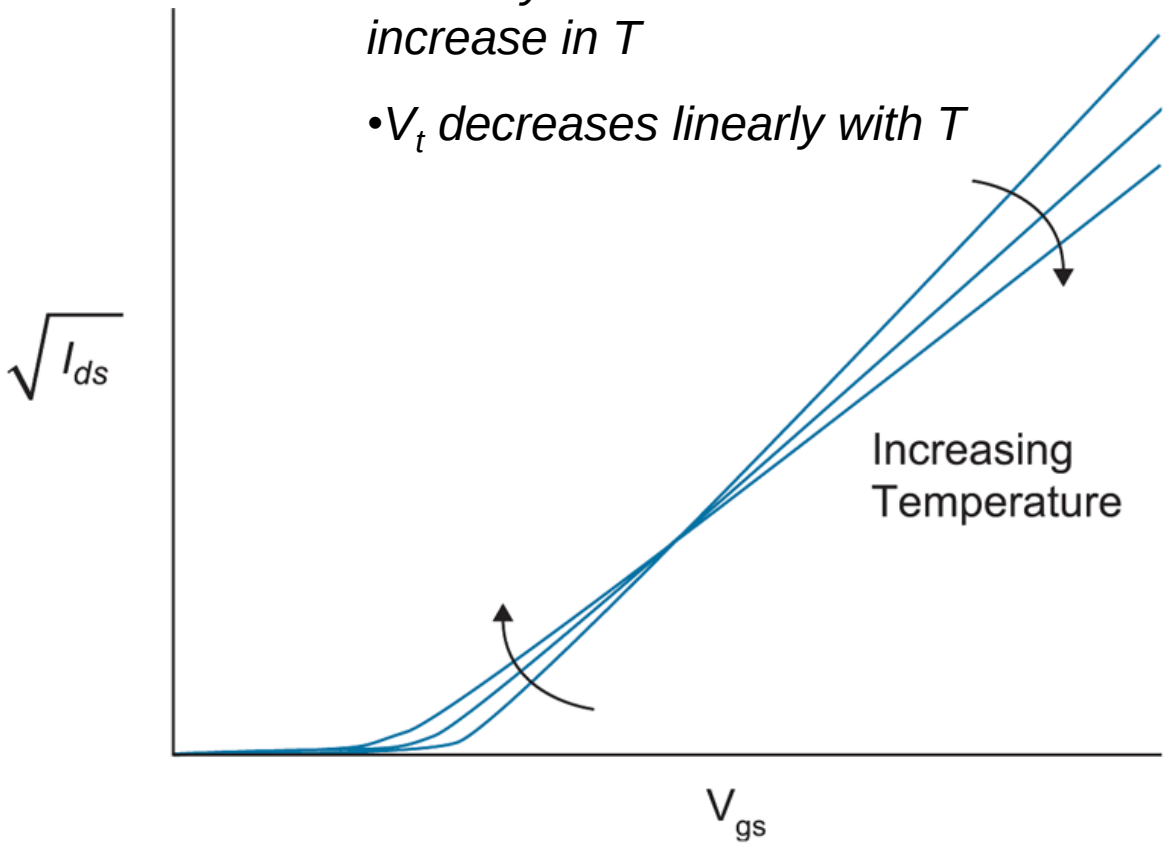


FIG 2.21 I–V characteristics of nMOS transistor in saturation at various temperatures

Temperature Effects

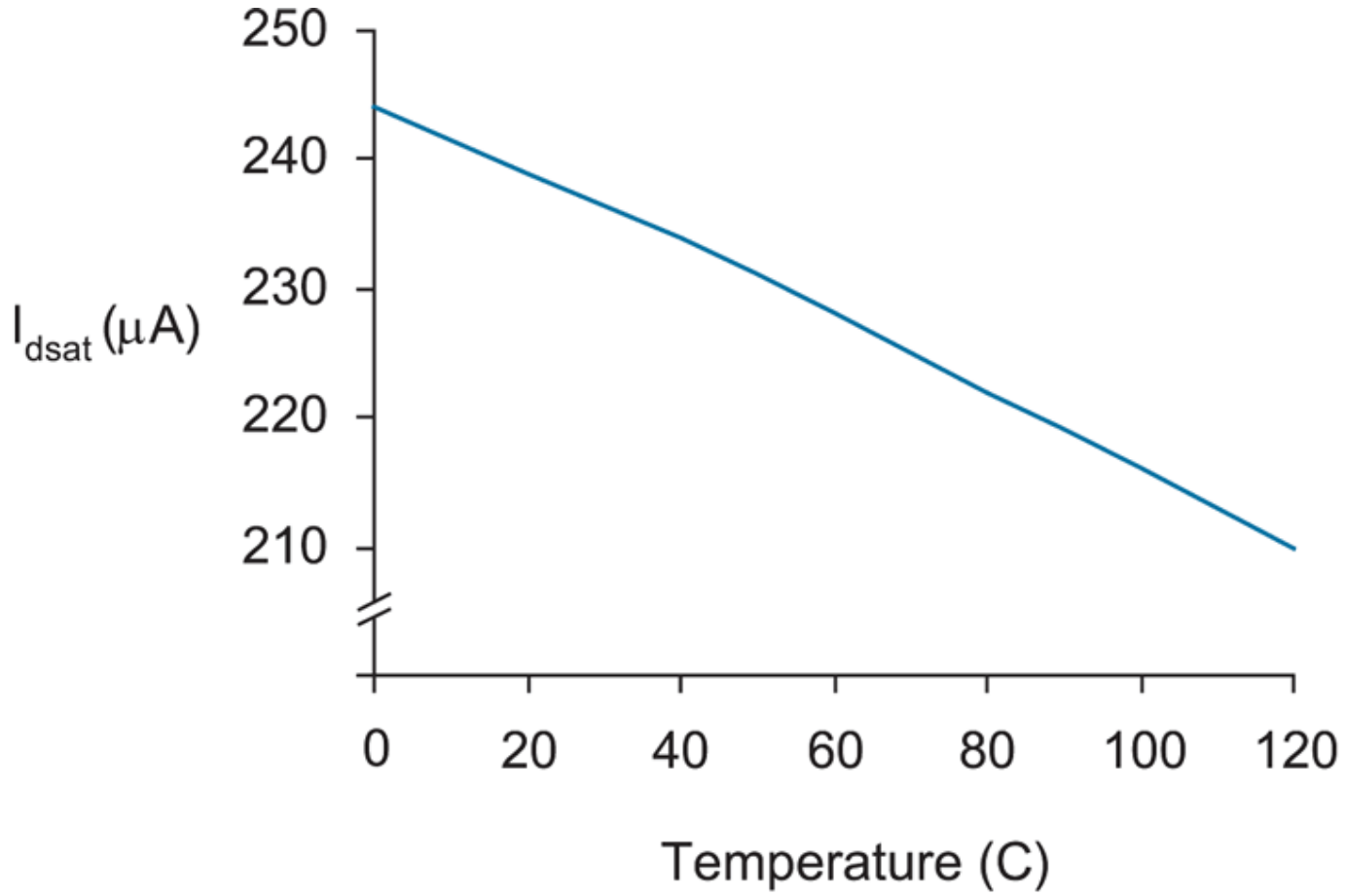


FIG 2.22 I_{dsat} vs. temperature

Temperature Effects

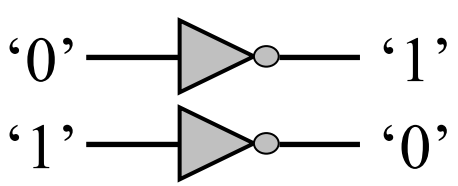
Chip Cooling can:

1. *Improve Circuit performance*
   - *speed up transistors since mobility improves*
   - *decrease the delay of interconnects since metal resistance decreases with temperature*
   - *Lowers junction capacitance (increases depletion width)*
2. *Decrease leakage (mainly subthreshold)*
3. *Improve reliability of the chip*

For more detailed info. read the paper posted on the class web site: "Cool Chips: Opportunities and Implications for Power and Thermal Management", by S-C. Lin and K. Banerjee, IEEE Transactions on Electron Devices, vol. 55, No. 1, 2008, 245-255

Inverter Operation

- Inverter is the simplest digital logic gate

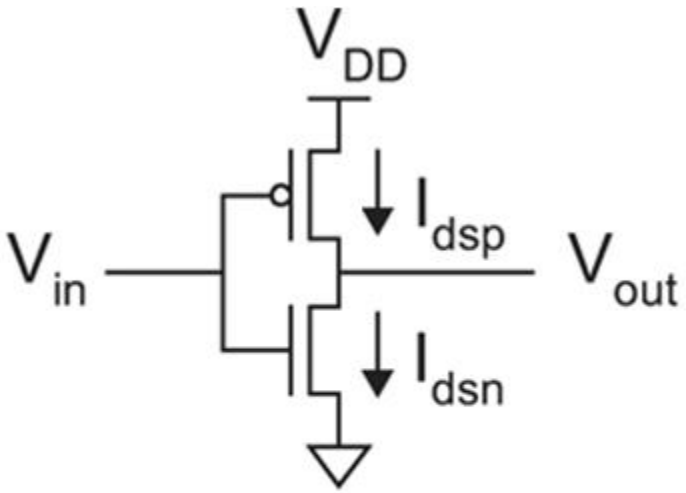


In	Out
0	1
1	0

- Many different circuit styles possible
  - CMOS
  - Resistive-load
  - Pseudo-NMOS
  - Dynamic
- Important characteristics
  - Performance (operating speed or delay through the gate)
  - Power/Energy consumption
  - Robustness (tolerance to noise)
  - Cost (complexity and area)

CMOS Inverter

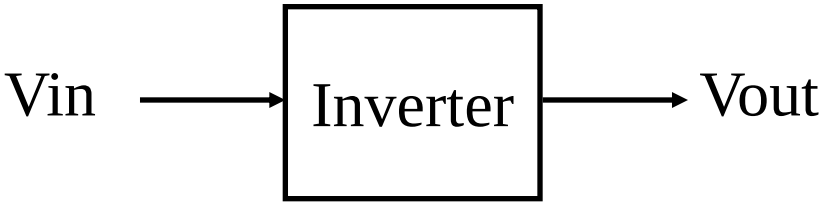
The most widely used gate….

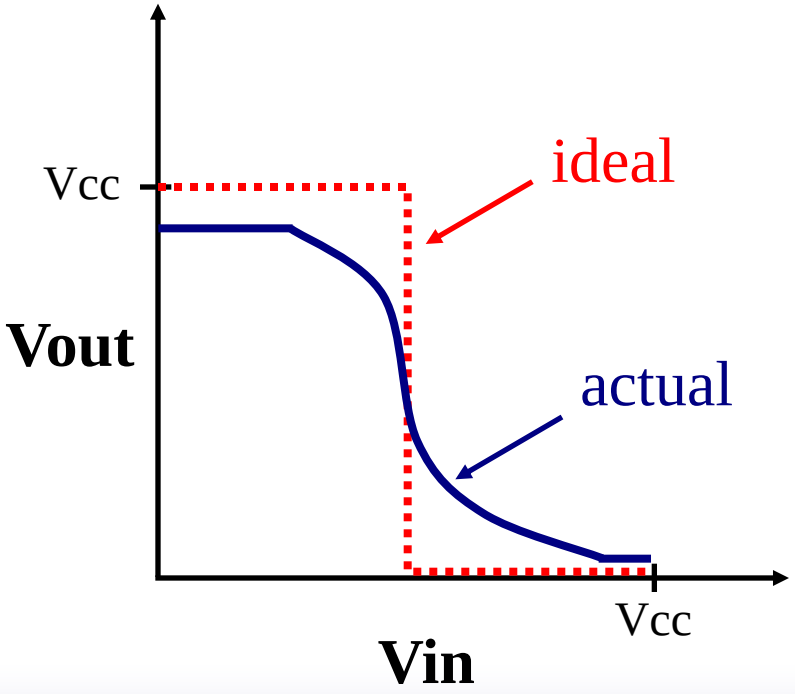


A CMOS inverter

Inverter model: VTC

Voltage transfer curve (VTC): plot of output voltage Vout vs. input voltage Vin

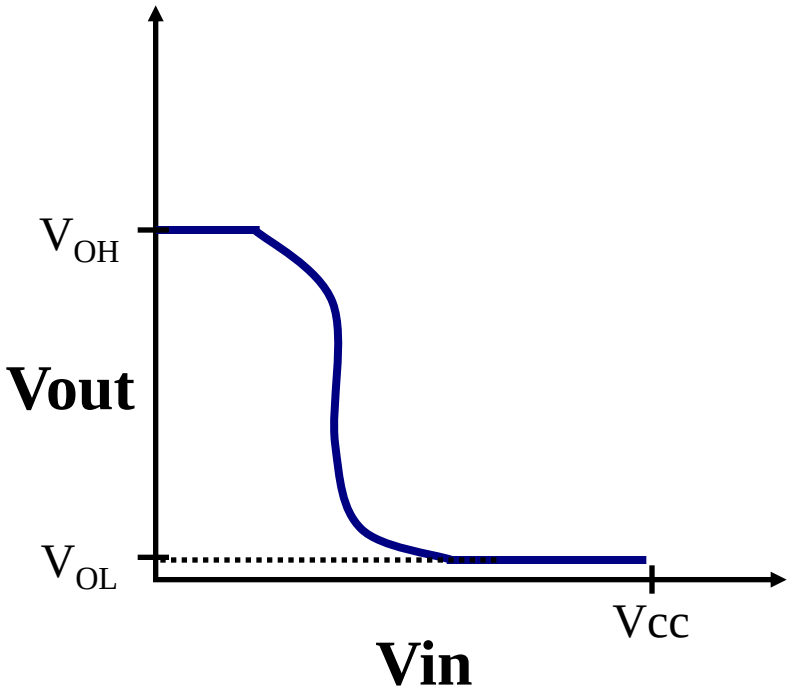




Ideal digital inverter:

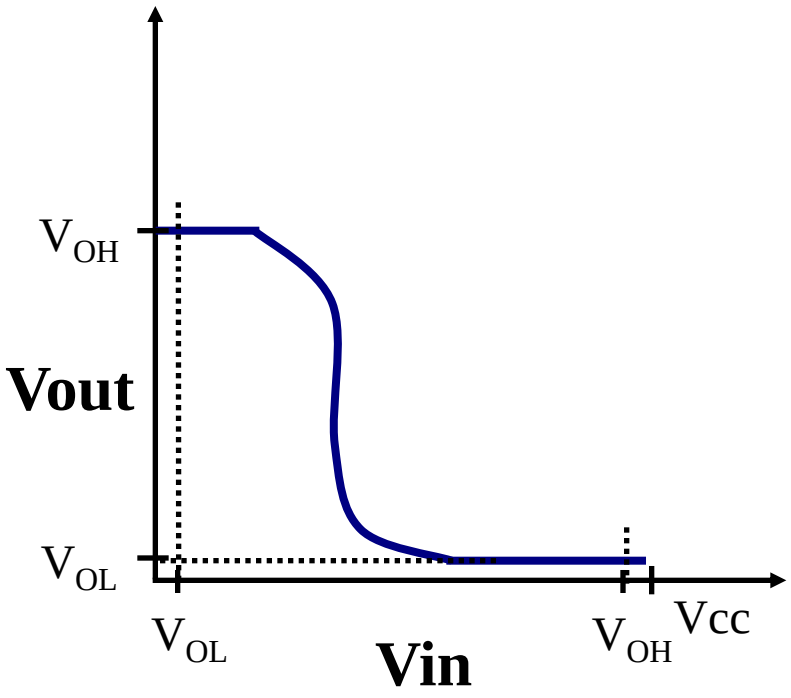
- When Vin=0, Vout=Vcc
- When Vin=Vcc, Vout=0
- Sharp transition region

Actual inverter: V_{OH} and V_{OL}



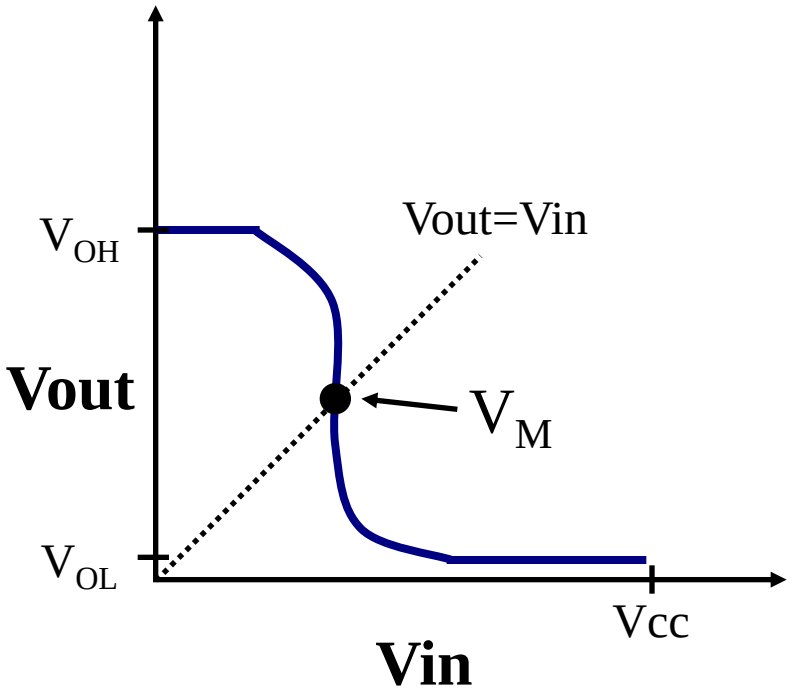
- V_{OH} and V_{OL} represent the "high" and "low" output voltages of the inverter
- V_{OH} = output voltage when Vin = '0'
- V_{OL} = output voltage when Vin = '1'
- Ideally,
  - V_{OH} = Vcc
  - V_{OL} = 0

V_{OL} and V_{OH}



- In transfer function terms:
  - $V_{OL} = f(V_{OH})$
  - $V_{OH} = f(V_{OL})$
  - f = inverter transfer function
- Difference (V_{OH}-V_{OL}) is the *voltage swing* of the gate
  - *Full-swing logic* swings from ground to Vcc

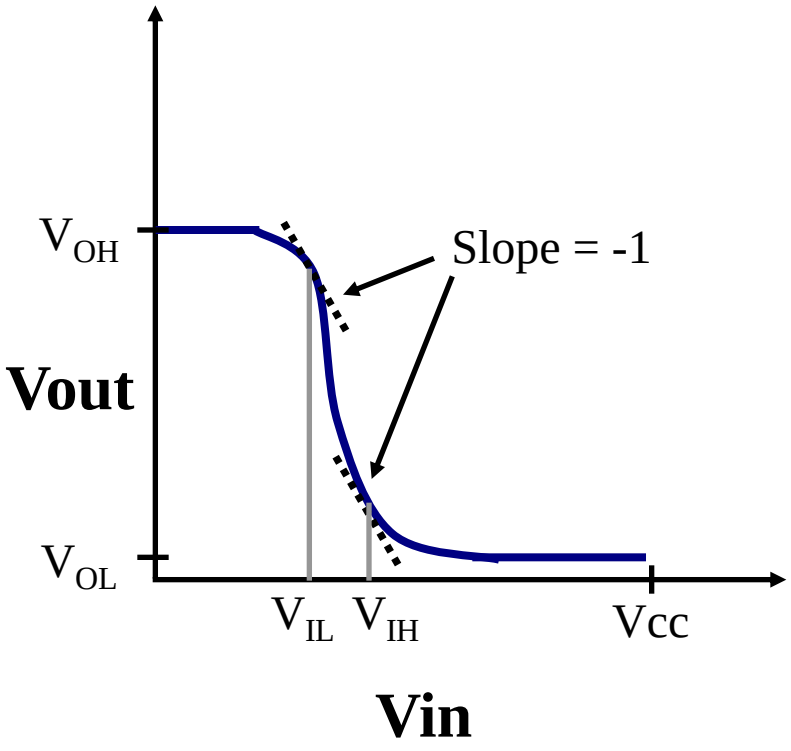
Inverter Threshold



Inverter switching threshold:

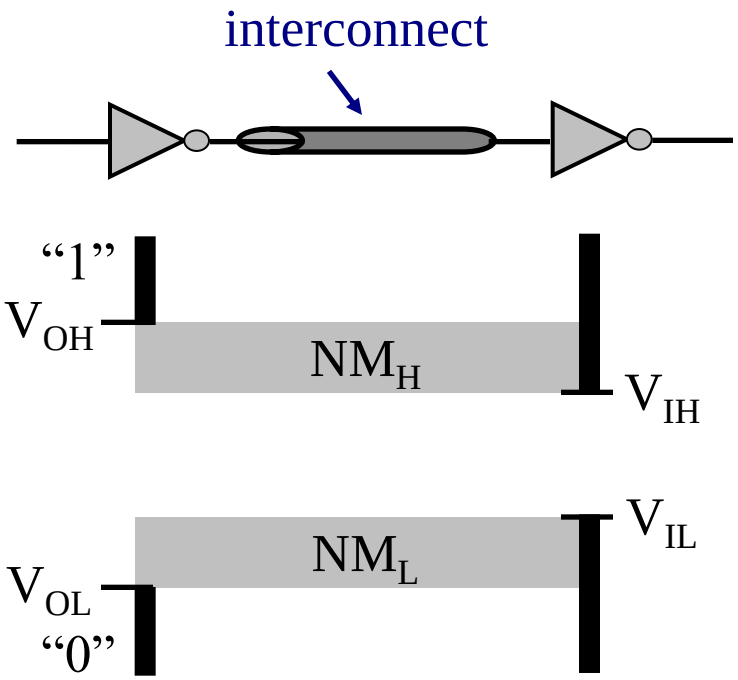
- Point where voltage transfer curve intersects line Vout=Vin
- Represents the point at which the inverter switches state
- Normally, $V_M \approx Vcc/2$
  - Why?

Noise Margins….



- V_{IL} and V_{IH} measure effect of input voltage on inverter output
- V_{IL} = largest input voltage recognized as logic ‘0’
- V_{IH} = smallest input voltage recognized as logic ‘1’
- Defined as point on VTC where slope = -1

Inverter Noise Margin



Ideally, noise margin should be as large as possible

- Noise margin is a measure of the *robustness* of an inverter
  - $N_{ML} = V_{IL} - V_{OL}$
  - $N_{MH} = V_{OH} - V_{IH}$
- Models a chain of inverters. Example:
  - First inverter output is V_{OH}
  - Second inverter recognizes input $> V_{IH}$ as logic '1'
  - Difference V_{OH}-V_{IH} is "safety zone" for noise

Noise Margin (cont)

- Why are V_{IL}, V_{IH} defined as unity-gain point on VTC curve?
  - Assume there is noise on input voltage V_{in}

$$V_{out} = f(V_{in} + V_{noise})$$

  - First-order approximation (Taylor Series):

$$V_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} V_{noise}$$

Note: **$dV_{out}/dV_{in} = 0$ occurs only at the beginning and at the end of the VTC curve, elsewhere it is negative**

  - If gain (dV_{out}/dV_{in}) > 1, noise will be amplified.
  - If gain < 1, noise is filtered. Therefore V_{IL}, V_{IH} ensure that gain < 1

CMOS Inverter Noise Margins

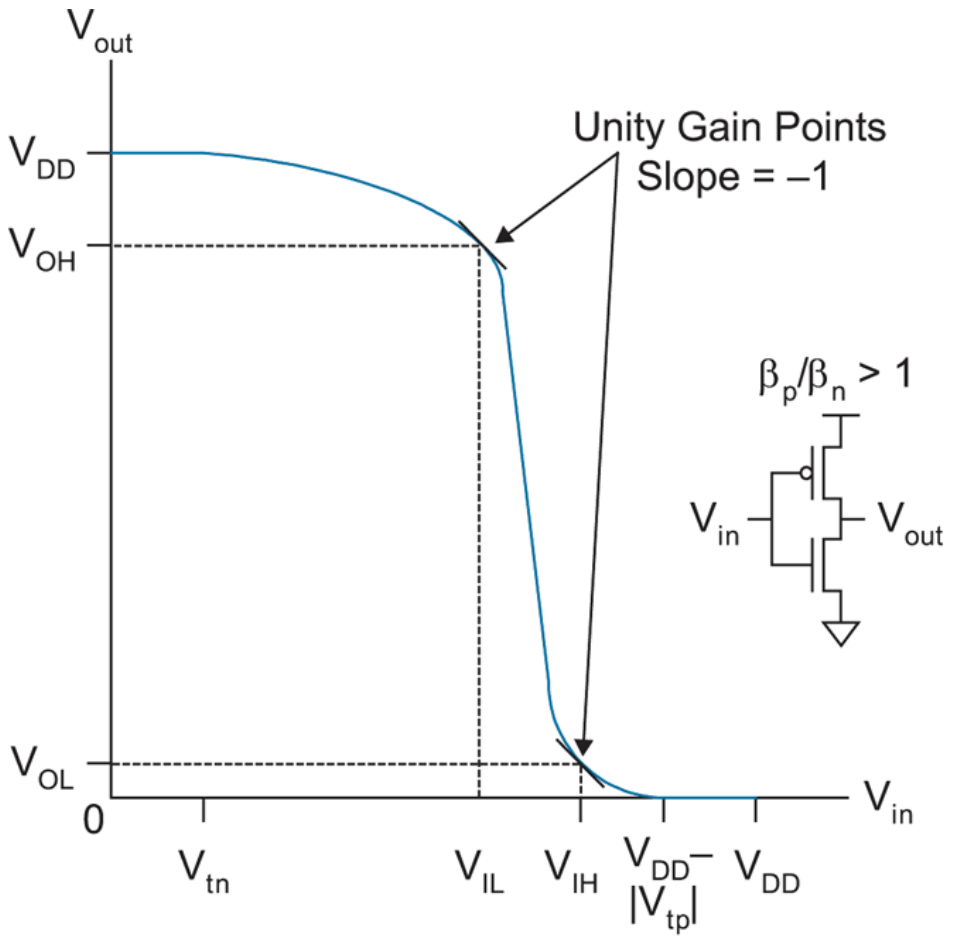
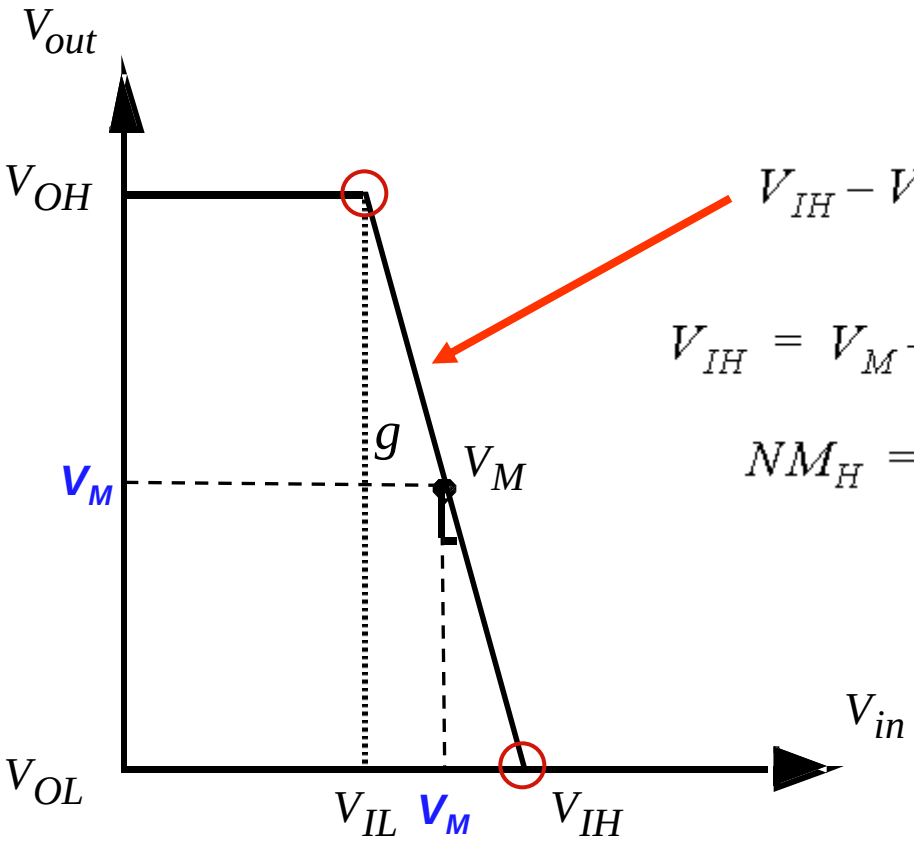


FIG 2.28 CMOS inverter noise margins

Determining V_{IH} and V_{IL}

A simplified approach: piecewise linear approximation of the VTC



i.e., $V_{OH}=V_{DD}$ and $V_{OL}=0$

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

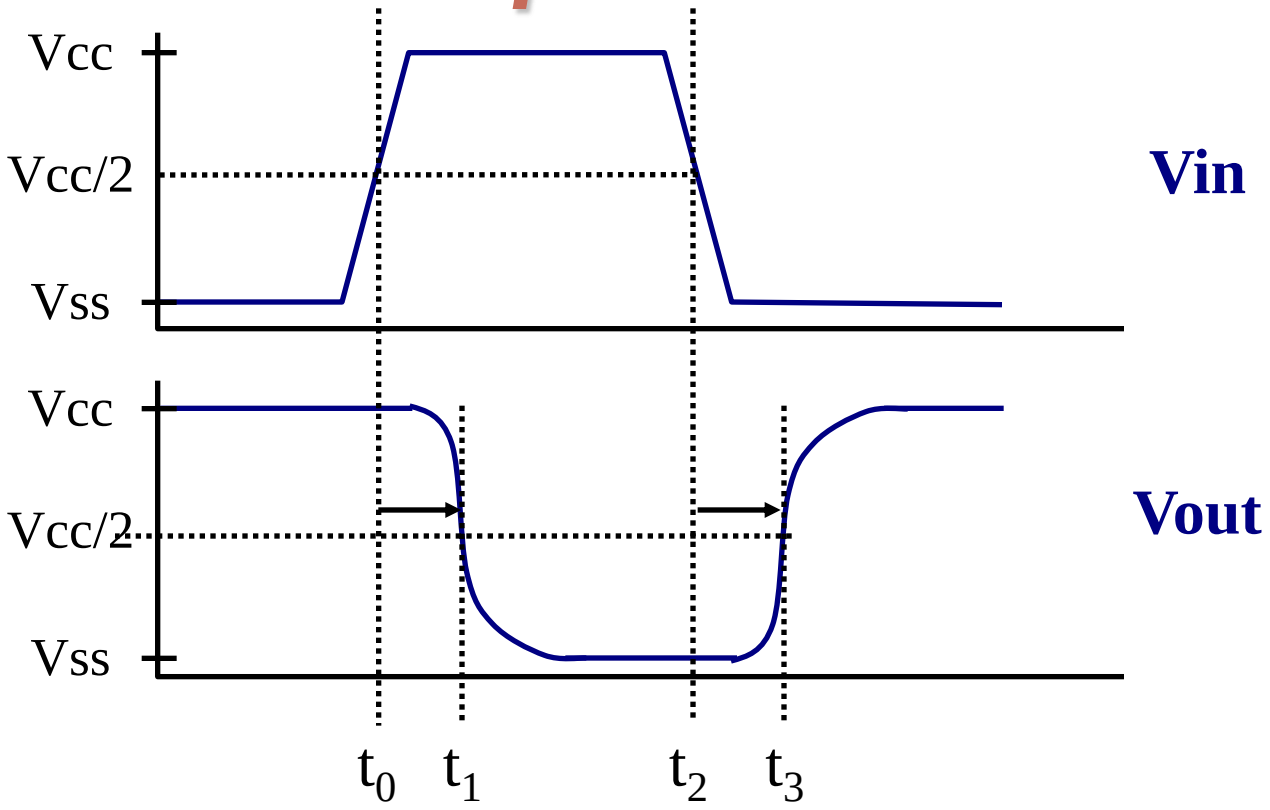
$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

Note: As $g \rightarrow \infty$, $V_{IH}=V_{IL}=V_M$

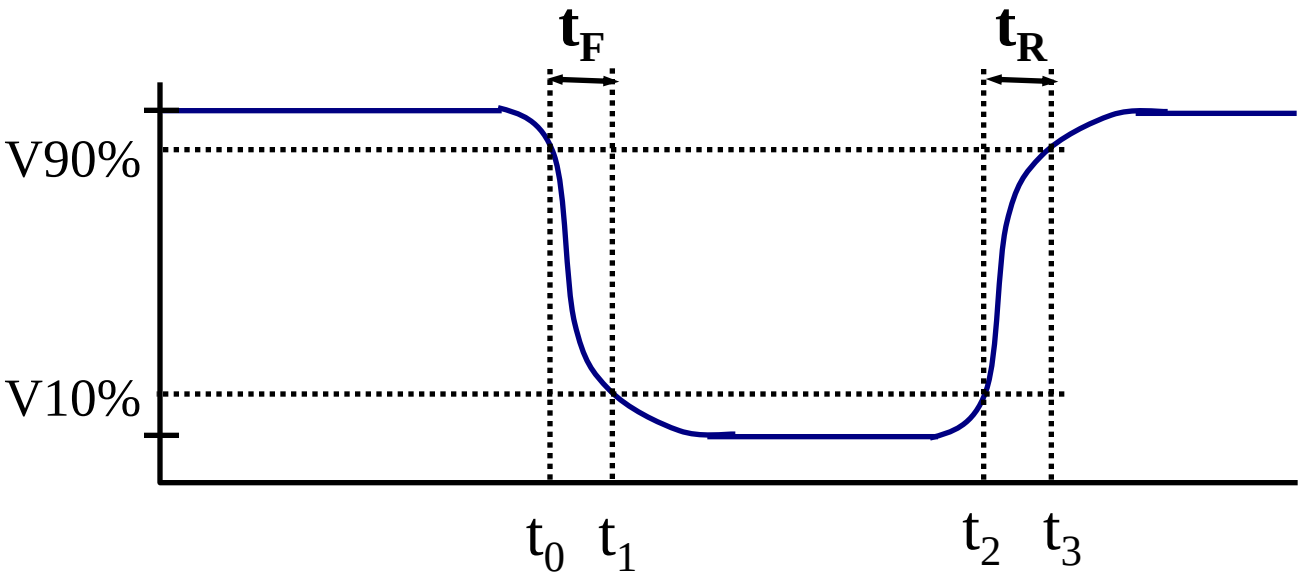
i.e., ideal inverter

Inverter Time Response



- Propagation delay measured from 50% point of Vin to 50% point of Vout
- $t_{phl} = t_1 - t_0$, $t_{plh} = t_3 - t_2$, $t_p = \frac{1}{2}(t_{phl}+t_{plh})$

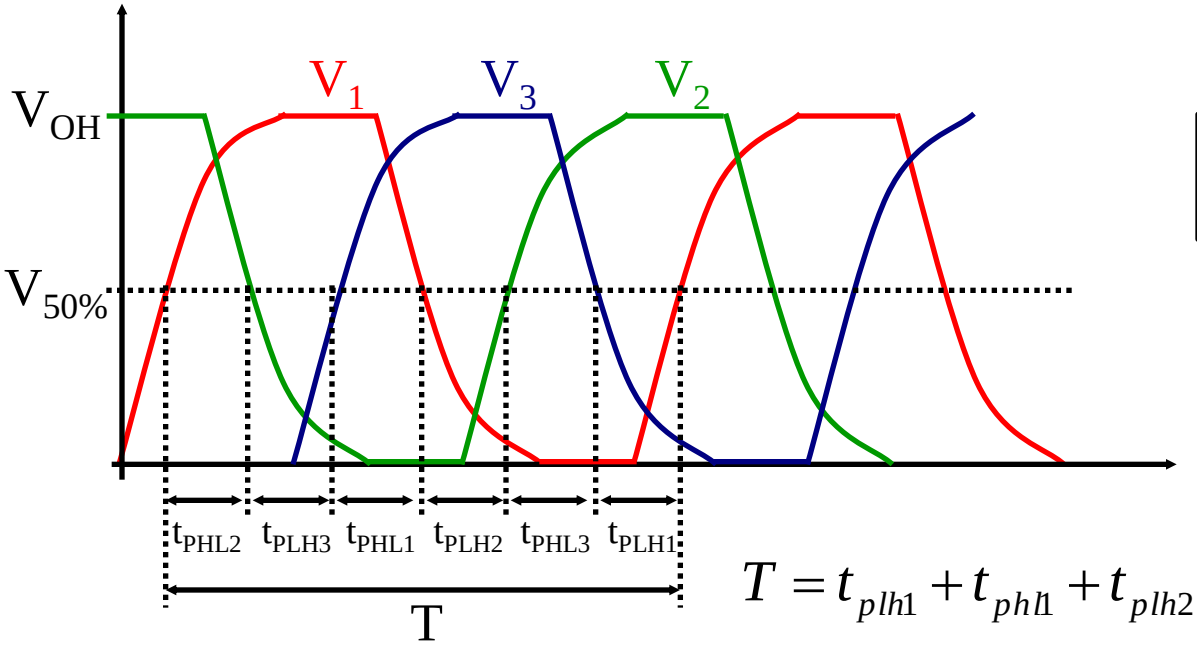
Rise and Fall Time

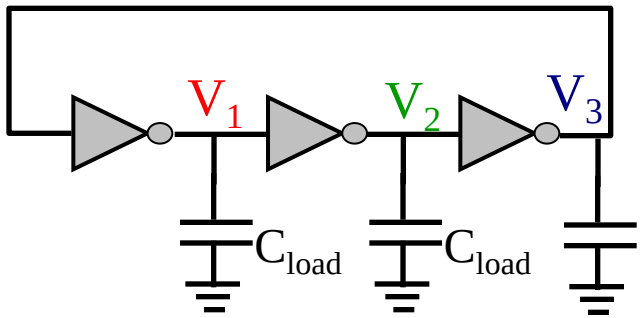


- Fall time: measured from 90% point to 10% point
  - $t_F = t_1 - t_0$
- Rise time: measured from 10% point to 90% point
  - $t_R = t_3 - t_2$
- Alternately, can define 20%-80% rise/fall time

Ring Oscillator

- *Ring oscillator circuit*: standard method of comparing delay from one process to another
- Odd-number n of inverters connected in chain: oscillates with period T (usually n >> 5)



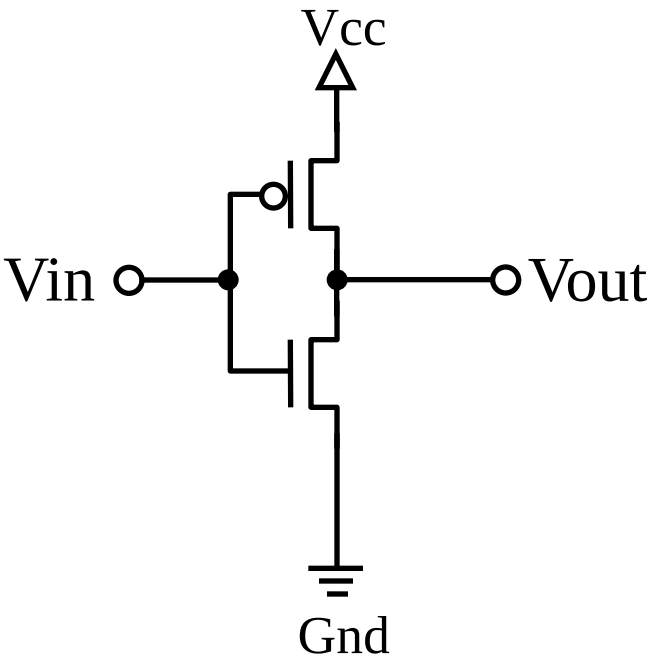


$$T = t_{plh1} + t_{phl1} + t_{plh2} + t_{phl2} + t_{plh3} + t_{phl3} + \cdots$$

For n stages: $T = 2nt_p$, $f = \frac{1}{T} = \frac{1}{2nt_p}$, $t_p = \frac{1}{2nf}$

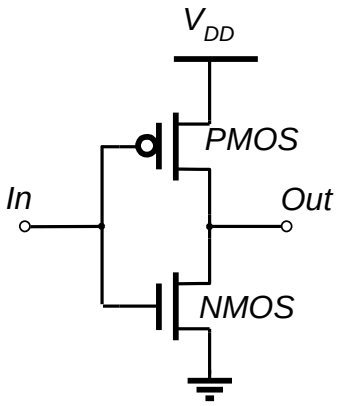
CMOS Inverter

- Complementary NMOS and PMOS devices
- In steady-state, only one device is on (no static power consumption)
- Vin=1: NMOS on, PMOS off
  - Vout = V_{OL} = 0
- Vin=0: PMOS on, NMOS off
  - Vout = V_{OH} = Vcc
- Ideal V_{OL} and V_{OH}!
- High input resistance (insulated gate) and low output impedance (finite resistance path between output and Vcc or Gnd)
- **Ratioless logic**



Generating the Inverter VTC

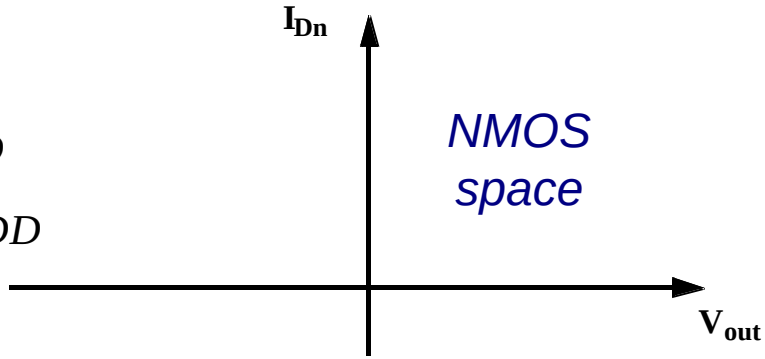
A. *Translate PMOS I-V Relations into NMOS Variable Space using the following:*

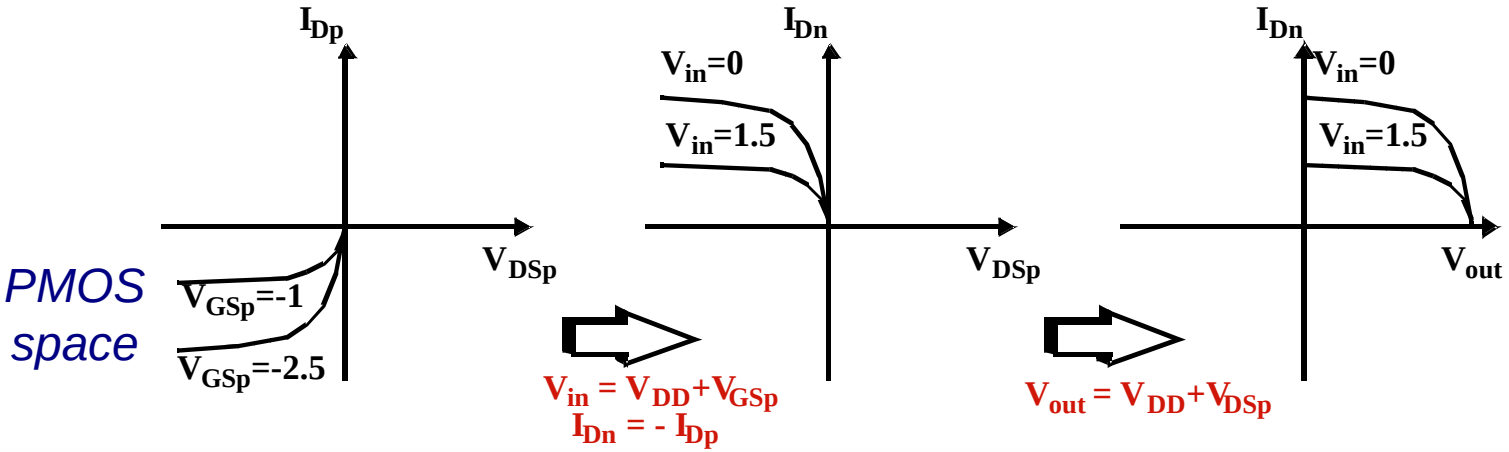


$$I_{Dsp} = -I_{Dsn}$$

$$V_{Gsn} = V_{in}; \quad V_{Gsp} = V_{in} - V_{DD}$$

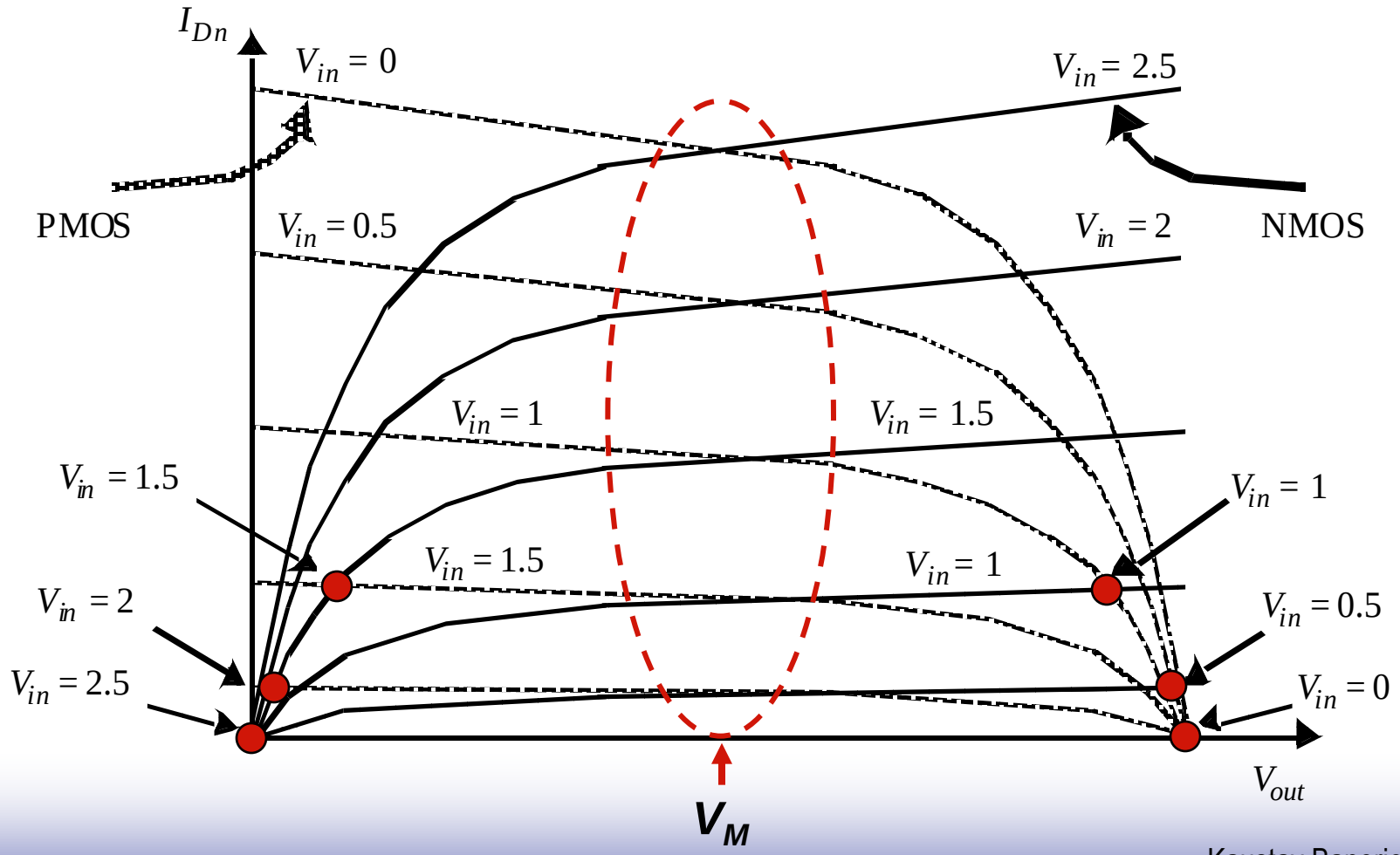
$$V_{Dsn} = V_{out}; \quad V_{Dsp} = V_{out} - V_{DD}$$



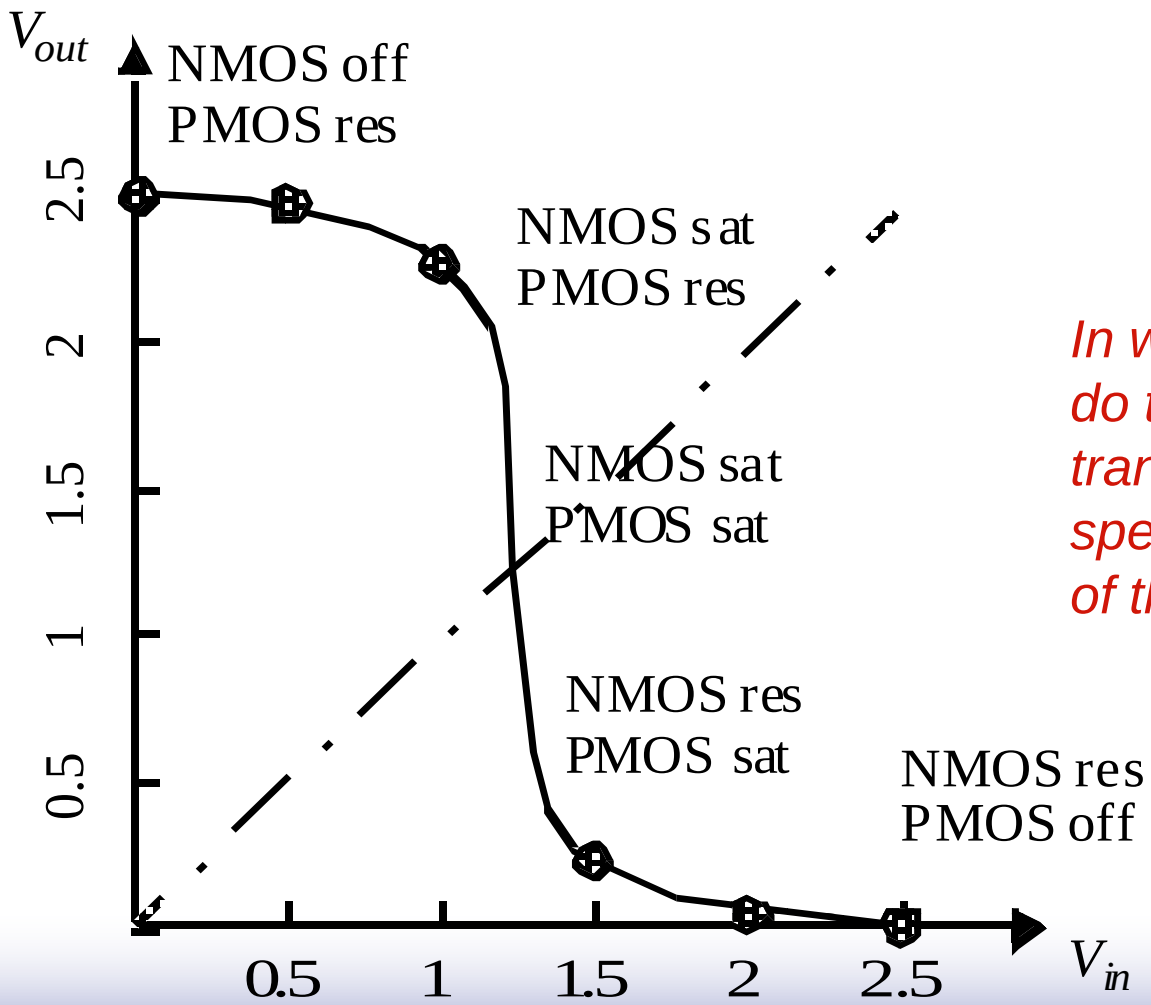


CMOS Inverter Load Characteristics

B. For a DC operating point to be valid, currents through NMOS and PMOS must be equal (for a given V_{in}), hence find the points of intersection.



CMOS Inverter VTC



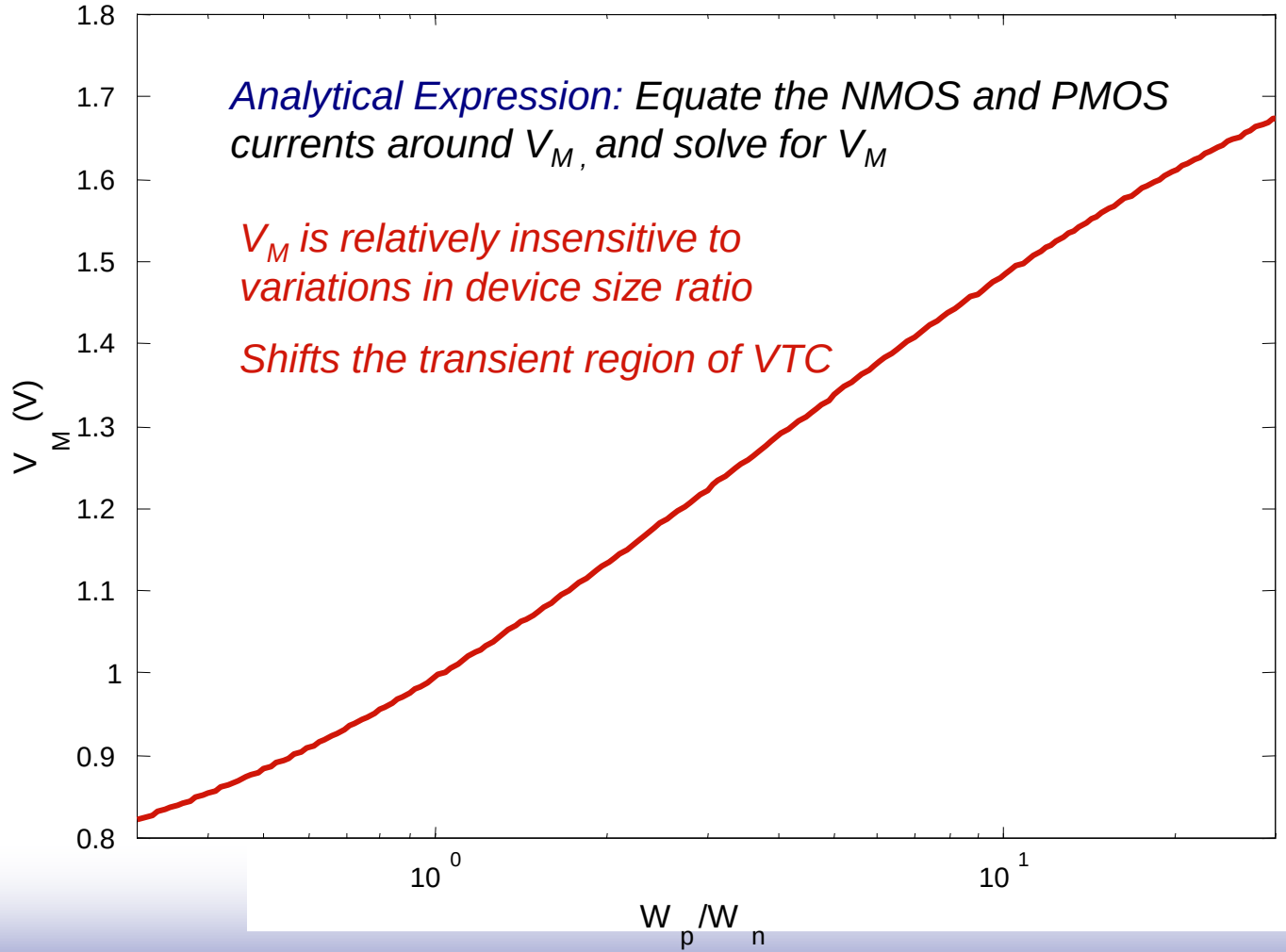
In which state do the transistors spend most of their time?

CMOS Inverter Operation (summary)

Table 2.2 Relationships between voltages for the three regions of operation of a CMOS inverter

	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

Switching Threshold as a function of Transistor Ratio

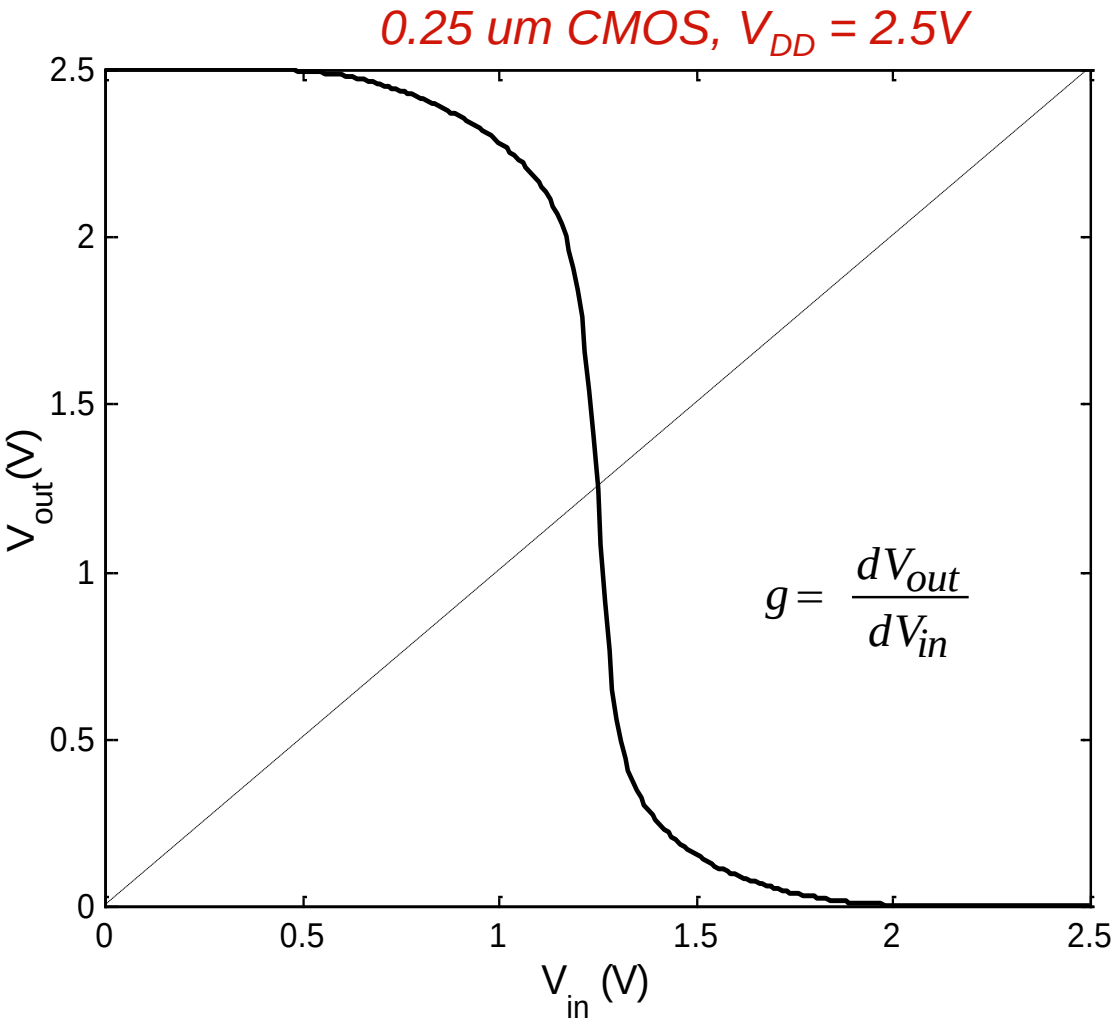


Analytical Expression: Equate the NMOS and PMOS currents around V_M, and solve for V_M

V_M is relatively insensitive to variations in device size ratio

Shifts the transient region of VTC

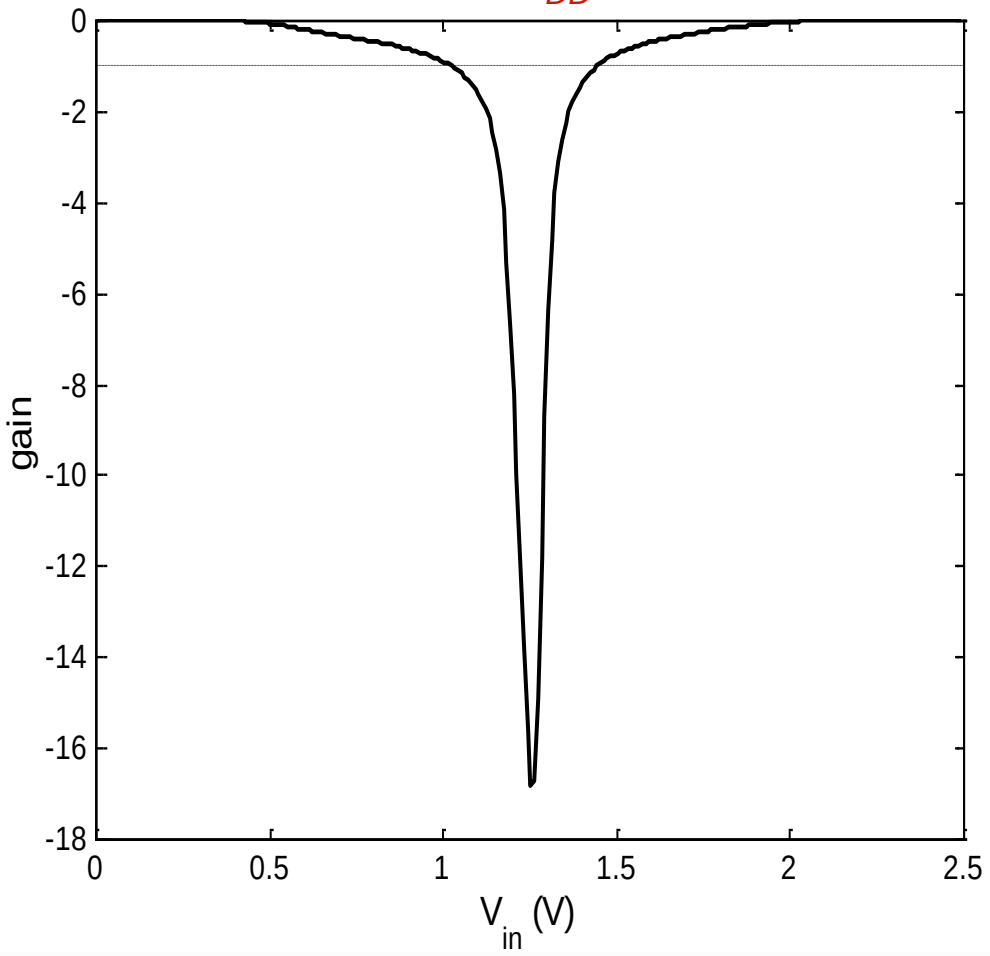
Simulated VTC



Note: piecewise linear approximation of the VTC would lead to higher gain

Inverter Gain

0.25 um CMOS, V_{DD} = 2.5V



Gain is mostly determined by technology parameters, especially channel length modulation, but also by V_{DD}

Note: approximately $V_M \propto V_{DD}$

Inverter Skew

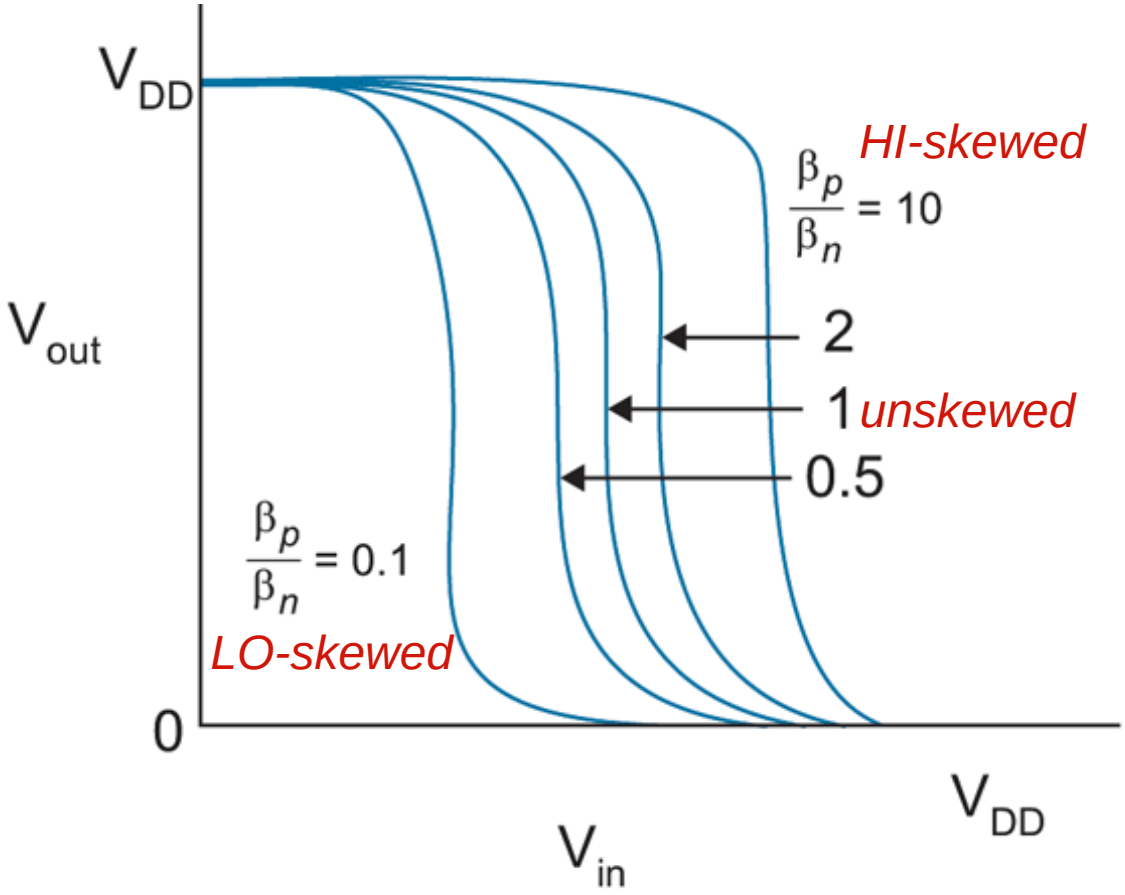


FIG 2.26 Transfer characteristics of skewed inverters