UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

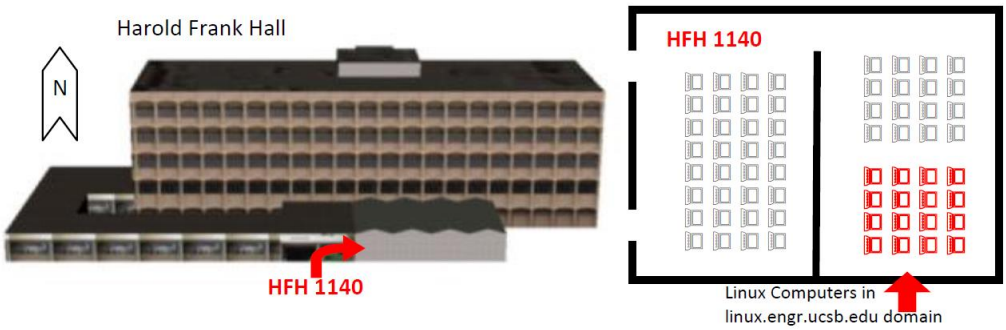
ECE 122A VLSI Principles

LAB 1 – Environment Setup and Tool Practice

Due Date: ***Monday, 10/06/2021, 5:00 pm***

The objective of Lab 1 is to give you an initial exposure to the software environment (HSpice, Cscope, MAX and SUE) that will be used in this course throughout the quarter. HSpice (netlist simulator), Cscope (waveform-analyzer for Linux), MAX (layout editor), and SUE (schematic capture tool) will be used to execute some of the procedures that are necessary in many lab and your project, during the course.

The lab is at HFH 1140. Please use one of the Linux computers shown in the figure below.



I. Simulation Environment Setup

1. Apply for an **Engineering Account**

   Make sure your account at engr.ucsb.edu is working. You can apply for a COE computer account directly on the ECI website (http://www.engr.ucsb.edu/eci/) by clicking the "New Account". If encountering any difficulties, you can also send an email to help@engineering.ucsb.edu or fill a form in ECI main office in 3110 Engineering 1 (Monday-Thursday 9AM-12 noon & 1PM-4PM). You need to change your password within 7 days of your account being activated.

2. Get **Necessary Files** for Lab 1

   Download the following necessary files from the course website.

   180nm_bulk.txt

   Bash_configure

   Inv.sp

3. Set Linux **Environment Variables**

This step helps you link your command (hspice, scope, max, sue, etc.) in the terminal to the tools on the ECE server. In other words, environmental variables must be set before you can start using the software. If you are using BASH shell, find ***.bashrc*** file in your home folder (~/.bashrc), and add the lines in provided file *bash_configure* to it. Type "source ~/.bashrc" to set the environmental variables for your account.

II. Tool Practice

1. HSpice

HSpice is a general-purpose analog electronic circuit simulator. It can be used to simulate electrical circuit in steady-state, transient, and frequency domains.

The provided file *180nm_bulk.txt* is a MOSFET model library, which can be downloaded from http://ptm.asu.edu. Look into *180nm_bulk.txt*, and **answer the following questions**:

a. Which **two devices** are defined in the library file (*180nm_bulk.txt*)?
b. Explain the following parameters in the file.
Lint, Rdsw, JS, Tox, Cj, Cjsw, Vsat, Vth0
(Hint: Try google "BSIM3 MOSFET Model JS")

The provided file *inv.sp* is a spice netlist that you are going to simulate in Lab 1. There are three main sections in the netlist file:

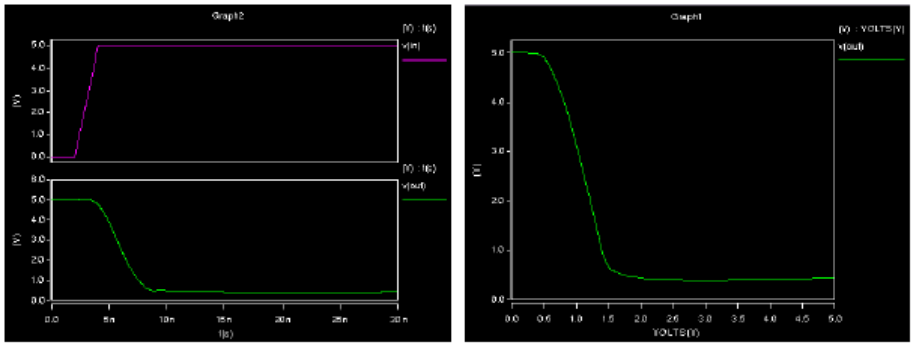
The models used. A model in hspice is a description of the parameters of devices.	.include '180nm_bulk.txt'
The netlist description. Netlist is a designation for a computer readable representation of the circuit schematic.	vdd vdd 0 2.5 vin in 0 pulse 0 2.5 1ns 1ns 1ns 3ns 8ns M1 out gate 0 0 NMOS L=.18u W=.36u M2 out gate vdd vdd PMOS L=.18u W=.72u
The analysis to be performed during the simulation. We are requesting a transient analysis and the DC Transfer Characteristic of the circuit.	.options post=2 nomod .op .tran .1ns 8ns .DC vin 0 2.5 0.1

In the terminal, type "hspice inv.sp". Upon proper completion of the simulation, you should see "info: ***** hspice job concluded".

Now you will have several new files in the folder:
inv.sp is the input netlist.
inv.sw0 is the DC sweep data output.
inv.tr0 is the transient data output.
inv.lis is the output listing from HSPICE.
inv.st0 is the simulation run information.
inv.ic is the information about input to HSPICE.

2. CosmoScope

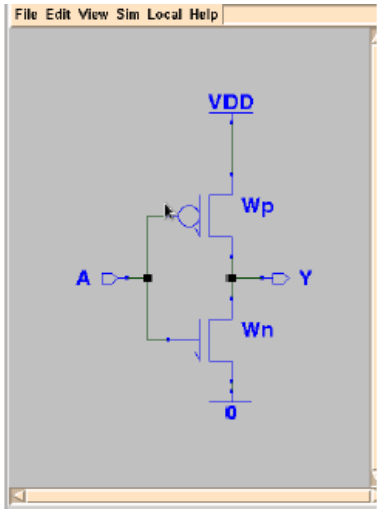
CosmoScope is a graphical waveform analyzer tool that allows you to view and analyze simulation results. An example of the waveforms in CosmoScope is as follows.



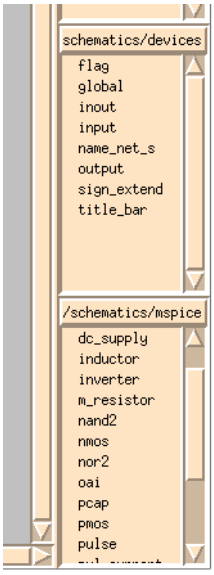
Type in "cscope" or "scope" to launch CosmoScope. Load your simulation results (inv.tr0 and inv.sw0), and you will see the corresponding waveform. **Attach a screenshot of your waveforms in your lab report.**

3. SUE

Draw a standard inverter cell (as shown below) with NMOS (gate width of 1) and PMOS (gate width of 2). An example is as below.

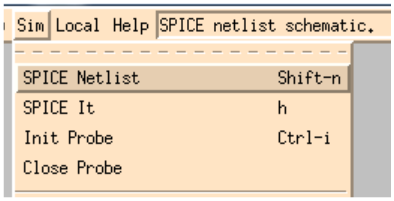


Voltage source, ground signal, pins and FETs can be found in the side toolbox:



Attach a screenshot of your schematic in you lab report.

Now generate a SPICE netlist using the following method, and you will find a new.sp file in the folder.



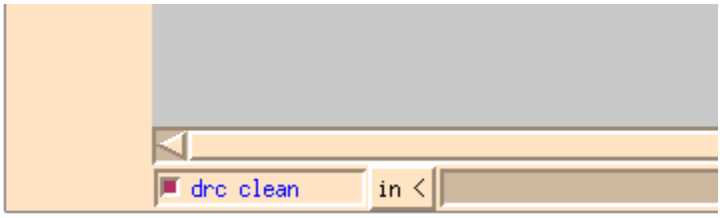
Attach the .sp file in your lab report.

4. MAX

Draw a standard inverter cell (as shown in Fig. 1.40 in the textbook) with a unit of NMOS and double-sized for PMOS by MAX. Your print out should show that no DRC error exists on graph by including the "DRC clean" string at the left bottom corner of MAX screen. Grid and labels for Vdd, Gnd, In and Out are needed. Refer to MAX manual on course webpage for help.

Please make sure:

- Your print out should show that no DRC (Design Rule Check) error exists on graph by showing the "**DRC clean**".



- You should have an N-Well under your PMOSFET.

- Your layout should have texts "Vdd", "Gnd", "A" and "Y" at input/output nodes. To do so, select the metal electrode, and then press "t" to add a text.

Attach a screenshot of your layout in your lab report. (An example is as below)