UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

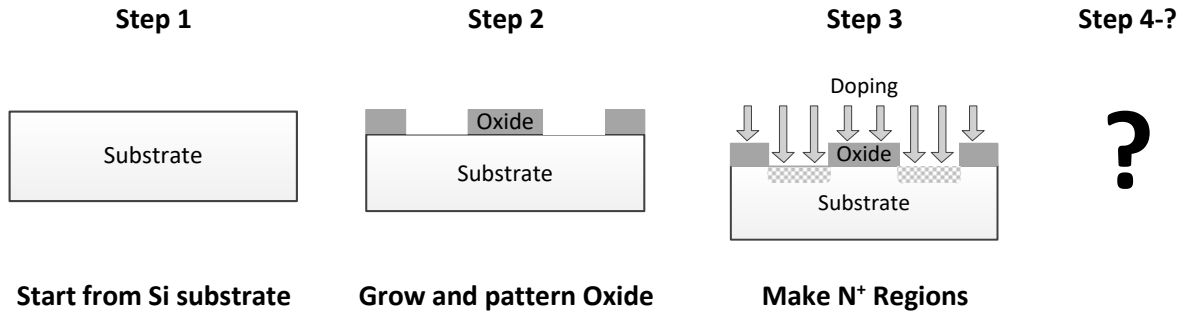
ECE 122A VLSI Principles

Homework #2 CMOS and Pass Transistors

Due Date: **10/17/2023, Tuesday 5:00 PM**

Problem 1 CMOS Fabrication

(A) View the videos on CMOS fabrication (on the course website) and read the slides from Intel: "From Sand to Silicon" or "From Sand to Circuit" (on the course website), briefly describe the process of how an NMOS transistor is made on a clean wafer. You may include your sketches, for example as following: (10')

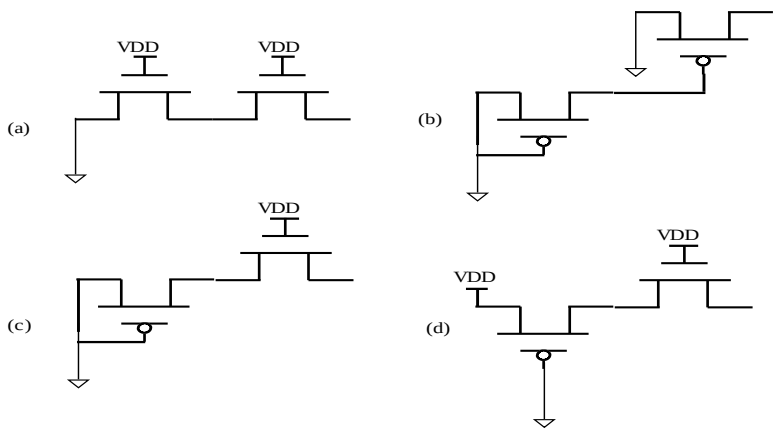


Think about what materials should be used and what the right procedures are.

(B) Draw the layout for a pMOS transistor (hint: refer to Lab-1) in an n-well process that has active, p-select (for p-type implanted ion doping), n-select (for n-type implanted ion doping), polysilicon (gate), contact, and metal1 (the lowest metal layer, connecting contacts) masks. Include the well contact to V_{DD}. (10')

Problem 2 Pass Transistors (20')

(A) Assume the threshold voltages for NMOS and PMOS are V_{thn} and $(-V_{thp})$. Give the expressions of the output voltage for each circuit. (5')



(B) Design an XNOR gate with transmission gates. (5')

(C) Design an 8-to-1 multiplexor using transmission gates and inverters. (10')

Problem 3 Multiplexer and Combination Logic (20')

Implement the following 4-input function with a single 8-1 multiplexer:

$F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$

Problem 4 CMOS Circuit (20')

(A) Simplify the following expression. (10')

F(a,b,c,d,e) = Σm(0, 2, 3, 7, 8, 9, 10, 12, 15, 18, 19, 31) +Σd(4, 13, 23)

(B) Implement your answer in (A) to a one-stage static CMOS circuit. (10')

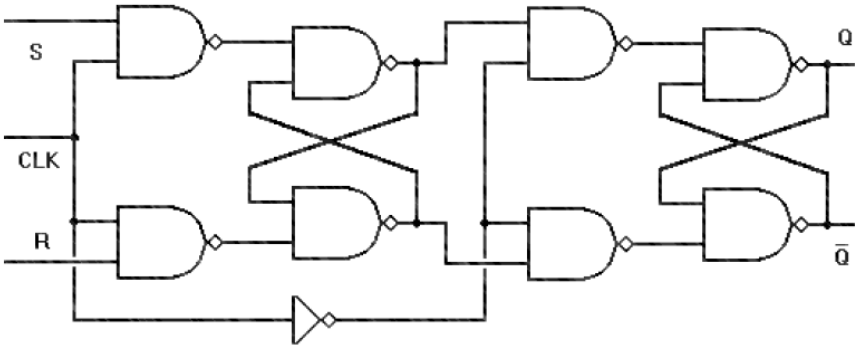
Problem 5 Flip Flop and Latches (20')

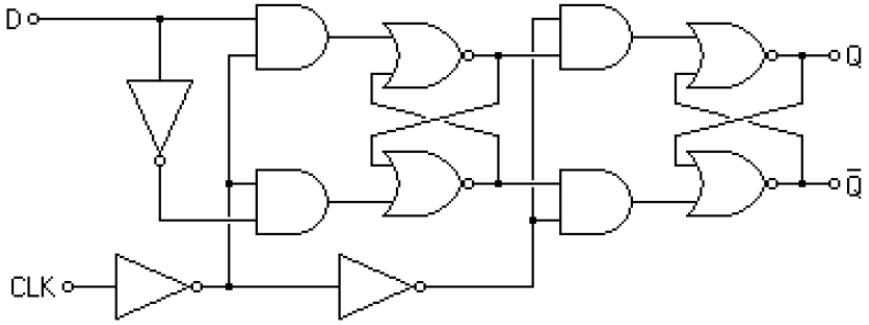
(A) Draw the waveform vs. time for a high-level-triggered D-latch and a positive-edge-triggered D Flip-Flop, given the clock and D signal. (5')

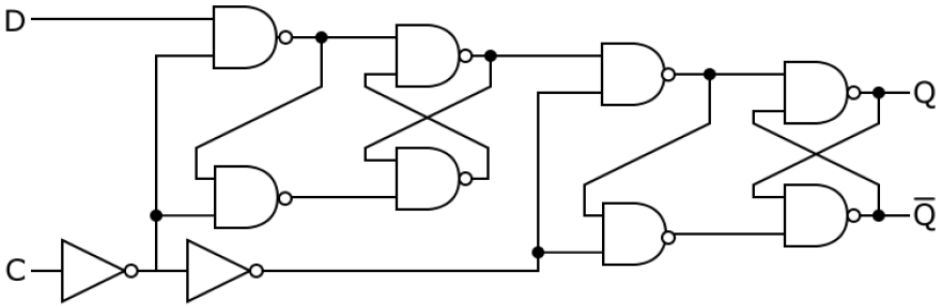
(B) The following figures show **four** flip flops. Answer for each figure: (10')

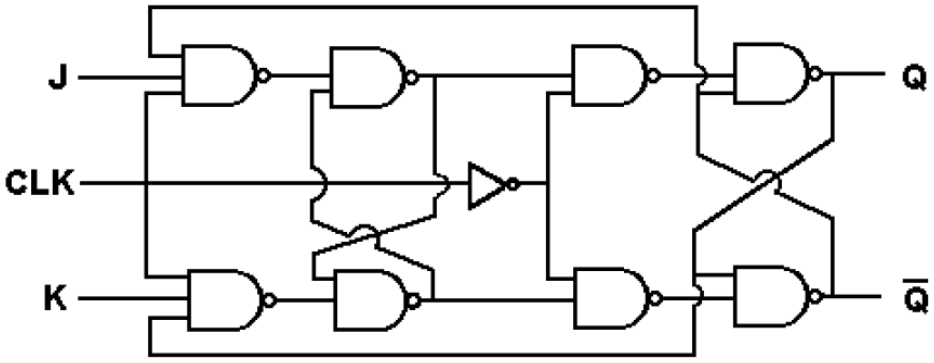
(i) Is it positive-edge-triggered or negative-edge-triggered by clock signal (CLK or C marked in figures)?

(ii) List the excitation table for each one.









(C) As shown in (B), flip flops can be implemented by two latches of the same design. But there are also flip flops that cannot be implemented by two same latches. Give an example (draw the schematic and briefly explain how it works). (5')

Problem 6 Comparator Design (20')

Come up with a design for a 4-bit comparator which compares two 4-bit numbers A and B and makes the output go high when A is greater than B. Ideally, your comparator should start by comparing the MSBs of the two numbers, and cascade down to the LSBs. Marks will be given based on the size and the logic behind the design. Draw the circuit schematic with basic gates.

Problem 7 MUX Implementation (20)

An 8x1 MUX has inputs A, B and C connected to the selection inputs S2, S1 and S0 respectively. The data inputs through I0 and I7 are as follows:

(a) I1 = I2 = I5 = 0; I3 = I4 = 1; I0 = I6 = D; and I7 = D'
(b) I2 = I3 = 0; I4 = I5 = I7 = 1; I0 = I6 = D; and I1 = D'

Implement the same Boolean expression using pass transistors.