UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering
ECE 122A VLSI Principles

Homework #4 MOSFET and CMOS Inverter

Due Date: **11/06/2023, Monday, 5:00 PM**

For all the questions, the dielectric constant of SiO_2 is $\varepsilon/\varepsilon_0 = 3.9$, where $\varepsilon_0 = 8.85\times10^{-12}$ F·m^{-1} is the vacuum dielectric constant. The dielectric constant of Si is $\varepsilon_s/\varepsilon_0 = 11.7$.
$e = 1.6\times10^{-19}$ C and $k_BT/e = 26$mV.

Problem 1 Threshold Voltage (4 + 4 + 4 + 2 + 2 + 4 = 20)

An N-MOSFET and a P-MOSFET are fabricated with substrate doping concentration of 6×10^{17} cm^{-3} (P-type substrate for N-MOSFET and N-type substrate for P-MOSFET). The gate oxide thickness is 5 nm.

(a) Find V_t of the N-MOSFET when N+ poly-Si is used to fabricate the gate electrode.

(b) Find V_t of the P-MOSFET when N+ poly-Si is used to fabricate the gate electrode.

(c) Find V_t of the P-MOSFET when P+ poly-Si is used to fabricate the gate electrode.

(d) Assume that the only two voltages available on the chip are the supply voltage $V_{dd} = 2.5$ V and ground, 0 V. What voltages should be applied to each of the terminals (body, source, drain, and gate) to maximize the source-to-drain current of the N-MOSFET?

(e) Repeat part (d) for P-MOSFET.

(f) Which of the two transistors (b) or (c) is going to have a higher saturation current. Assuming that the supply voltage is 2.5V, find the ratio of the saturation current of transistor (c) to that of transistor (b).

Problem 2 Body Bias (10+10 = 20)

An NMOS device has the following parameters:

N+ poly gate (work function difference between gate and channel is $\Phi_{GC} = -1.06$V);
P-doped channel with doping concentration $N_a = 1.5\times10^{15}$ cm^{-3}; $n_i = 1.5\times10^{10}$cm^{-3}.

SiO_2 thickness is $t_{ox} = 30$nm;
Positive charges in oxide: $Q_{ox} = 3.48\times10^{-9}$ C/cm^2.

(A) Determine V_T.
Hint 1: calculate substrate Fermi potential φ_F first.
Hint 2: Inversion layer can be formed even in zero gate voltage due to the positive charges in oxide and the work function difference.

(B) Is it possible to apply a V_{SB} voltage such that $V_T = 0$? If so, what is the value of V_{SB}?
Be careful about the sign of φ_F.

Problem 3 Capacitance and Band Diagram (10+10 = 20)

A n^+ polysilicon gate n channel MOS transistor is made on a p-type Si substrate with Na = 5 x 10^{15} cm^{-3}. The SiO_2 thickness is 10 nm in the gate region.

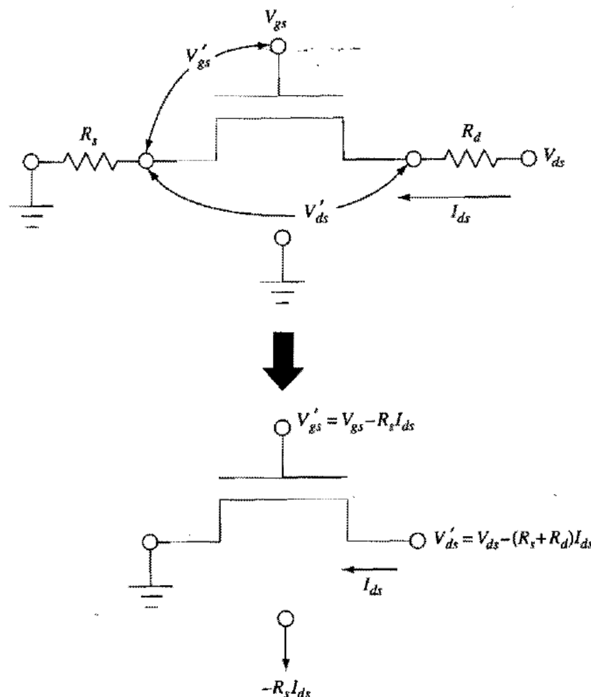
A. Calculate V_{FB} and V_T. Also, calculate the depletion capacitance, and the minimum gate-substrate capacitance.
B. If I have an effective interface charge Q_i is 4 x 10^{10} qC/cm^2, find how do the V_{FB}, V_T, depletion capacitance and minimum gate-substrate capacitance change.

Problem 4 Device Parasitics (20)

The source-drain resistance needs to be considered when the contacts for drain and source are not good enough. The figure shows a simple model of MOS parasitic resistance. A source resistance R_s and a drain resistance R_d are assumed to connect to an intrinsic MOSFET. The external terminals are driven by voltage source V_{ds} and V_{gs}. The internal voltages are V_{ds}' and V_{gs}' for the intrinsic MOSFET. One can write the following relations:

$$V'_{ds} = V_{ds} - (R_s + R_d)I_{ds}$$

$$V'_{gs} = V_{gs} - R_s I_{ds}$$



Assume the transconductance g_m' corresponds to internal voltages V_{ds}' and V_{gs}', the transconductance gm corresponds to external V_{ds} and V_{gs}. Prove that g_m and g_m' have the following relation:

$$g_m' = \frac{g_m}{1 - g_m R_s - g_{ds}(R_s + R_d)} \ ,$$

where $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$ is the extrinsic transconductance, and $g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$ is the extrinsic output conductance.

Problem 5 CMOS Inverter (5+5+4+4+4+4+4=30)

In a typical 2:1 CMOS inverter, if the PMOS can be made to operate at a lower temperature (e.g. 20 ºC) than the NMOS (e.g. 120 ºC), what will be the impact on:

(A) The voltage transfer curve (indicate with a sketch of the VTC).

(B) Inverter switching threshold.

(C) Gain.

(D) Delay.

(E) Power (both switching and leakage).

(F) What can be done to the NMOS to make the inverter symmetric (without changing the temperature).

(G) Show that the capacitance power consumption (P_{cap}) of a CMOS inverter is independent of the load capacitance (C_L) when operating at its maximum speed.