*UNIVERSITY OF CALIFORNIA, SANTA BARBARA*

*Department of Electrical and Computer Engineering*

*ECE 122A VLSI Principles*

# *Homework #5* MOSFET, CMOS Sizing, Logical Effort, Ratioed and Pass Transistor Logic

# Due Date: **Friday, 11/24/2023, 5:00 PM**

**Problem 1 CMOS Sizing (20)**

(A) Implement the following function in a single stage CMOS logic (avoid the use of inverter at output). Appropriately size the transistors to mimic the rise and fall times of a 3:2 inverter (PMOS width: NMOS width = 3:2). (20 pts)

$F(a,b,c,d) = \sum(0,2,4,9,15) + d(7,13)$

**Problem 2 CMOS Sizing II (20 + 20 = 40)**

Simulate a 3 input NAND gate in SPICE with three inputs – A, B and C (180 nm technology), and a $V_{DD}$ of 2.5 V. Assume an output capacitance load of $C_L = 100fF$. Consider two cases:

(A) Do not size the transistors [ $(W/L)_p = 2(W/L)_n$ ]. Calculate the input-output delays for the following cases: $A = B = C = 1 \rightarrow 0$, $C = B = 1$ and $A = 1 \rightarrow 0$, $A = C = 1$ and $B = 1 \rightarrow 0$, and $A = B = 1$ and $C = 1 \rightarrow 0$

(B) Now size the transistors properly to ensure the rise and fall times mimic a standard 2:1 inverter. Repeat the calculation above.

For each of the two cases please elaborate on the reason for the difference in the delays.

**Problem 3 Inverter Delay (20)**

As shown in the schematic below, a unit-size inverter (0.72 um/0.36 um) is driving a Pseudo-NMOS inverting stage. The external load capacitance, $C_L=50fF$. Assume the unit-size inverter has an equivalent capacitance of $C_{unit}$, and equivalent output resistance of $R_{unit}$. Also assume the equivalent output resistance of Pseudo-NMOS stage $R_{eq}=R_{unit}/S$
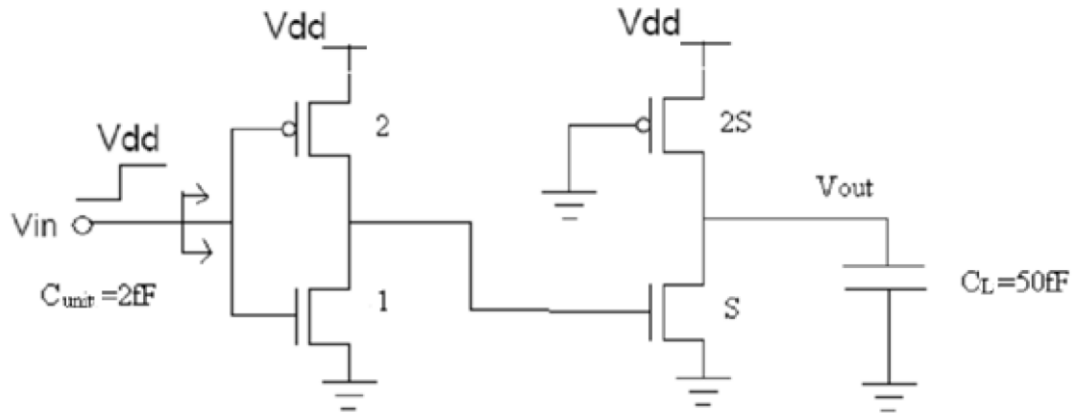
(a) Keep the *Wp/Wn* ratio of the Pseudo-NMOS stage 2:1, find the delay for a low-to-high transition at the output, $t_{pLH}$, in terms of $C_{unit}$ and $R_{unit}$.

(b) Use $C_{unit} = 2$ fF, find the optimal S that minimize the low-to-high delay by taking derivative of your result in part (a).

(c) Use $t_{p0} = 0.69 * R_{unit} * C_{unit} = 20$ps, calculate the minimum delay for low-to-high transition at the output, $t_{pLH}$, for a given $R_{unit} = 2$kΩ.

(d)  Suppose that the probability for input being 0V, $\alpha 0 = 50\%$; the probability for input being 2.5V, $\alpha 1 = 50\%$. Ignore short circuit current, what is the average power dissipated by this circuit? Use $VDD = 2.5$V, $f_{clk} = 3$GHz. Use $C_{unit} = 2$fF, $R_{unit} = 2$kΩ.
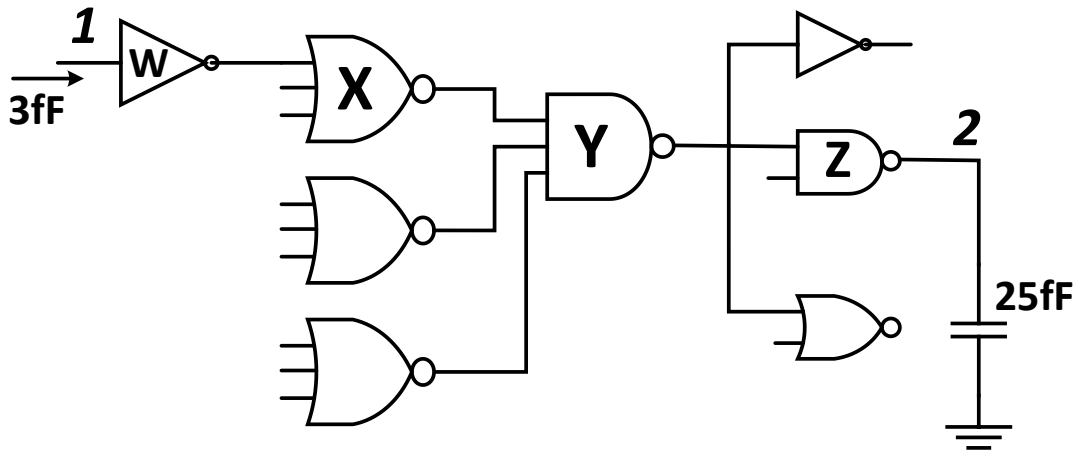
## Problem 4 Logical Effort I

Calculate the logic effort of the transmission gate shown in figure below, given that $W_p = 2W_n = 2W_{min}$. (20')
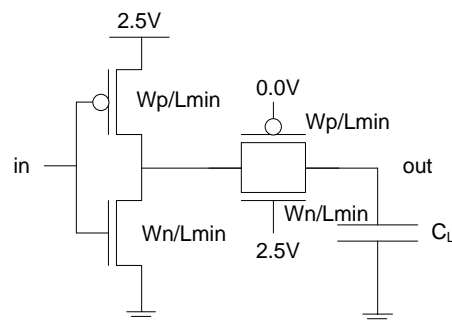
**Problem 5 Logical Effort II – Part I (20)**

(A) (**10 PTS**) The figure below shows a logic path from node 1 to node 2. Find the input capacitances necessary for each of the gates {W, X, Y, Z} in the path to minimize path delay.

For part A, B and C, a unit size inverter is assumed to have the ratio Wp:Wn = 3:1.



**Problem 6 Logical Effort II – Part II (10+10)**

This is a continuation of the previous problem:

(**A**) As discussed in the course, the carrier mobility decreases when temperature increases. Assume temperature only affects carrier mobility. Intuitively, higher temperature makes it more difficult for a circuit stage to drive the next stage, because the driving current decreases. Hence, we may define a temperature effort (*T* for path temperature effort, and *t* for single stage temperature effort) to describe the effects of temperature-induced current decrease in a combinational logic block.

The following figure shows the relation between fan-out (f) and delay of a logic gate. The logical effort and intrinsic delay of this gate are g0 and p0. What is the fan-out to delay curve of a gate of logical effort g1 and intrinsic delay p1 (g1 > g0, p1 > p0)? If temperature increases, how will the fan-out to delay relation change? Show your answers in the same figure. (You need to draw the three curves in the same figure)

From the above analysis, derive the temperature effort t of a logical gate, with respect to the change of mobility.
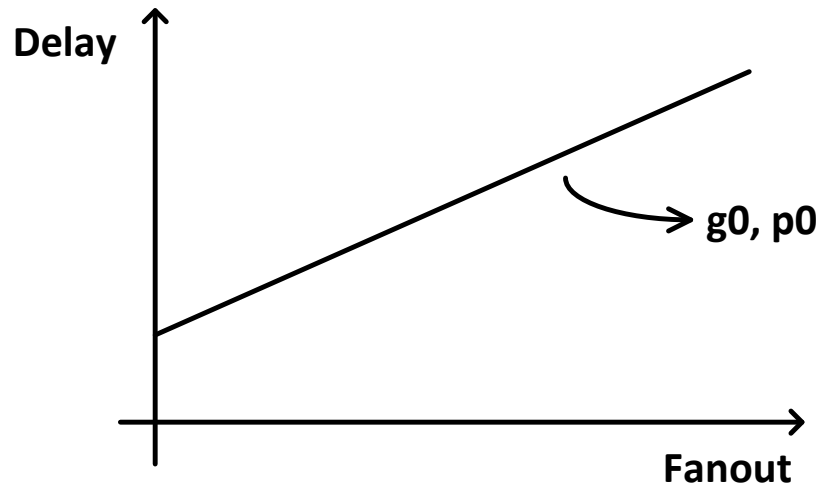
(B) Again, a unit size inverter has the ratio Wp:Wn = 3:1, and operates at temperature T0, when the mobility of electrons and holes is $\mu_{n0}$ and $\mu_{p0}$. Assume temperature T1 causes the mobility to decrease by 10% ($\mu_n/\mu_{n0} = \mu_p/\mu_{p0} = 0.9$), and temperature T2 causes the mobility to decrease by 20% ($\mu_n/\mu_{n0} = \mu_p/\mu_{p0} = 0.8$). Assume temperature only affects the mobility of a device.

Now each stage is set to be at temperature either T1 or T2, as shown in the figure below. Find the input capacitances necessary for each of the gates {W, X, Y, Z} in the path in order to minimize path delay. Assume the path delay is minimized when each stage bears the same effort.