

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

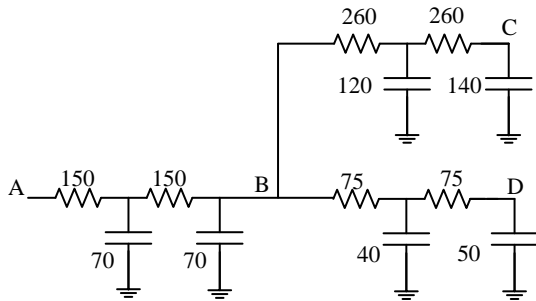
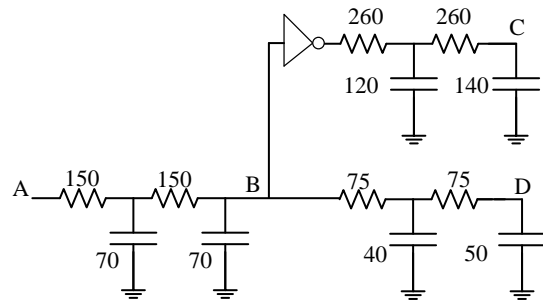
Department of Electrical and Computer Engineering

ECE 122A VLSI Principles

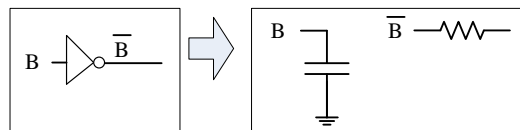
Homework #6 Interconnects, Dynamic and Sequential Logic**Due Date: Tuesday, 12/05/2023, 5:00 PM****Problem 1 Interconnect I (20)**

(A) For Figure 1, calculate the Elmore delay from node A to nodes B, C, and D (units of resistance and capacitance are Ω and fF). (5')

(B) In order to reduce the delay from node A to C, an inverter with size h is added after node B as shown in Figure 2. Assuming $R_{inv} = 2k \Omega/h$ and $C_{inv} = 2fF \cdot h$, find the h to minimize the delay? (5')

**Figure 1****Figure 2**

Hint 1: the inverter can be modeled as:



Hint 2: The delay from A to C can be estimated by the summation of the Elmore delays from A to B.

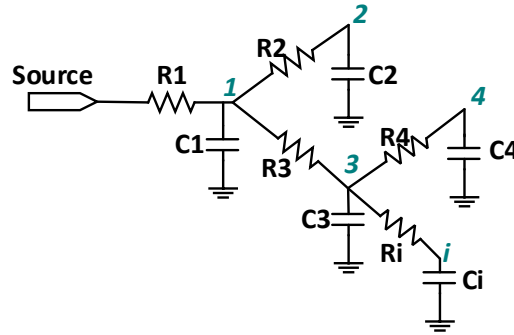
(C) What is the delay from A to C in this case in Figure 2? (5')

(D) What is the delay from node A to D? (5')

Problem 2 Interconnect II (20)

(A) Compute the Elmore delay for node i in the following lumped RC network. (10')

(B) Assume a positive step signal appear at source at $t = 0$. How long does it take for node i to reach 10% and 90% point? (10')



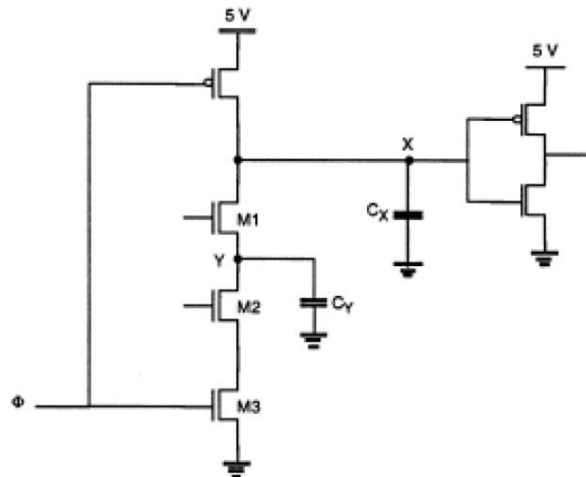
Problem 3 Interconnect III (20)

Consider a uniform interconnect of length L , resistance per unit length r and capacitance per unit length c that is buffered by N identical repeaters (inverters). Assume that for a minimum sized repeater, the input capacitance is c_0 , the output parasitic capacitance is C_s , and output resistance is r_s . The interconnect drives a load C_L (input capacitance of each repeater). If the length of the interconnect segment between adjacent repeaters is l ($= L/N$) and the repeater size is s , then:

- (A) Explain why is it necessary that the repeaters are of identical size. Reconcile this with the fact that we have spent long hours understanding why and how gates have to be sized to minimize delay. (4')
- (B) Find the delay (τ) of each repeater-interconnect-repeater block. Define the delay (τ) as the time difference between the input of the first repeater and the input of the second repeater. (4')
- (C) Find an optimum value for s (s_{opt}) that makes total interconnect delay minimum. (4')
- (D) Find an optimum value for l (l_{opt}) that makes the total interconnect delay minimum. (4')
- (E) Find the minimum value of the total interconnect delay τ_{opt} . (4')

Problem 4 Dynamic Logic

Consider the CMOS logic circuit in the figure, which is a simple Domino circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the domino circuit.

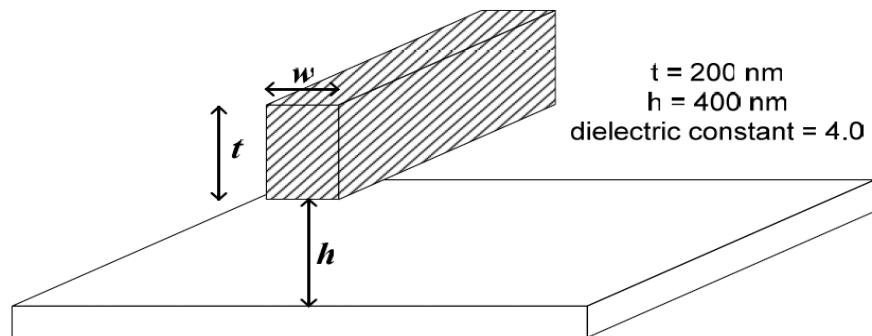


(a) Explain how the voltage level at node X, after it is pre-charged to 5 V, can be affected during “evaluate” by the charge sharing between node X and node Y. Express the final voltage at node X in terms of the initial voltage at node Y, when the charge sharing is completed following the full pre-charge operation. During pre-charge, the gate terminal of the transistor M2 is fixed at 0 V.

(b) Determine the ratio between device transconductance parameters, k_p and k_n , of the inverter to prevent any logic error due to charge sharing between nodes X and Y under all circumstances. Assume that the magnitudes of threshold voltages in the inverter are equal to 1.0 V.

Problem 5 Interconnect Parasitic Capacitances (20)

The figure below shows a 1 mm long interconnect lying over a ground plane at a height ‘h’ above it.

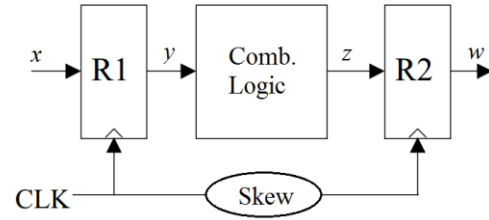


The wire cross-section (w , t) is shown. Assuming the surrounding material has a dielectric constant 4.0, and varying the wire width ‘w’ from 100 nm to 400 nm plot:

- (1) Parallel plate capacitance of the wire with respect to ground plane.
- (2) Fringing capacitance of the wire with respect to the ground plane.
- (3) Total capacitance (parallel plate + fringing).
- (4) For such a wire configuration, which interconnect dimension (w or t) should be smaller for low total capacitance?

Problem 6 Sequential Logic

In the circuit below, setup time, hold time, propagation delay and contamination delay of flip-flops (R1, R2) are 1 ns, 0.7 ns, 2 ns and 0.8 ns, respectively. The maximum delay of the combinational logic is 3.3 ns. Suppose there is a positive clock skew of 0.3 ns.



i) draw a time diagram for signals x , y , z and w .

ii) calculate the maximum clock frequency.

iii) calculate the minimum delay allowed for the combinational logic.