UNIVERSITY OF CALIFORNIA, SANTA BARBARA

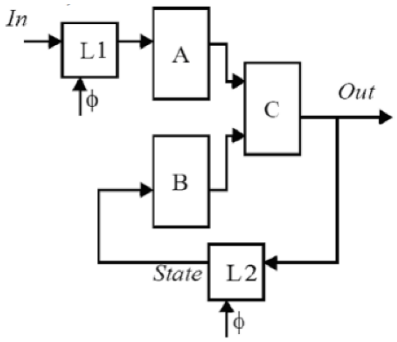
Department of Electrical and Computer Engineering

ECE 122A VLSI Principles

Homework #7 Sequential Logic, Adder, Memory

Due Date: **Monday, 12/11/2023, 5:00 PM**

Problem 1 Sequential Logic I



Consider the sequential circuit shown on the right. A, B and C represent combinational logic blocks with the following properties:

$t_{logic,minA}$ = 200 ps, $t_{logic,maxA}$ = 1 ns.

$t_{logic,minB}$ = 300 ps, $t_{logic,maxB}$ = 2 ns.

$t_{logic,minC}$ = 100 ps, $t_{hlogic,maxC}$ = 0.5 ns.

The L-units represent positive latches clocked by ϕ (i.e., the latches are transparent when ϕ is high). These latches have a setup time of 150 ps and a td-q delay of 250 ps (when the latch is transparent). The clock to output delay tclk-q is 120 ps, and thold is 110 ps. The clock has period Tclk and is high for a duration of T_{on}. In other words, the duty cycle of the clock is T_{on}/T_{clk}.

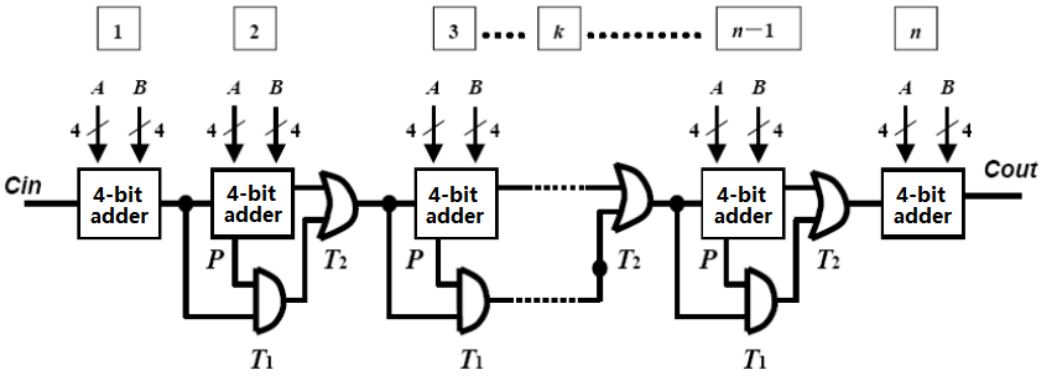
(A) Determine the conditions on the clock necessary to avoid the occurrence of hold time violations.

(B) Determine the absolute minimum clock period for this circuit to work correctly as well as the maximum duty cycle.

(C) Suppose that due to some sloppy clock-network routing, the clock signal at L1 arrives 100ps earlier than the clock signal at L2. Calculate the absolute minimum clock period for this circuit to work properly as well as the maximum duty cycle.

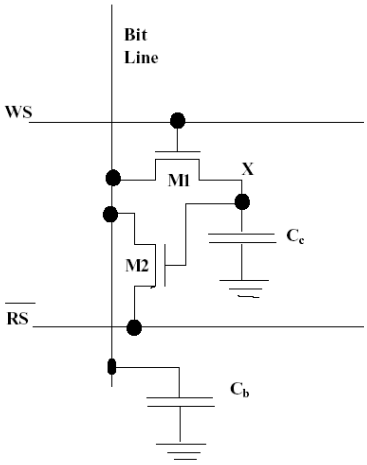
Problem 2 Datapath

A Carry-Bypass Adder consists of n 4-bit ripple-carry adders, as shown in the figure. P is carry propagation signal. Assume the delay of 1-bit adder is T_a = 2.5 ns (delay from {*A*, *B*, *Cin*} to {*S*, *Cout*}), and the time of generation of carry bypass propagation signal is T_p = 2 ns (delay from {*A*, *B*} to *P*). AND gate delay is T_1 = 1.3 ns while OR gate delay is T_2 = 1.7 ns. What is the time needed for the whole adder to finish the 4n-bit sum?



Problem 3 DRAM

The 2-T memory cell shown below uses 2 identical transistors with W/L = 0.4/0.25. Separate lines are provided for the read select (RS) and write select (WS) signals, which both switch between 0 and 2.5V. The Bit Line is precharged to $V_{dd}/2$ prior to a read. A write is done by pulling the bit line either to V_{dd} or to *GND*. Ignore the body effect and channel-length modulation. ($\gamma = 0$ and $\lambda = 0$). You may assume that $k_n' = 115$ uA/V^2, $V_{dd} = 2.5$ V, $V_t = 0.4$ V.



i) Explain the operation of the memory. Draw waveforms for V(BL), V(WS), and V(RS) and V(X) for reads and writes of both '1's and '0's.

ii) Determine maximum current through M2 during a read operation.

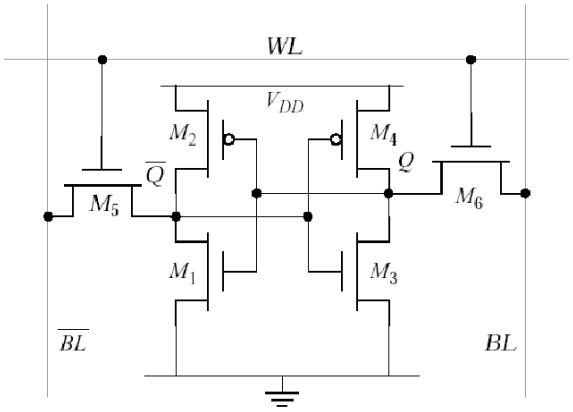
iii) The bit line is connected to a single-ended sense-amp, which switches when the voltage reaches V_{dd} / 2 – 200 mV. Compute the time required to read a data bit. Assume that $C_c = 10$ fF and $C_b = 2$ pF. (You may need MATLAB)

Hint: the drain current can be expressed as follows:

$$I_{DS} = \begin{cases} \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2, \text{ Saturation region} \\ k'\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right), \text{ Linear region} \end{cases}$$

Problem 4 SRAM

A generic SRAM cell is shown below. At first, it seems like the margins in such a memory cell should be good, since it contains two CMOS inverters, which we know have large margins. However, the problems are associated with those access devices connected to the cell. When cell is not accessed, it has great margins; when access devices are on, they act like load devices. Capacitance on bit lines is large enough to act like a voltage source.



(*kn'* = 115 uA/V^2 , *kp'* = 30 uA/V^2, *Vdsatn*=0.63V, *Vdsatp*=0.7V, *Vtn*=0.4 *Vtp*=-0.4)

i) Read Operation

Assume first that node Q is in the "1" state, we further assume that both bit line are precharged to VDD, 2.5V, before the read operation is initiated. Suppose that noise margin of inverter is 0.7V.

Please find out the dimension ratio of M5 and M1 to avoid "read upset" under the WORST case. (Note: During a correct read operation, the values stored in Q and *Q'* are transferred to the bit lines by leaving BL at its precharge value and by discharge *BL* through M1 – M5. A careful sizing of the transistors is necessary to avoid accidentally writing a "1" into the cell. This type of malfunction is called "read upset"). (You may need MATLAB)

ii) Write operation

Assume that a "1" is stored in the cell. A "0" is written in the cell by setting *BL* to "1" and BL to "0". The noise margin is given as in part a). What is the ratio of M4 and M6 to guarantee a successful write operation? (You may need MATLAB)