*UNIVERSITY OF CALIFORNIA, SANTA BARBARA*

*Department of Electrical and Computer Engineering*

*ECE 122A VLSI Principles*

# LAB 2 – CMOS Circuit Simulation with HSpice

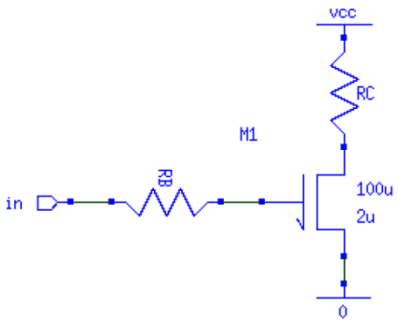
## Due Date: ***Thursday, 10/19/2023, 5:00 pm***

## Part 1: HSpice Syntax

In this part, you will learn to read and write basic netlist file for HSpice simulation.

Here is a typical HSpice netlist (the schematic is shown on right):

```
.title 'Resistor-load inverter'
.include '180nm_bulk.txt'
VCC vcc 0 5
VIN in 0 PULSE 0 5 2NS 2NS 2NS 30NS 60NS
RB in gate 10k
M1 out gate 0 0 NMOS L=2u W=100u
RC vcc out 1k
.options post=2 nomod
.op
.TRAN 1ns 30ns
.DC VIN 0 5 0.1
.END
```




The following is the explanation of each line:

| | |
|---|---|
| .title 'Resistor-load inverter' | The title<br>**Syntax: .TITLE 'string of up to 72 characters'** |
| .include '180nm_bulk.txt' | include a file (a library)<br>**Syntax: .INCLUDE 'filepath filename'** |
| VCC vcc 0 5 | Voltage source<br>**Syntax: Vxxx node+ node- voltage** |
| VIN in 0 PULSE 0 5 2NS 2NS 2NS 30NS 60NS | Pulse source function<br>**Syntax:**<br>**PULSE v1 v2 delay rise_ramp fall_ramp pulse_width period** |
| RB in gate 10k<br>RC vcc out 1k | Resistor<br>**Syntax: Rxxx node+ node- resistance** |
| M1 out gate 0 0 NMOS L=2u W=100u | MOSFET<br>**Syntax: Mxxx drain gate source base TYPE Length Width** |
| .options post=2 nomod | Output binary waveforms |
| .op | Calculate DC operating point of the circuit |
| .TRAN 1ns 30ns | Transient Analysis<br>**Syntax: .TRAN step_length duration** |
| .DC VIN 0 5 0.1 | Perform DC Sweep<br>**Syntax: .DC voltage_source start end** |

| | **step_length** |
|---|---|
| .END | The Star-Hspice input netlist file must have an .END statement as the last statement. |

For detailed syntax, see HSpice Manual posted on the course website. Note that the manual has 1800+ pages. Use find command to look for the syntax you need.

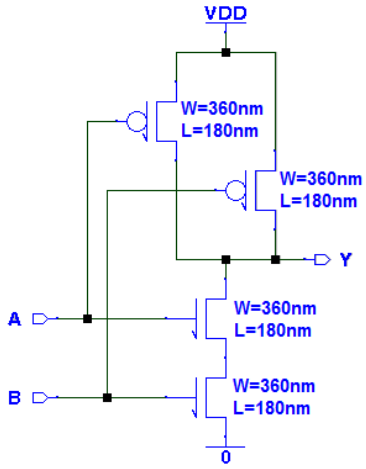
Now write a netlist for the following circuit on yourself. Given Vdd=2.5V, input A=1 and B changes from 0 to 1. Fill the blanks below:

```
.title 'NAND2'
.include '180nm_bulk.txt'

* Transistors:
M1 _____ _____ node1 0 NMOS L=180n W=____
M2 node1 B 0 0 NMOS L=____ W=____
M3 Y A VDD VDD ____ ______ ______
M4 _____ _____ _____ _____ ____ ______ ______

* Sources
VDD VDD 0 ____
VA A ___ ____
VB ___ ___ PULSE 0 ___ 5ns 0.1ns 0.1ns 10ns 20ns

.options post=2 nomod
.TRAN 0.1ns 20ns
.END
```




Save your netlist to file name ‘NAND2.sp’. **Attach your printed NETLIST in your report.**

## PART 2: Simulation with HSPICE

Add the following statement before '.END', which measures the delay from B to Y.

*.MEAS TRAN delay TRIG V(B) VAL='2.5/2' RISE=1 TARG V(Y) VAL='2.5/2' FALL=1*

```
Syntax:
.MEAS TYPE name TRIG V(node) VAL='value' RISE/FALL=number (determine which rise/fall edge)
+ TARG V(node) VAL='value' RISE/FALL=number
```

Save the change to 'NAND2.sp'.

Put the library file '180_bulk.txt' (from Lab 1) in the same folder with 'NAND2.sp'. Run HSpice to simulate your netlist. Launch CScope , load the file 'NAND2.tr0', and plot the waveforms of V(B) and V(Y).

**Attach your waveforms in the report.**

In the output info in the file 'NAND2.lis', you can find these lines, which tells you the delay from B to Y.


Make a note of the delay.

Now keep input B=1 and A changes from 0 to 1. You can do this by modify the netlist file. Make a note of the delay again this time. Similarly, you could measure the delays for the following cases, and fill in the table:

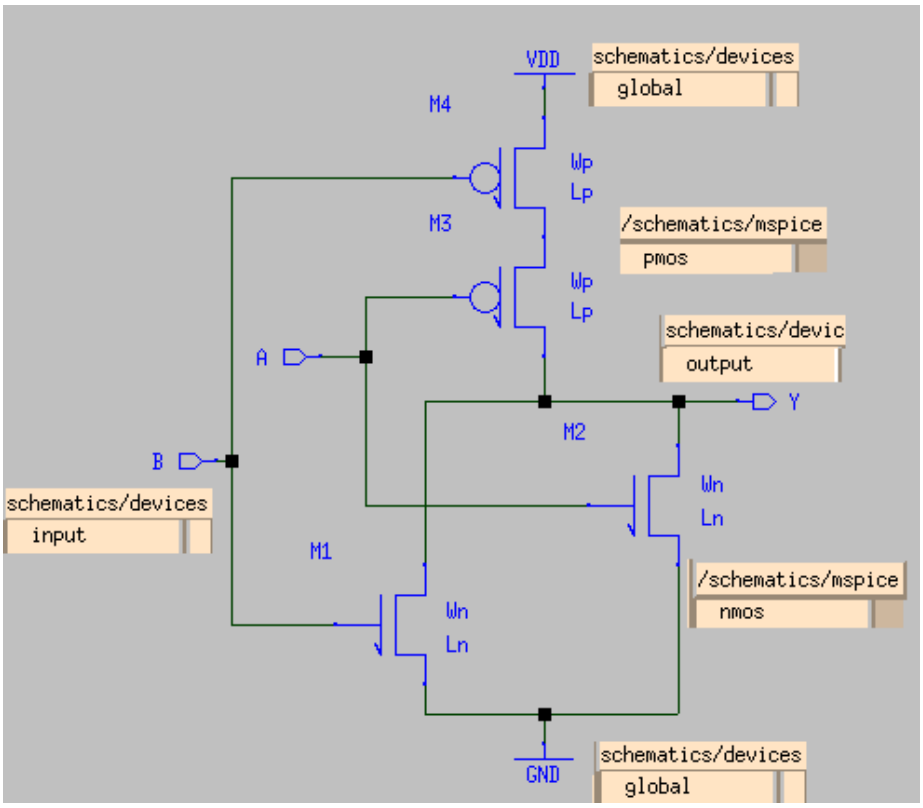
| CASES | INPUT A | INPUT B | OUTPUT Y | DELAY |
|---|---|---|---|---|
| CASE 1 | 1 | 0→1 | 1→0 | |
| CASE 2 | 0→1 | 1 | 1→0 | |
| CASE 3 | 0→1 | 0→1 | 1→0 | |
| CASE 4 | 0 | 1→0 | 0→1 | |
| CASE 5 | 1→0 | 0 | 0→1 | |
| CASE 6 | 1→0 | 1→0 | 0→1 | |

**Explain briefly why these delays are different, and attach your table in the report.**

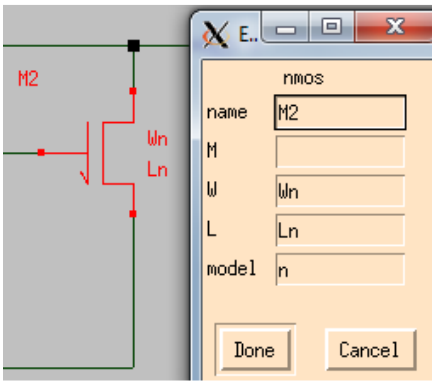
## PART 3: Netlist Generation from SUE

Now we practice how to generate HSpice netlist from SUE.

Build NOR2 gate circuit as follows:




The models you will use are marked on the figure. You should give every model a name by double clicking on it. Note that you can modify the sizes of MOSFETs by double clicking on the symbol:




Save your Schematic to NOR2.sue. Click on Sim\SPICE Netlist. You will see this message ‘Wrote spice netlist to /…/NOR2.sp’.

Modify your generated netlist as follows:

| Orignial | Change to |
|---|---|
| .OPTIONS post NOMOD post_version=9601 | .OPTIONS post=2 NOMOD |
| .include '${MMI_TOOLS}/sue/ schematics/mspice/mmi25.mod' | .include '180nm_bulk.txt' |
| .PARAM vddp=2.25 | .PARAM vddp=2.5 |
| .TEMP 105 | (Remove) |
| .TRAN 5p 10n | .TRAN 0.1ns 20ns |
| * .SUBCKT NOR2 A B Y | .SUBCKT NOR2 A B Y |
| (In all the MOSFET Statements) | Change ‘n’ and ‘p’ to ‘NMOS’ and ‘PMOS’ |
| * .ENDS $ NOR2 | .ENDS $ NOR2 |
| (add before .END) | .param Ln=0.18u<br>.param Lp=0.18u<br>.param Wn=0.18<br>.param Wp=0.72<br>X1 A B Y NOR2<br>VA A gnd 0<br>VB B gnd PULSE vddp 0 5ns 0.1ns 0.1ns 10ns 20ns<br>.MEAS TRAN tpLH TRIG V(B) VAL='vddp/2' FALL=1<br>+ TARG V(Y) VAL='vddp/2' RISE=1<br>.MEAS TRAN tpHL TRIG V(B) VAL='vddp/2' RISE=1<br>+ TARG V(Y) VAL='vddp/2' FALL=1 |

**Save your changes, and attach your printed netlist in your report.**

## PART 4: Netlist Simulation

Simulate your NOR2.sp file with HSpice. Plot the waveforms of V(A) and V(Y) in CScope.

**Attach the waveforms in your report.**

You will also find delays ‘tpHL’ and ‘tpLH’ in ‘NOR2.lis’ file.

Now change the widths of PMOSFETs ‘Wp’ from ‘0.72’ to ‘0.36’ and ‘0.9’; Simulate for these two cases and fill this form:

| CASES | Wp / Wn | tpLH | tpHL | Average delay tp=(tpLH+tpHL)/2 | Rise/fall imbalance \|tpLH - tpHL\|/ tp |
|---|---|---|---|---|---|
| CASE 1 | 0.36 / 0.18 | | | | |
| CASE 2 | 0.72 / 0.18 | | | | |
| CASE 3 | 0.90 / 0.18 | | | | |

**Attach your form to your report.**