UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

ECE 122A VLSI Principles

LAB 3 – Single-Stage CMOS Logic Gate Layout

Due Date: ***Thursday, 10/26/2023, 5:00 pm***

You will learn how to implement a layout for a CMOS logic gate. First carefully read my example story in Part I and then do the work in Part II according to the steps in Part II. You can finish steps 1-3 in Part II on paper at home, and step 4 when in the lab.

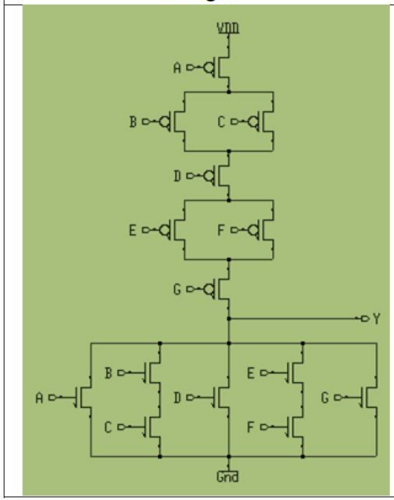
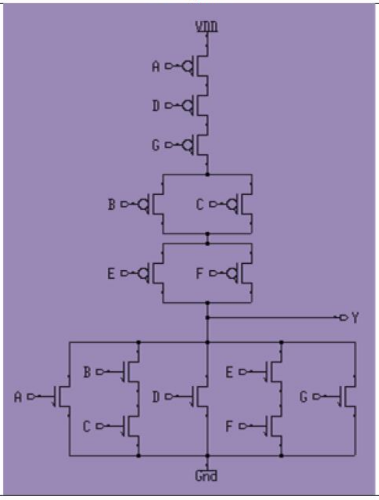
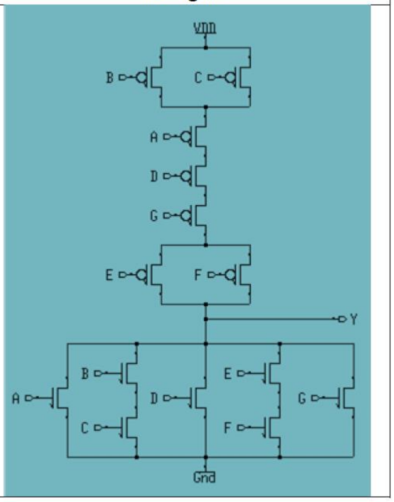
Make sure you understand Eular path, stick diagram and layout rules before starting with Part I.

PART I – EXAMPLE

Build a single-stage CMOS logic gate Layout to implement the Boolean function $Y = \overline{A + BC + D + EF + G}$. Now I will show how to solve this question in 4 steps (Schematic, Eular Path, Stick Diagram and then Layout).

STEP 1 – Sketch a Circuit Schematic

Using CMOS logic, there are many different designs which can implement the function $Y = \overline{A + BC + D + EF + G}$, because gate ordering can be varied. I came up with three different CMOS designs as shown below. There are logically identical.

Design 1	Design 2	Design 3
		

They all implement the function $Y = \overline{A + BC + D + EF + G}$, but I know there should be a best design (the optimum gate ordering), which would have the simplest layout and the smallest layout area.

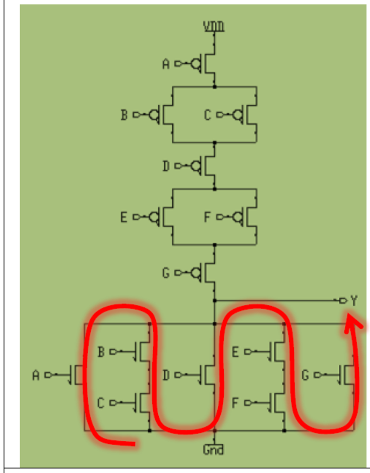
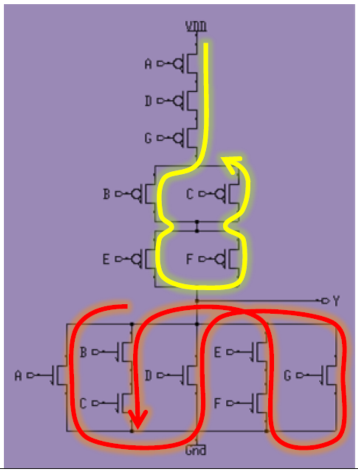
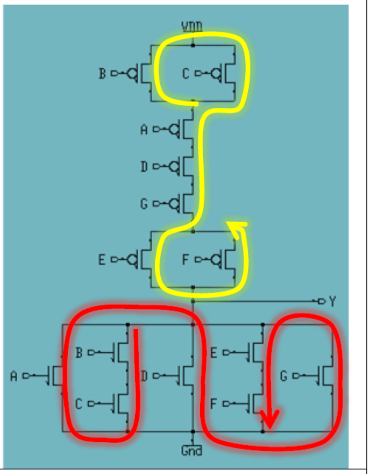
How to find the best design? As we learned from Lecture 4, a simple method for finding the optimum gate ordering is the Euler-path method.

STEP 2 – Find the Eular Path

The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once.

To find the optimal gate ordering, simply find an Euler path in the pull-down network graph and an Euler path in the pull-up network graph with the identical ordering of input labels. If possible, find a common (consistent) Euler path for both graphs.

The figures below show the construction of Euler paths for my three designs.

Design 1	Design 2	Design 3
		

Eular paths:
PUN=No Eular path
PDN=ABCDEFG
No Eular path for PUN
	Eular paths:
	PUN=ADGBEFC
	PDN=ADGFEBC
	No common Eular path
		Eular paths:
		PUN= BCADGEF
		PDN= BCADGEF = PUN
		Common Euler path

Finding a common Euler path in both graphs for the pull-down and pull-up net provides a gate ordering that minimizes the number of active-area breaks.

Note: Euler path is not unique.

For Design 3, there is a common sequence (BCADGEF) in both PUN and PDN graph. According to Lecture 4, the polysilicon gate columns can be arranged according to this sequence, which results in uninterrupted active areas (diffusion strips) for NMOS as well as for PMOS transistors.

For Design 2, there is no common Eular path. But both PUN and PDN have Eular paths.

If the polysilicon gate columns are arranged as ADGBEFC, NMOS diffusion strip will be interrupted.
If the polysilicon gate columns are arranged as ADGFEBC, PMOS diffusion strip will be interrupted.

If I keep NMOS strip and PMOS strip uninterrupted, then the polysilicon gate columns will be interrupted. Any option results in more complex layout and more layout area than Design 3.

For Design 1, there is no Eular path in PUN. Hence, PMOS diffusion strip will be definately interrupted no matter how the polysilicon gate columns are arranged, resulting in more complex layout and more layout area than Design 3.

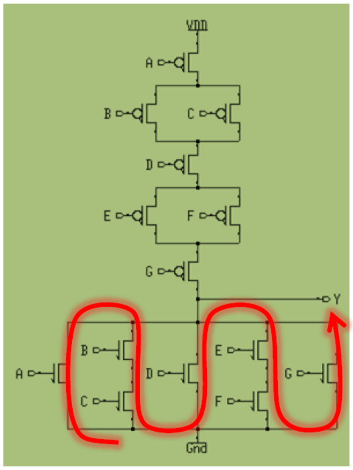
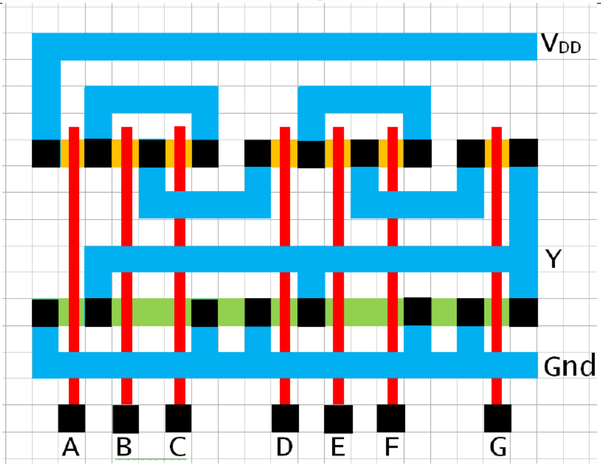
Hence, I claimed that Design 3 is the best among the three. To understand it better, please continue to Step 3.

STEP 3 – Draw Stick Diagrams

In Lecture 4, we introduced the concept of stick diagrams, which can be used very effectively to simplify the overall topology of a layout in the early design phases. With the help of stick diagrams, the designer can have a good understanding of the topological constraints, and quickly test several possibilities for the optimum layout without actually drawing a complete mask diagram.

By drawing stick diagrams, you will understand why I claimed Design 3 was better than Design 1 and 2.

The stick diagram of Design 1 is shown below:

Design 1	Stick Diagram
 VDD A B C D E F G Y B A C D E F G Gnd PUN=No Eular path PDN=ABCDEFG	 🟦 Metal 1 ■ Via 🟥 Polysilicon gate 🟩 N active area (NMOS diffusion strip) 🟨 P active area (PMOS diffusion strip)

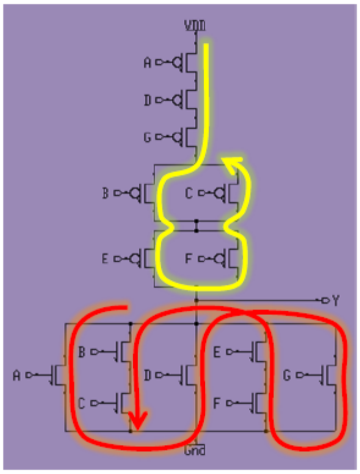
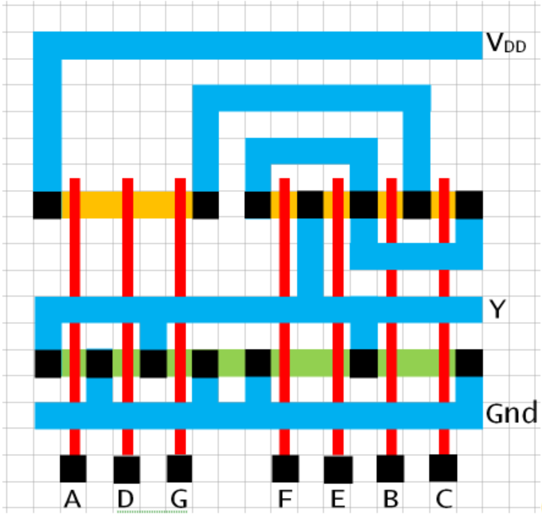
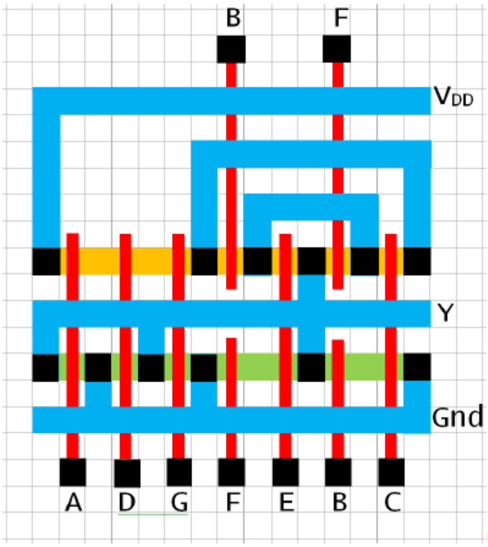
PDN has an Eular path ABCDEFG so that we arrange polysilicon gate colomns (poly) in sequence ABCDEFG. Hence, NMOS diffusion strip (ndiff) is uninterrupted. But PMOS diffusion strip (pdiff) will be definately interrupted no matter how poly are arranged.

Now let us estimate the area of Design 1.

As we learned from Lecture 4, A wiring track (the space required for a metal wire) is 8λ in width (4λ wire width + 4λ spacing), and transistors also consume a wiring track.

Hence, the area is estimated as (8λ * 10 tracks wide) by (8λ * 8 tracks high) = $5120\lambda^2$.

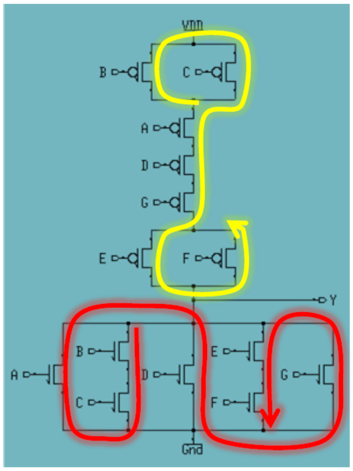
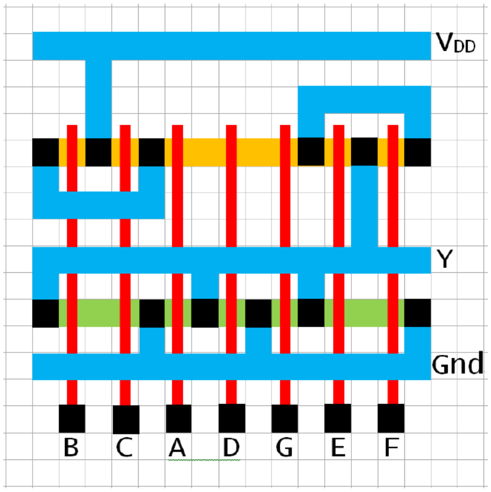
The stick diagrams of Design 2 are shown below:

Design 2	Stick Diagrams
 VDD A D G B C E F Y A B C D E F G Gnd PUN=ADGBEFC PDN=ADGFEBC No common Eular path	 (a)  B F VDD Y Gnd A D G F E B C (b)

As we mentioned in Step 2, since Eular paths for PUN and PDN cannot be the same, we may have either interrupted ndiff/pdiff with uninterrupted poly (a) or uninterrupted ndiff/pdiff with interrupted poly (b).

The area of (a) is (8λ * 9 tracks wide) by (8λ * 9 tracks high) = $5184\lambda^2$.

The area of (b) is (8λ * 8 tracks wide) by (8λ * 9 tracks high) = $4608\lambda^2$.

Design 3	Stick Diagram
 VDD B C A D G E F Y B A C D E G F Gnd Common Euler path: PUN=PDN=BCADGEF	

There is a common Eular path BCADGEF for both PUN and PDN. Hence, I arranged poly in ordering of BCADGEF and drew the stick diagram as shown above, which has uninterrupted ndiff/pdiff and uninterrupted poly.

The area of the stick diagram is (8λ * 8 tracks wide) by (8λ * 8 tracks high) = $4096\lambda^2$.

Then I listed this table, where it is clear that Design 3 is the best.

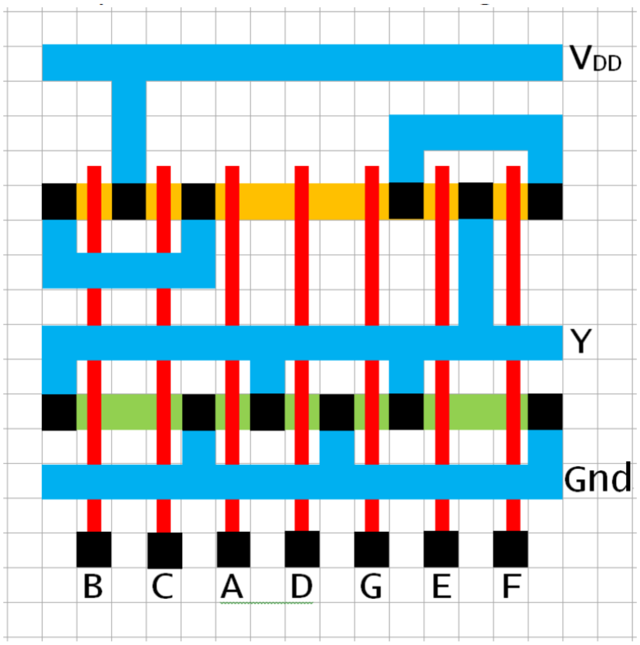
	Design 1	Design 2 (a)	Design 2 (b)	Design 3
pdiff	interrupted	interrupted	uninterrupted	uninterrupted
ndiff	uninterrupted	uninterrupted	uninterrupted	uninterrupted
poly	uninterrupted	uninterrupted	interrupted	uninterrupted
area	$5120\lambda^2$	$5184\lambda^2$	$4608\lambda^2$	$4096\lambda^2$

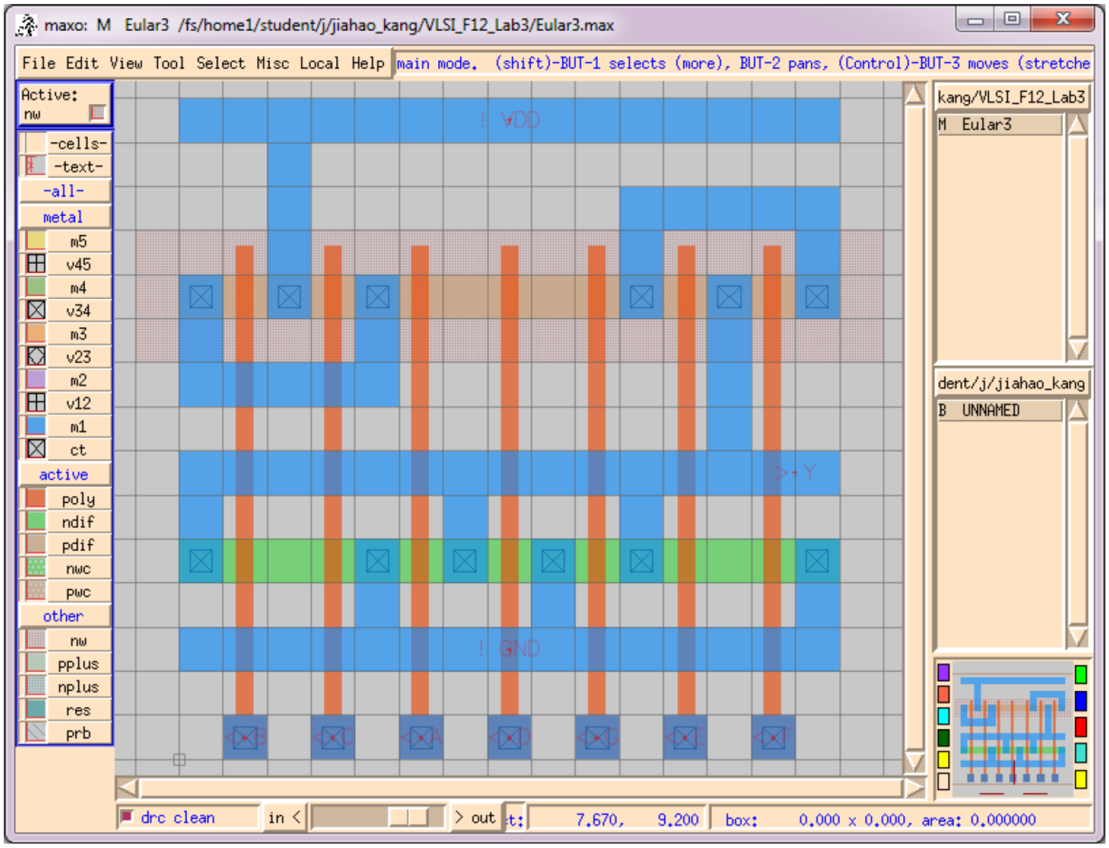
🟥 means not preferred.

Hence, I implemented the layout using Design 3.

STEP 4 –Layout

The layout was drawn according to the stick diagram.




maxo: M Eular3 /fs/home1/student/j/jiahao_kang/VLSI_F12_Lab3/Eular3.max

main mode, (shift)-BUT-1 selects (more), BUT-2 pans, (Control)-BUT-3 moves (stretche

Active: nw

drc clean

7.670, 9.200 box: 0.000 x 0.000, area: 0.000000

In this layout, λ is 0.15um, which means each track is 0.6um wide with 0.6um spacing.

PART II – YOUR TASK

Question: Build a single-stage CMOS logic gate layout to implement Boolean function

$$Y = \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D}$$

You may use $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$ as inputs.

Uninterrupted ndiff/pdiff and uninterrupted poly are preferred. (extra credit).

Hint: Each input may have more than one poly strips.

AB CD	00	01	11	10
00	1	0	1	1
01	0	0	0	0
11	1	0	0	0
10	0	1	1	0

STEP 1 – Sketch a Circuit Schematic

Show how you simplify or deform the Boolean function into a form easy to implement. Attach it to your report.

Hint: forms like $Y = \overline{AB + CD}$ or $Y = \overline{(A + B)(C + D)}$ are easy to implement.

Sketch a transistor-level schematic for a single-stage CMOS logic gate for Y in your report. Attach it to your report.

STEP 2 – Find the Eular Path

Find if there is a common Eular path or not. Write down the Eular paths for PUN and PDN in your report. Attach it to your report.

Also draw the Eular paths on circuit schematic. Attach it to your report.

STEP 3 – Draw Stick Diagrams

Draw the stick diagram in your report. Using DIFFERENT COLORS for metal, poly, ndiff, pdiff and vias. Attach it to your report.

Estimate the area. Attach it to your report.

STEP 4 –Layout

Draw the layout in MAX.

I have a requirement that λ is 0.15 um, which means each track is 0.6 um wide with 0.6um spacing.

Note: Please do this necessary setting: "File -> User preferences -> Grid Setup -> coarse grid size" (set to 0.6) Turn on grids using "View->Toggle Grid".

You may use "Edit -> Edit properties" to modify the dimension of a wire.

You may use the via models from library "/ece/mmi/max/cells". Your layout should be DRC clean.

Print out your MAX layout in your report. Attach it to your report.