

UNIVERSITY OF CALIFORNIA, SANTA BARBARA  
Department of Electrical and Computer Engineering  
ECE 122A VLSI Principles

## LAB 4 – Inverter, CMOS Sizing and Delay

Due Date: **Thursday, 11/02/2023, 5:00 pm**

For this lab, please use 65nm CMOS transistor model from <http://ptm.asu.edu/>.

### **PART I -- Inverter VTC**

(A) Show the VTC curves of minimum size inverter in 65nm technology with  $V_{DD} = 1.5$  V. Simulate your inverter netlist with HSPICE, and then plot the VTC.

**Attach your netlist and VTC curve in your report.**

(B) Increase the threshold voltage of NMOS transistor by 0.15V and decrease the (absolute value) threshold voltage of PMOS by 0.2V. Plot the VTC curve.

**Attach the VTC curve in your report, and explain the shift in VTC curve.**

(C) Start with the netlist in (A), decrease the threshold voltage of NMOS transistor by 0.15V and increase the (absolute value) threshold voltage of PMOS by 0.2V.

**Attach the VTC curve in your report, and explain the shift in VTC curve.**

Hint: Refer to HSpice Manual Page 690/1714 (Session 15-12), where you can find out how to adjust  $V_T$ .

### **PART II – Sizing of Inverter Chain**

#### **(A) Measurement of the Parasitics of Inverter**

Build a unit size inverter with 65nm model. Simulate it with HSPICE. Add this statement to your netlist:

```
.OP
```

In the .lis file, you will find 'cdtot' and 'cgtot' for each transistor. The Values are difference for cutoff, linear and saturation. Think about how to calculate the average.

**Based on the values you find, estimate the input capacitance and self-load coefficient of the unit size inverter.**

### (B) Inverter Chain Sizing, for Given N

Use **three** inverters in series to drive a 5 pF capacitor. Based on Lecture 10, calculate the optimal sizing for each stage. Write or generate a netlist for the inverter chain you optimized, and calculate the delay of the inverter chain through simulation.

**Attach your netlist, and results in the report.**

Hint: refer to HSPICE Manual Page 141/1714 (Session 4-19), where you will see how to use .measure statement. You might find these statements useful:

<pre>.subckt INV X Y Size=1 * Defining subcircuit with parameters M1 Y X 0 0 NMOS L=65n W='Size*65n' M2 Y X VDD VDD PMOS L=65n W='Size*130n' .ends</pre>	
X2	2 3 INV Size=4 * Using subcircuit with parameters
Cout	out 0 5p * Defining load capacitance

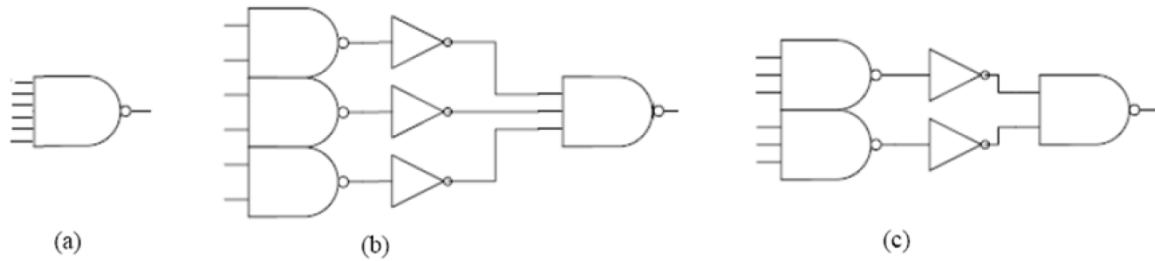
### (C) Inverter Chain Sizing

Now design another inverter chain to drive a 5 pF capacitor, with **optimal** number of stages. Based on Lecture 10, calculate the optimal inverter number and the optimal sizing for each stage. Write or generate (by SUE) a netlist for the inverter chain you optimized; simulate for the delay.

Attach you're the inverter number, optimal sizing, netlist, and the delay to your report.

## PART III – Sizing of CMOS Gate

Consider the design of a six input NAND gate. In the figure below, three different approaches for implementation of such a gate are given. Use 65 nm technology with  $V_{DD} = 1.5$  V.



**(A) Optimization of Gates**

Let the output node drive a 5 pF capacitor. **Show how you will calculate the optimal sizing for each stage in (a) (b) and (c).**

**(B) Delay Measurement**

Build netlists for the three circuits. **Attach your netlists.**

Compare the delay  $tp=(tplh+tpfl)/2$  of these three implementations. For low-to-high transition, assume that all but one of the inputs is high and transition begins when the last input goes high. For low-to-high transition, assume that just one of the inputs goes low and the other inputs remain high.

Measure the average power consumption  $P_{avg}$  of these circuits, when there is one low-to-high and one high-to-low at the output in a specified time period (use same input transitions as in part (a)).

Note: Refer to HSpice Manual Page 141/1714 (Session 4-19) where you can find out how to use .measure statement

Compare the three designs using energy-delay product (EDP) metric, which is defined as:  $EDP = P_{avg} \cdot tp^2$

**Fill the table below with simulation results and explain which circuit would be your choice if you want to optimize power, delay, or the EDP.**

	Delay (tp)	Power	EDP
Circuit (a)			
Circuit (b)			
Circuit (c)			