

Name: _____

ECE 122A Fall 2022

Perm #: _____

Prof. Kaustav Banerjee

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

MIDTERM EXAMINATION - ECE122A

November 3, 3:30-4:45 PM

READ CAREFULLY:

- This is a **CLOSED BOOK** Exam. One page (8.5"x11") of cheat-sheet is allowed. Calculators are OK.
- **READ** the questions carefully before answering. Include all your answers in locations specified on these pages. Show **ALL WORKING** used to arrive at answers. Use space provided for all working. Use the back sides if necessary. There are **18** pages including the cover page and a blank page at the end. Be sure to write Your **NAME/Perm No.** on **EVERY PAGE**.

Question	Scores
#1	/30
#2	/25
#3	/25
#4	/20
TOTAL	/100

Good Luck!

Part I. (30 pts) For each question, choose ALL the CORRECT statements among the four. Fill in the table below with your answers: (Approximate time: 15 min)

Question	1	2	3	4	5	6	7	8
Answer								
Question	9	10	11	12	13	14	15	
Answer								

(Completely correct: 2pts; for each correct answer not chosen/every incorrect answer chosen: -0.5 pt)

1) **(CMOS Processing)** Select the right statement(s): (2 pts)

- A. Phosphorous is a p-type dopant in Silicon.
- B. Uninterrupted diffusion strips are possible only if there exists a common Euler path in the logic graph.
- C. Irradiation of light weakens the photoresist in the exposed regions of a positive photoresist.
- D. PMOS transistors utilize a p-doped well.

2) **(Band Model)** Select the right statement(s): (2 pts)

- A. Silicon crystal has a diamond-type crystal lattice with sp³ bonding.
- B. Splitting of energy states occurs due to Coulombic repulsion.
- C. Higher energy bands generally span wider energy range.
- D. The band gap of a semiconductor is typically larger than that of an insulator.

3) **(Metals, Semiconductors and Insulators)** Select the right statement(s): (2 pts)

- A. Electrical conduction happens if one band is neither empty nor full.
- B. The material is insulator if adjacent bands overlap in energy.
- C. Pure silicon at absolute zero temperature is insulator.
- D. Insulators have smaller band-gap than that of metals.

4) (**Static CMOS**) Select the right statement(s): (2 pts)

- A. In a static CMOS design, only one of PUN and PDN will be turned on during each output transition. Therefore, static power consumption is greatly reduced.
- B. The output of a static CMOS circuit is degraded.
- C. CMOS logic does not need to be sized.
- D. A CMOS NAND gate has PMOS's connected in series in the PUN.

5) (**Pass Transistor & Transmission Gate**) Select the right statement(s): (2 pts)

- A. NMOS pass transistor guarantees a strong 1.
- B. In a transmission gate, PMOS and NMOS need to be sized for equal driving capacity.
- C. Transmission gate restores the signal since combining PMOS and NMOS gives strong 0 and 1.
- D. Transmission gates are slower than pass-transistors.

6) (**Sequential Circuits**) Select the right statement(s): (2 pts)

- A. The latches you need for designing a flip flop (FF) can have same level sensitivity (high or low).
- B. A flip-flop is an edge-triggered device.
- C. You can design a positive edge flip-flop by having a series combination of a high-sensitive latch followed by a low-sensitive latch.
- D. Hold time determines the maximum operational frequency of a circuit.

7) (**Carrier Statistics**) Select the right statement(s): (2 pts)

- A. The Fermi-Dirac distribution is an inverted step function at absolute zero temperature.
- B. The resistance of an intrinsic semiconductor increases with increase in temperatures.
- C. Semiconductor is still electrically neutral when donor impurities are added.
- D. Only one type of carrier can contribute to the current in semiconductors.

8) (**P/N Junction**) Select the right statement(s): (2 pts)

- A. At equilibrium, drift and diffusion currents are zero in a P/N junction.
- B. Depletion region of a P/N junction is electrically neutral because carriers are depleted.
- C. The depletion width of a P/N junction increases as forward bias is applied.
- D. Reverse bias increases the electric field in the depletion region of a P/N junction.

9) (**MOS Capacitor**) Select the right statement(s): (2 pts)

- A. The frequency in a MOSCAP is limited by the thermal generation of minority carriers in the bulk required to form the inversion layer.
- B. When inversion happens in NMOS, density of electrons on surface equal the density of holes in bulk.
- C. You have depletion charge even when the MOSFET is under inversion.
- D. The work function is the amount of energy needed to excite carriers from the Fermi level to the free space.

10) (**MOSFET**) Select the right statement(s): (2 pts)

- A. Body doping concentration is generally higher than that of the source and drain regions.
- B. Subthreshold leakage current increases with increase in temperature.
- C. Threshold voltage is always positive in value.
- D. The threshold voltage of a MOSFET increases when you shine light.

11) (**Threshold voltage of MOS**) Select the right statement(s): (2 pts)

- A. Presence of positive fixed oxide charges in the oxide decreases NMOS threshold voltage.
- B. A MOSFET with a larger threshold voltage drives larger current.
- C. The threshold voltage can be decreased by decreasing the gate oxide thickness.
- D. The threshold voltage of a transistor is determined by its width and length.

12) (**Inverter and Ring Oscillator**) Select the right statement(s): (2 pts)

- A. CMOS VTC curve shifts to right if PMOS oxide thickness reduces.
- B. CMOS switching threshold (V_M) decreases if NMOS channel width increases.
- C. Pseudo-NMOS inverter consumes more static power than CMOS inverter.
- D. A 3-inverter-ring oscillates faster (i.e., has higher frequency) than a 5-inverter ring oscillator

13) (**Inverter Sizing**) Select the right statement(s): (2 pts)

- A. The NMOS and PMOS are always equally sized in a balanced inverter.
- B. The delay of an inverter will not be zero when external load capacitance is zero because of the existence of internal load capacitance.
- C. Scaling the size of the inverter has no effect on the intrinsic delay of the inverter.
- D. A ring oscillator requires an even number of inverters connected in a circle.

14) (**Logical Effort**) Select the right statement(s): (2 pts)

- A. Inverter has the smallest logical effort of all static CMOS gates.
- B. Intrinsic delay increases as the gate sizing increases.
- C. Logic effort of a 3-input NAND gate is larger than that of a 2-input NOR gate.
- D. Logical effort increases with gate complexity.

15) (**Chain of logic gates**) Select the right statement(s): (2 pts)

- A. The delay of a chain of inverters decreases as you keep on increasing their size.
- B. A buffer is two inverters connected in parallel.
- C. A single-stage 6-input NAND gate has lower delay than a 3-stage 6-input NAND gate.
- D. The total dynamic energy consumption of a chain of inverters is independent of the total number of stages, and only depends on the output capacitance.

Part II. Threshold Voltage Modulation (25 pts) (Approximate time: 25 min)

In this problem, you will calculate the threshold voltage of a MOSFET and plot the band-diagram based on the threshold voltage value. Also, the effect of oxide charge and body-bias will be discussed.

Assume you have a n-MOSFET fabricated on Silicon channel with the following design parameters:

- Crystal:
Intrinsic carrier concentration = 10^{10} cm^{-3} , Bandgap = 1.1 eV
- Doping:
Channel = 10^{16} cm^{-3}
- Gate: n⁺-poly (heavily doped Si with fermi level lying at conduction band edge)

The relative dielectric constant of Silicon is 12.

You must evaluate the following.

- A. Evaluate the position of the Fermi-level (E_F) in the silicon substrate w.r.t the conduction band (E_C) and with respect to the intrinsic Fermi-level (E_i) for the n-MOSFET with oxide parameters: $\epsilon_{\text{ox}} = 24$, $t_{\text{ox}} = 3\text{nm}$. (5)

- B. Using the values derived in part (A) calculate the threshold voltage (V_T) using the given formula which is valid when there is no oxide charge or body bias (hint: use the appropriate value of ϕ_S for determining the threshold voltage): (10)

$$V_{GS} = \phi_{ms} - \phi_S - \frac{Q_{dep}}{C_{ox}}$$

$$Q_{dep} = -\sqrt{2qN_A\epsilon_0\epsilon_{Si}|\phi_S|}$$

- C. Based on the threshold voltage derived in part (B), plot the band-diagram across the gate-oxide-body for zero-bias condition. Ensure that the band-diagram correctly represents the operating regime of the MOSFET (cutoff, depletion, inversion) and the E_F , E_i and E_C are labelled in your drawing. (5)

- D. If now we assume that charges are trapped in the oxide ($Q_{ox} = 10^{12}\text{cm}^{-2}$), the threshold voltage is going to change. Does the threshold voltage (a) increase or decrease? This change can be rectified by applying a body-bias (V_{SB}). Determine if the applied V_{SB} should be (b) positive, negative or zero. (2.5+2.5)

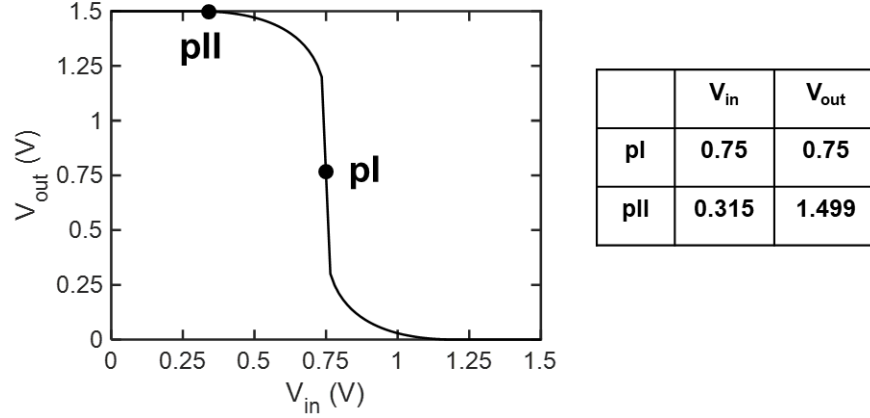
Problem III CMOS Inverter Fundamentals (25) (Approximate time: 25 min)

Suppose you have two identical transistors, one PMOS and another NMOS, both sized appropriately (width and length of PMOS and NMOS are W_{p0} , L_{p0} , W_{n0} , L_{n0} , $W_{p0}=2xW_{n0}$, $L_{p0}= L_{n0}$) so that the VTC of the inverter is symmetric.

- A. The width and length of the PMOS is increased by a factor of 10 ($W_p/W_{p0} = L_p/L_{p0} = 10$). What changes do you expect in the (i) VTC, (ii) Low-to-high delay relative to the original inverter (assuming zero external capacitance) and (iii) Power consumption relative to the original inverter if the frequency is held constant.

(3+3+3)

- B. In the VTC of the inverter (see figure below), two DC bias points (pI and pII) are marked. (i) Calculate (i) the current flowing through inverter and (ii) determine the operating regime (cutoff, linear, saturation) of the NMOS and PMOS transistors for both cases. Assume zero body bias. (8+8)



The current equations for the NMOS and PMOS are given by:

$$I_n = k_n \frac{W_n}{L_n} \times \begin{cases} 0 & V_{GS} - V_{tn} \leq 0 \\ V_{DS}(V_{GS} - V_{tn} - \frac{V_{DS}}{2}) & V_{GS} - V_{tn} > 0, V_{DS} \leq V_{GS} - V_{tn} \\ \frac{(V_{GS} - V_{tn})^2}{2} & V_{GS} - V_{tn} > 0, V_{DS} > V_{GS} - V_{tn} \end{cases}$$

$$I_p = k_p \frac{W_p}{L_p} \times \begin{cases} 0 & V_{GS} - V_{tp} \geq 0 \\ V_{SD}(V_{SG} + V_{tp} - \frac{V_{SD}}{2}) & V_{GS} - V_{tp} < 0, V_{DS} \geq V_{GS} - V_{tp} \\ \frac{(V_{SG} + V_{tp})^2}{2} & V_{GS} - V_{tp} < 0, V_{DS} < V_{GS} - V_{tp} \end{cases}$$

The MOSFET parameters are:

$$k_n = 2k_p = 100 \frac{mA}{V^2}, V_{DD} = 1.5V, V_{tn} = -V_{tp} = 0.3V, \frac{W_p}{L_p} = 2 \frac{W_n}{L_n}$$

Part IV. CMOS Logic Gate Design (20 pts) (Approximate time: 20 min)

In this question you will design and evaluate a variable fan-in NAND gate.

- A. Determine the size of each transistor in the pull-up and pull-down network in a general N-input NAND gate. Clearly state your reasoning for full credit. (5)

B. Determine the logical effort (g) and the relative parasitic effort (p) of the N-input NAND gate. (4+4)

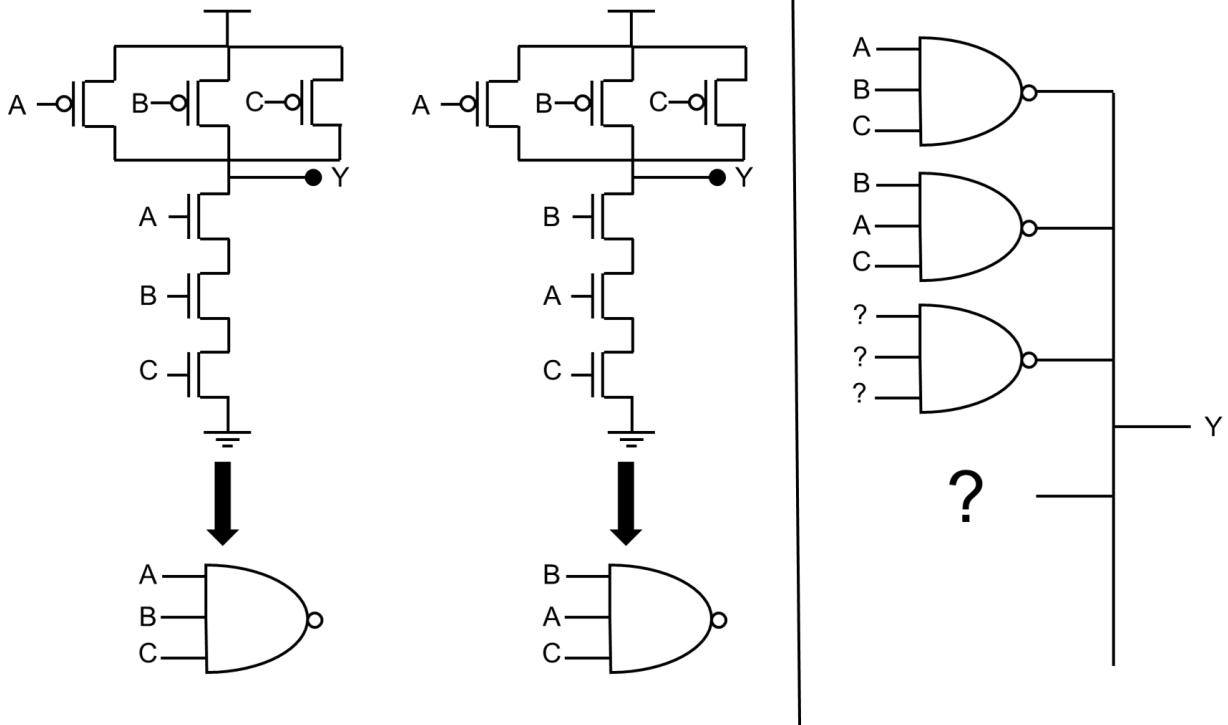
C. You have learnt through your labwork that there is huge mismatch in the high-to-low delay (see figure and table below) for a 2-input NAND gate when different input signals individually switch from low to high.



In certain applications, it is extremely important for this delay mismatch to be as low as possible. One way to accomplish this is to use two NAND gates in parallel with a different input sequences (to cover all possible combinations) in the pull-down network.

Draw the design for such a 3-input NAND gate (see below figure to get the general idea) with minimal delay mismatch.

(4)



- D. Calculate the area overhead (ratio) of this equal delay N-input NAND gate compared to the original single N-input NAND gate. (3)

