ECE 122A
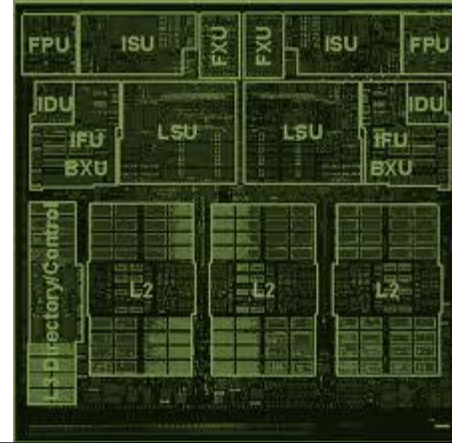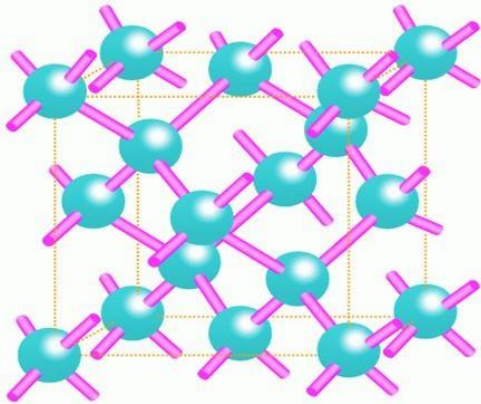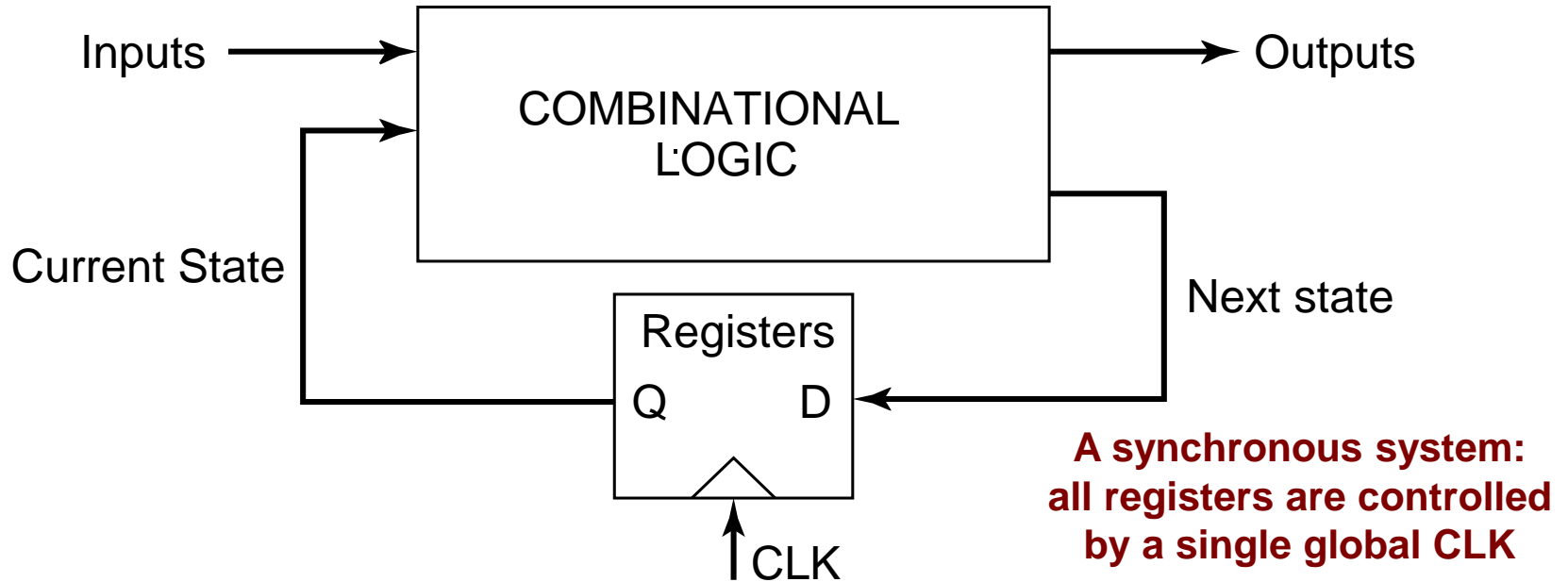# *VLSI Principles*

Lecture 14

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

Kaustav Banerjee

Designing Sequential Logic Circuits

Kaustav Banerjee

Sequential Logic

All useful systems require storage of state information….

Inputs → COMBINATIONAL LOGIC → Outputs

Current State

Next state

Registers

Q   D

↑ CLK

A synchronous system: all registers are controlled by a single global CLK

A generic Finite State Machine (FSM) consisting of combinational logic and registers.

Output of the FSM = *F* (*current inputs*, *current state*)

Next State is determined based on current state and current inputs—fed to the input (D) of the registers

At the rising edge of the CLK, D copied to Q (with some delay)

Note: There are 2 storage mechanisms: 1) positive feedback and 2) charge storage

Classification of Memory Elements

❑ Background Memory: large centralized memory core (high density array structures)---SRAMs and DRAMs

❑ Foreground Memory: embedded in a logic (individual registers or register banks)—focus of this section

Kaustav Banerjee

Classification of Memory Elements

Static Memory:

❑ preserves state as long as power is ON

❑ built by using positive feedback or regeneration where the circuit consists of intentional connections between the output and input of a combinational circuit

❑ most useful when register will not be updated for extended periods of time (eg., configuration data loaded at power-up time).

❑ Condition also holds for most processors that use conditional clocking, (gated CLK) where the CLK is turned off for unused modules----**no guarantee on how frequently the registers will be clocked and static memories are needed to store information.**

❑ bistable element is the most popular form

Kaustav Banerjee

Classification of Memory Elements

Dynamic Memory:

❑ store data for short (ms) period of time

❑ based on the principle of temporary charge storage on parasitic capacitors in MOS devices

❑ similar to dynamic logic….. capacitors need to be refreshed periodically to compensate for charge leakage

❑ significantly simpler----hence, provide higher performance and lower power dissipation

❑ most useful in datapath circuits that require higher performance levels and are **periodically clocked**

Kaustav Banerjee

Naming Conventions

❑ Definitions:

- a latch is a level sensitive device
- a register is an edge-triggered storage element

❑ There are many different naming conventions

- For instance, many books call edge-triggered elements flip-flops
- This may lead to confusion however…
- Any bistable component formed by the cross coupling of gates is a flip-flop (FF)
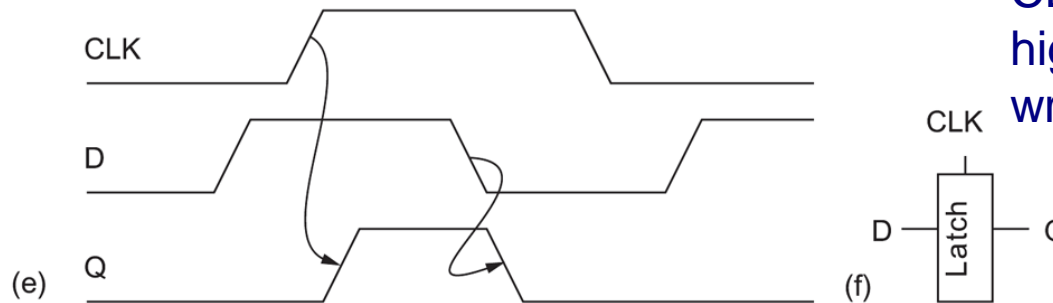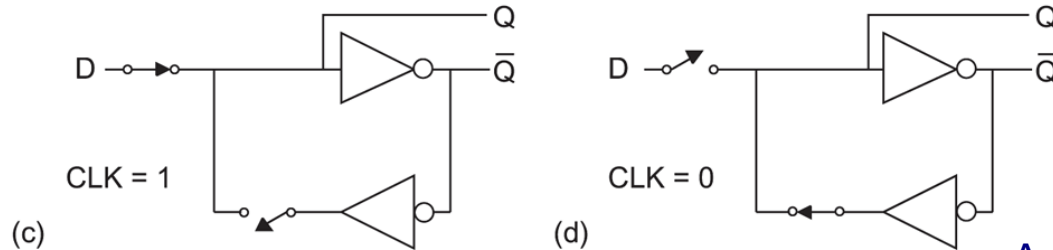
Kaustav Banerjee

Latches

Multiplexer based
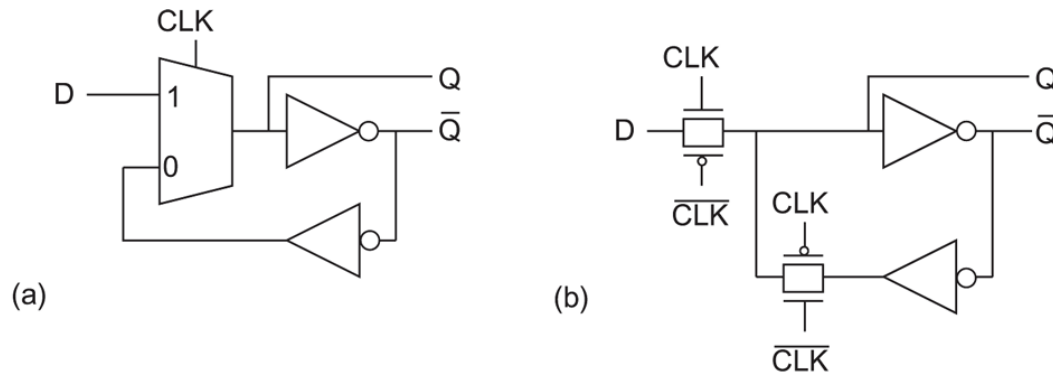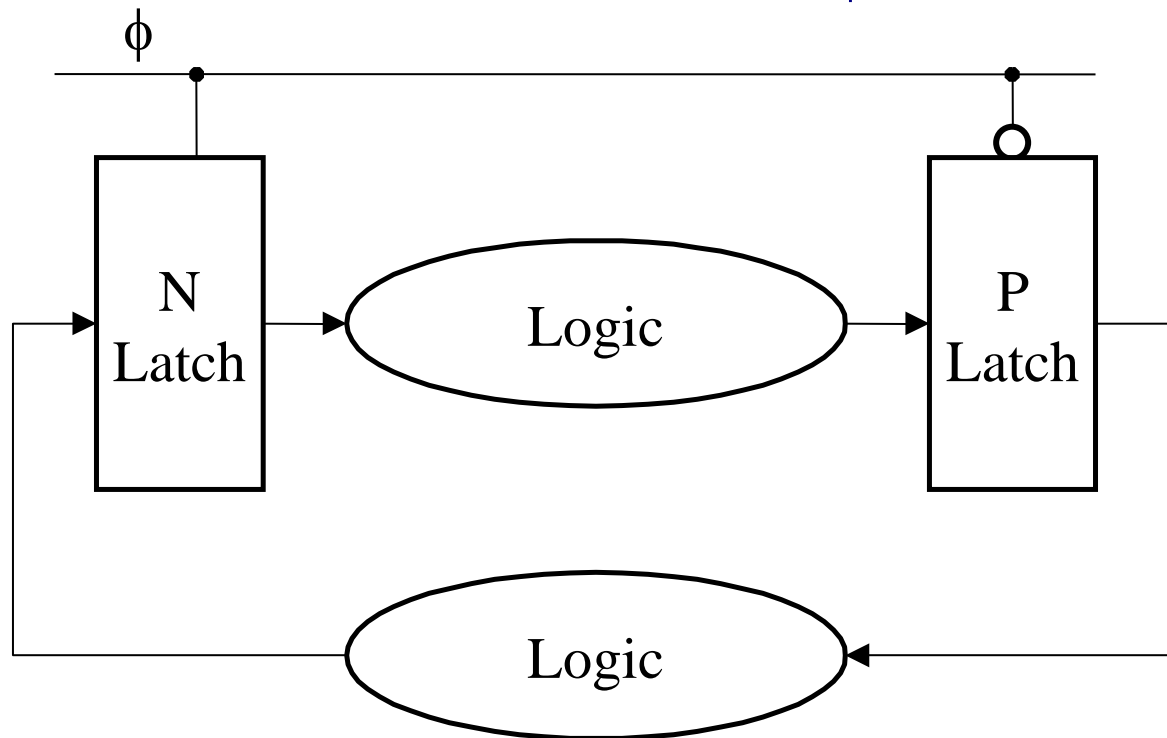
CLK=1: D to Q

CLK=0:Holds state of Q

As long as CLK remains high, D will be written on Q

FIG 1.30 CMOS positive-level-sensitive D latch

Latch-Based Design

• N (negative) latch is transparent when $\phi = 0$

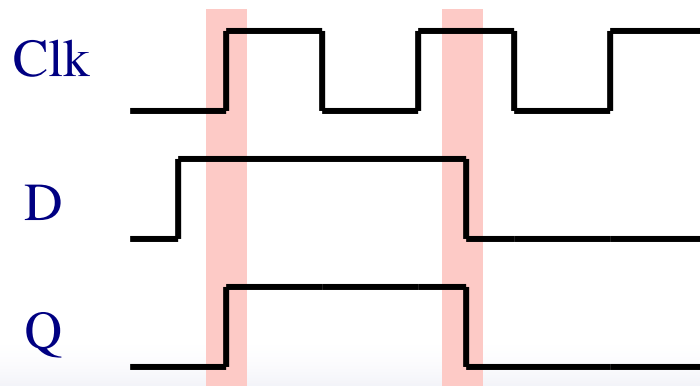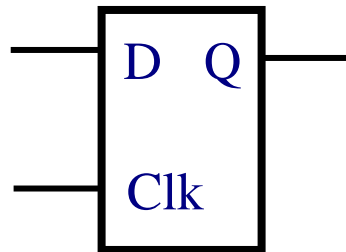• P (positive) latch is transparent when $\phi = 1$

Difficult to eliminate Race conditions…..under CLK overlap

Kaustav Banerjee

Timing of P/N Latches

Positive Latch

In → D — Q → Out

G

↑ CLK

Negative Latch

In → D — Q → Out

G

↑ CLK

Value of In is not important…

Value of In when clk goes low will be transferred to the Out…and sampled by next latch

clk

In

Out

Out stable

Out follows In

When clk is high…

clk

In

Out

Out stable

Out follows In

When clk is low…

Kaustav Banerjee

Latch versus Register

❑ Latch

stores data when clock is **high** (or low)

❑ Register

stores data when clock **rises** (or falls)

What kind of latch is this?

D Q

Clk

What kind of Register is this?

D Q

Clk

Clk

D

Q

Clk

D

Q

Kaustav Banerjee
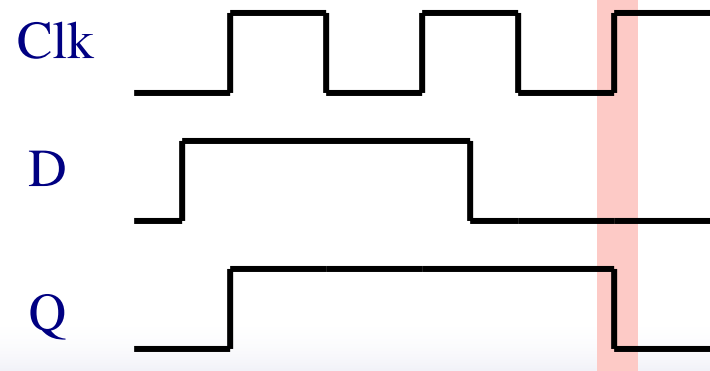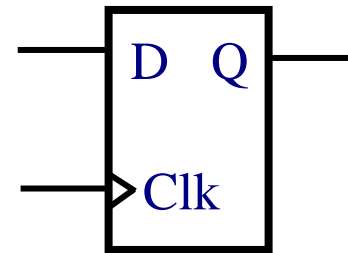
Characterizing Timing

Register

Latch

Data is ready when Clk arrives….
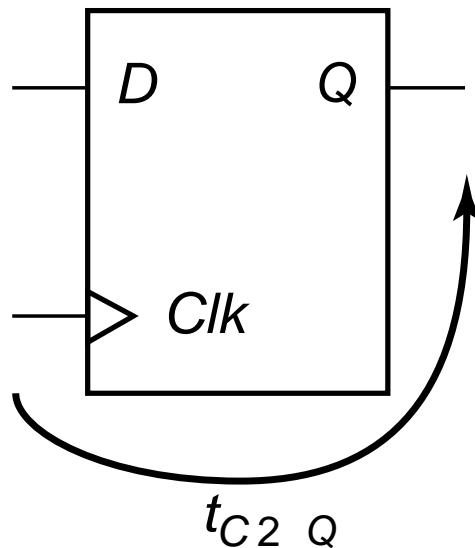
t_{D2Q}

Requires an extra timing parameter…

D   Q

D   Q
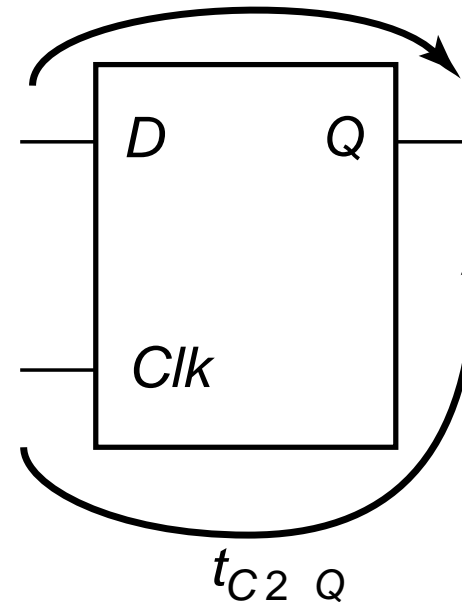
Data may arrive after Clk edge….

> Clk

Clk

t_{C2Q}

t_{C2Q}

*Note: In a **FF**, D is valid before CLK edge arrives……hence **only c2q** is relevant.*

*In a **Latch**, the relevant timing parameter (c2q or d2q) depends on the **relative position of the arrival of D w.r.t the clk edge**……if D arrives after clk edge, then d2q is important, while if D arrives before clk edge, c2q is important.*

Kaustav Banerjee

Registers or Flip-Flops

Combines two latches:

One +ve sensitive (slave) and one –ve sensitive latch (master)

Edge Triggered FF or Master-Slave FF

CLK=0: D to QM

$$\overline{QM} = \overline{D}$$

Slave holds previous value of Q

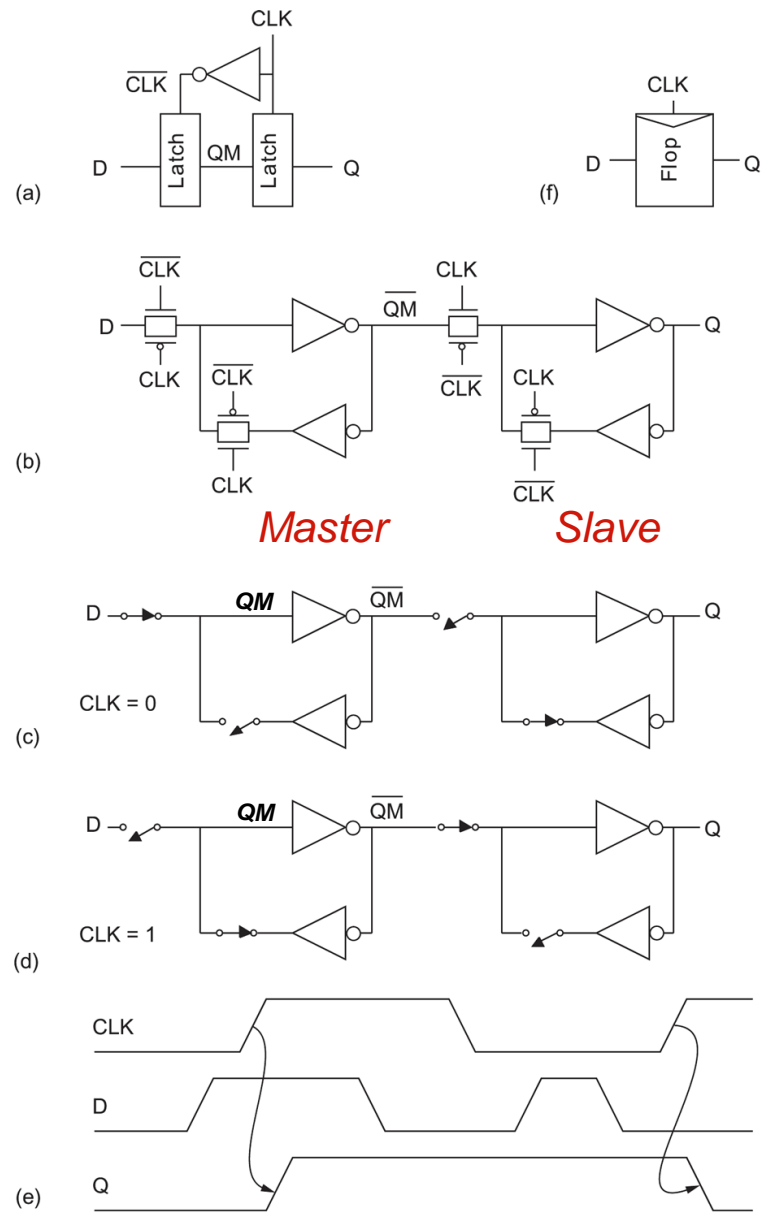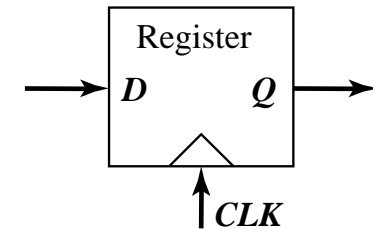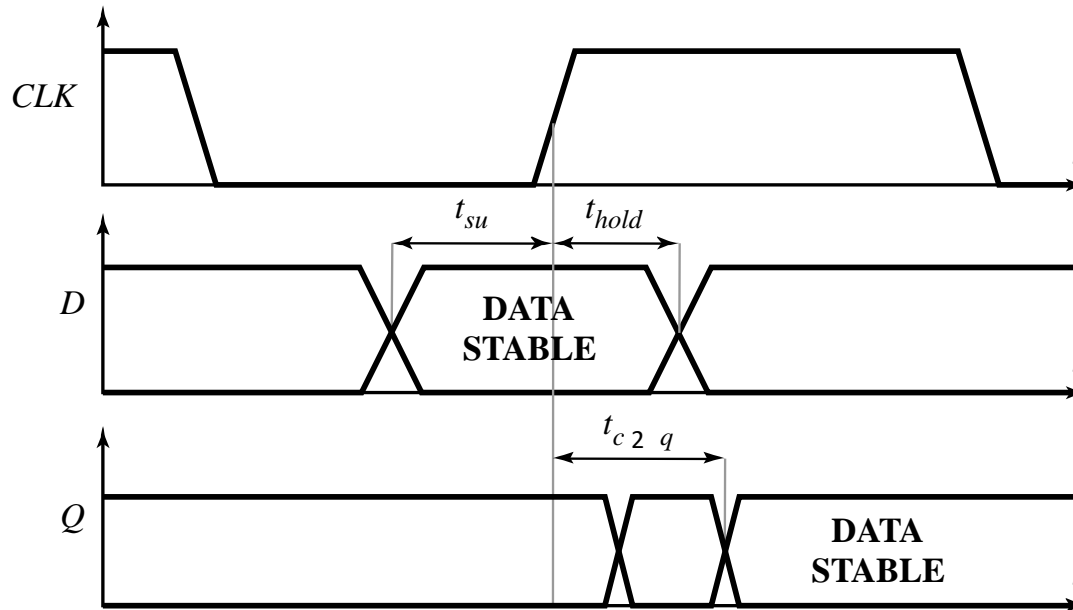*CLK=1: master can't sample input and holds value of D*

Slave opens and QM=(D) =Q

Master   *Slave*

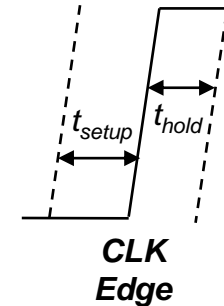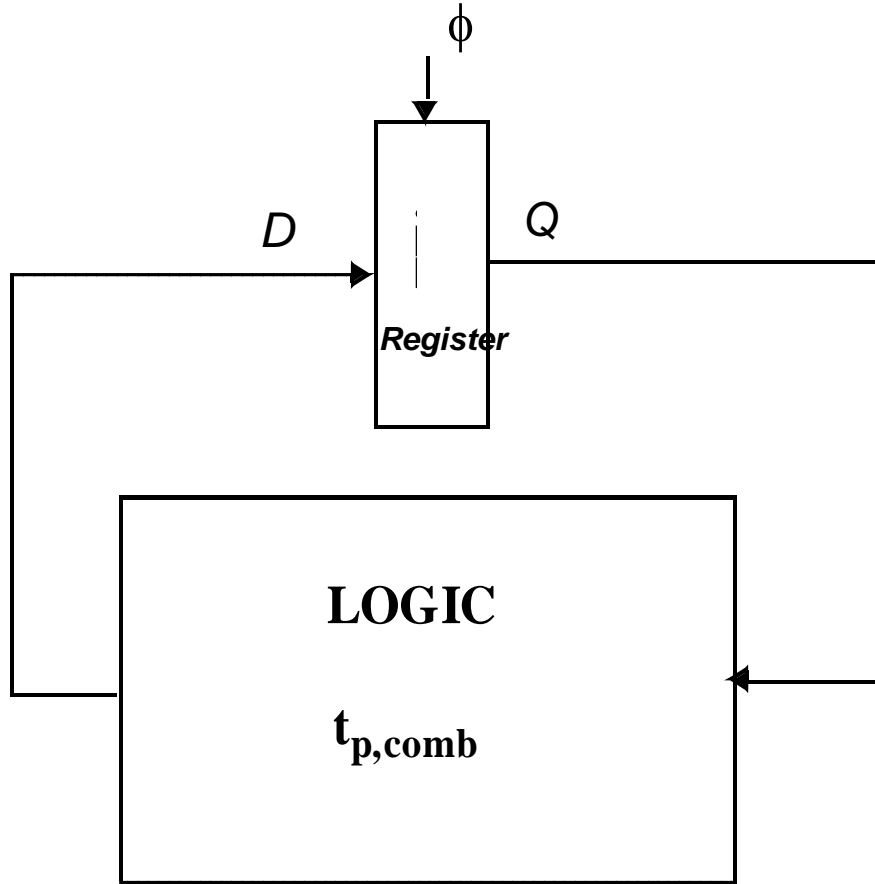**FIG 1.31** CMOS positive-edge-triggered D flip-flop

Timing Definitions

t_{su}= setup time =time for which the data inputs (D) must be valid before the CLK edge

t_{hold}= hold time =time for which data input must remain valid after the CLK edge

t_{c2q}= worst case propagation time through the Register (w.r.t the CLK edge)

Maximum Clock Frequency

ϕ

D   Q

Register

LOGIC

$t_{p,comb}$

t_{setup} t_{hold}

CLK Edge

2) $t_{cdreg} + t_{cdlogic} > t_{hold}$

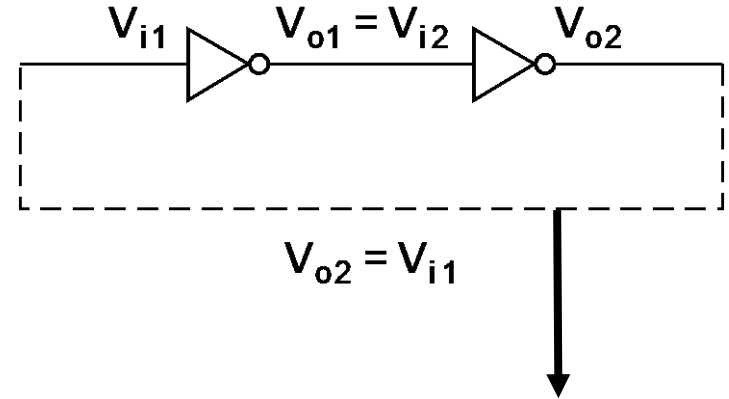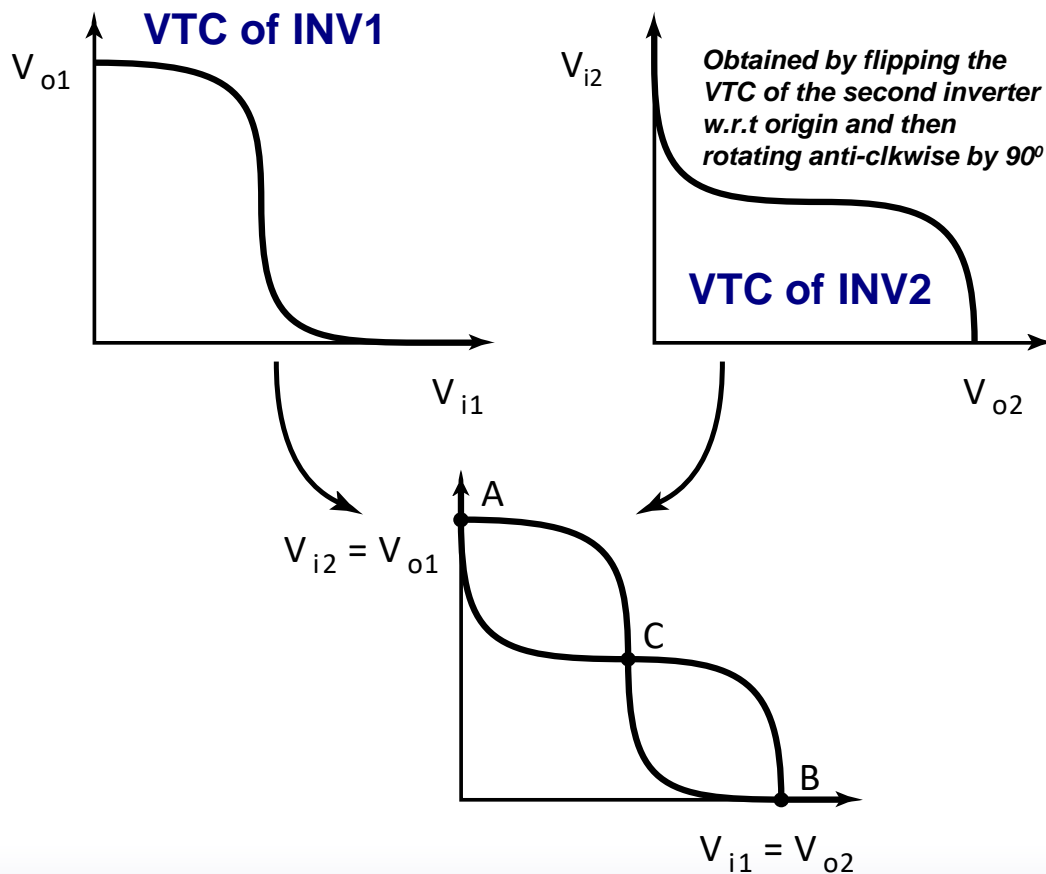t_{cd}: **contamination delay = minimum delay**

To ensure that the input data of the sequential elements is held long enough after the CLK edge and is not modified too soon by the new wave of data coming in

1) $T_{min} = t_{clk\text{-}Q} + t_{p,comb} + t_{setup}$

Clk period must accommodate the longest delay of any stage in the network

Static Latches and Registers

Static Memories use Positive Feedback: Bi-Stability

VTC of INV1

V_{o1}

V_{i1}

V_{i2}

Obtained by flipping the VTC of the second inverter w.r.t origin and then rotating anti-clkwise by 90^0

VTC of INV2

V_{o2}

$V_{i1} \xrightarrow{} V_{o1} = V_{i2} \xrightarrow{} V_{o2}$

$V_{o2} = V_{i1}$
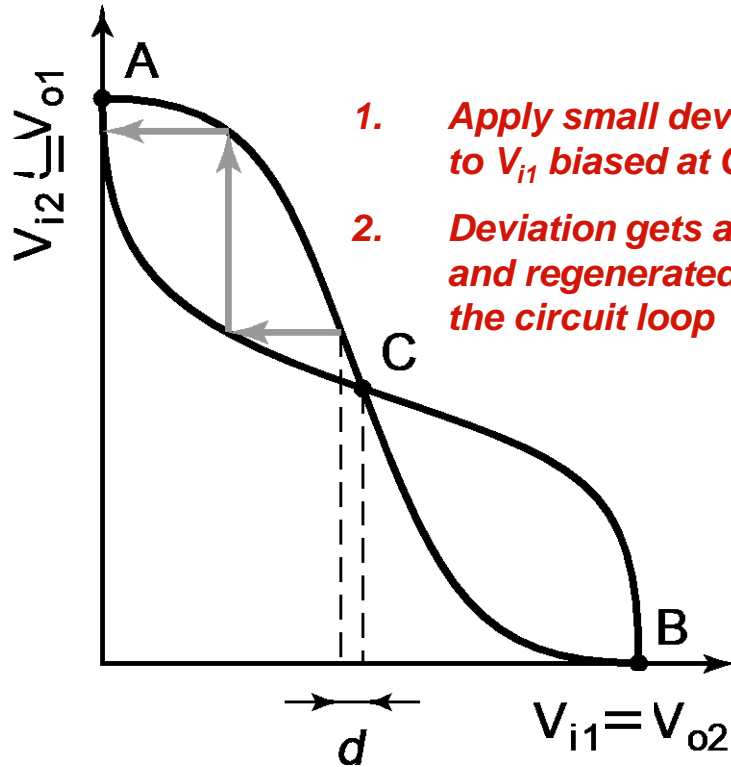
A

$V_{i2} = V_{o1}$

C

B

$V_{i1} = V_{o2}$

A, B, and C are the only three possible operating points

If gain>1 in the transient region: A and B are the only stable operating points, C is a metastable point
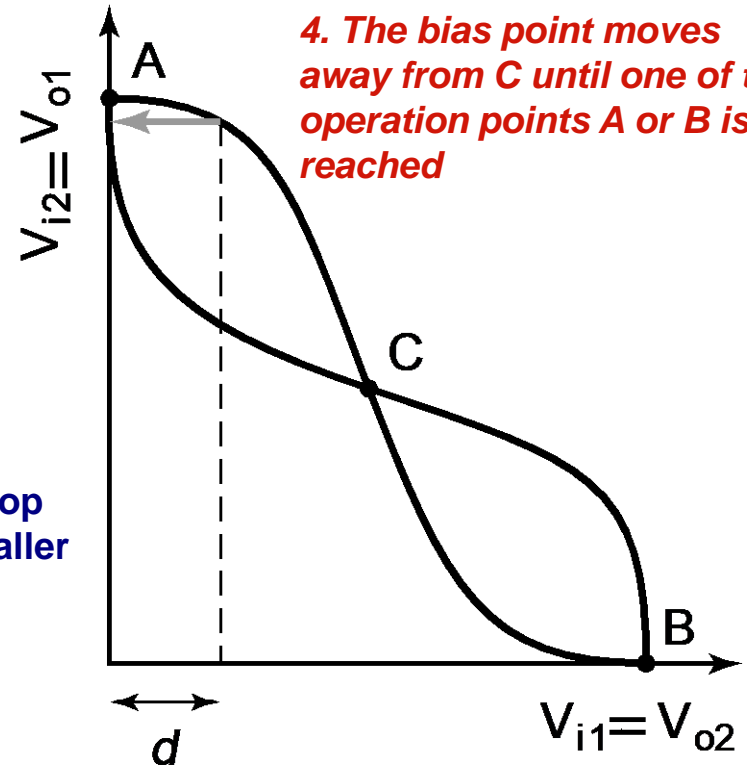
Point C is the V_M of the Inverters…

Kaustav Banerjee

Meta-Stability in Bi-Stable Circuits

Point C is the V_M of the Inverters…

3. Deviation is amplified by the gain of the first inverter and then further amplified by the second inverter

A: $V_{i1}=0$, $V_{i2}=1$

4. The bias point moves away from C until one of the operation points A or B is reached

1. Apply small deviation d to V_{i1} biased at C

2. Deviation gets amplified and regenerated around the circuit loop
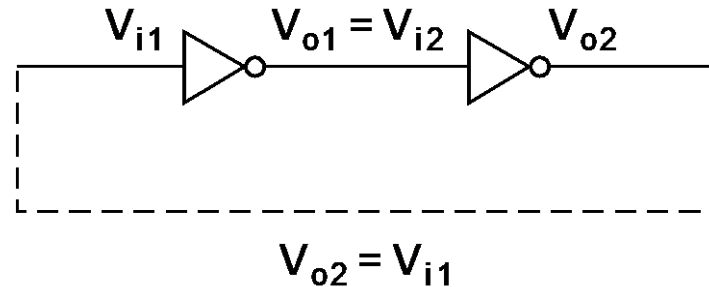
At A and B the loop gain is much smaller than 1…hence, stable points

- **Gain is larger than 1 in the transition region**
- **Every small deviation causes the operation point to move away from its original bias point, C ---therefore metastable**
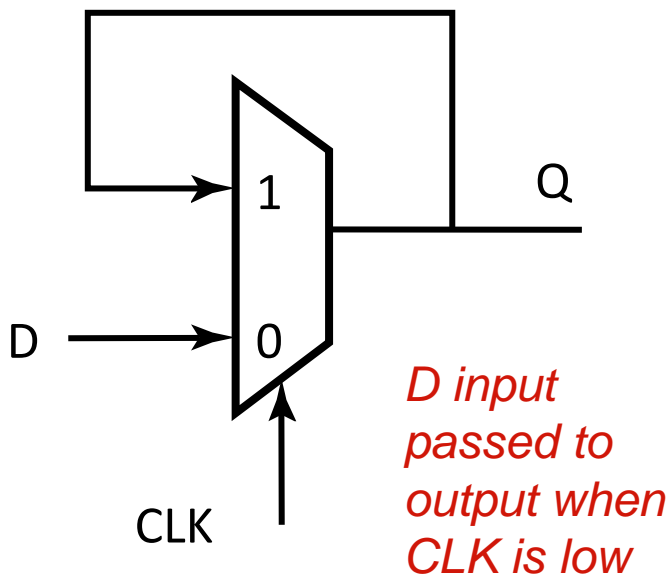
Kaustav Banerjee

Flip-Flop

A cross coupled pair of inverters results in a bistable circuit…

$$V_{i1} \quad \to \quad V_{o1} = V_{i2} \quad \to \quad V_{o2}$$

$$V_{o2} = V_{i1}$$

- ❑ A FF is a bistable circuit, which has 2 stable states
- ❑ In the absence of triggering the circuit remains in a single state
- ❑ The state can be changed by applying an external trigger
- ❑ Two ways to achieve a change of state:
    - ▪ Cut the feedback loop: so that a new value can be written into **out** or **Q**
        - – **This is MUX based: Q=$\overline{\text{CLK}}$. Q + CLK . In (most common)**
    - ▪ Overpower the feedback loop
        - – Apply a trigger signal at the input of the FF and force the new value into the cell by overpowering the stored value
        - – Needs careful sizing of transistors in the feedback loop and the trigger circuit
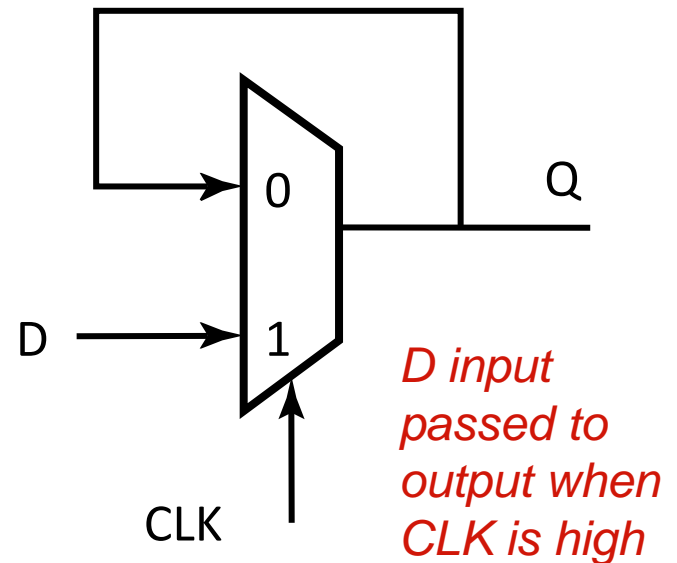   - – Used mostly in static background memories

Mux-Based Latches

Negative latch
(transparent when CLK= 0)

Positive latch
(transparent when CLK= 1)

Q

D

1

0

CLK

D input passed to output when CLK is low

Q

D

0

1

CLK

D input passed to output when CLK is high

$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Kaustav Banerjee

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

+ve Latch

MUX based (not so efficient….# of transistors driven by CLK is high= 4)
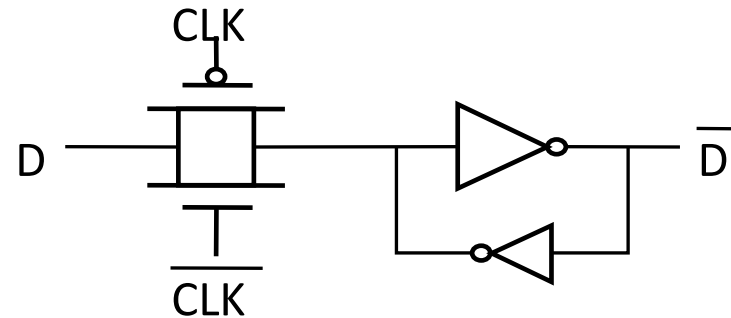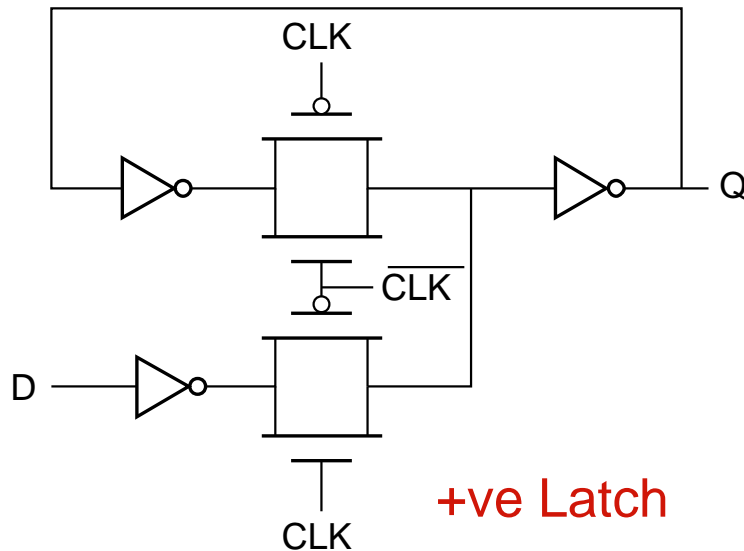
Forcing the state
(can implement as NMOS-only)

Kaustav Banerjee

Mux-Based Latch

CLK

CLK=0: top gate is on and Q is held stable

bottom gate is off

Q

$\overline{CLK}$

CLK=1: bottom gate is on and D is copied to Q

D

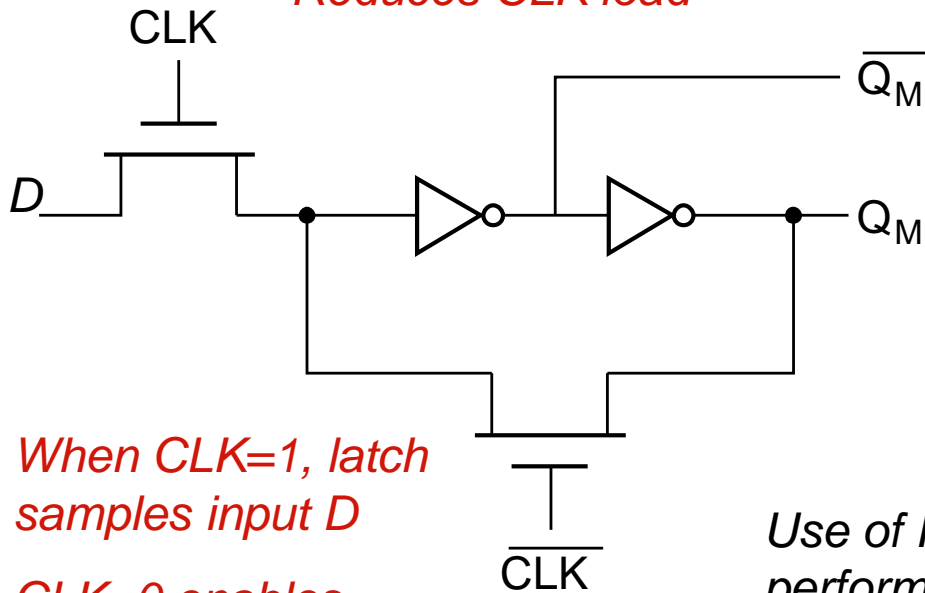*Top gate is off: no feedback*

CLK
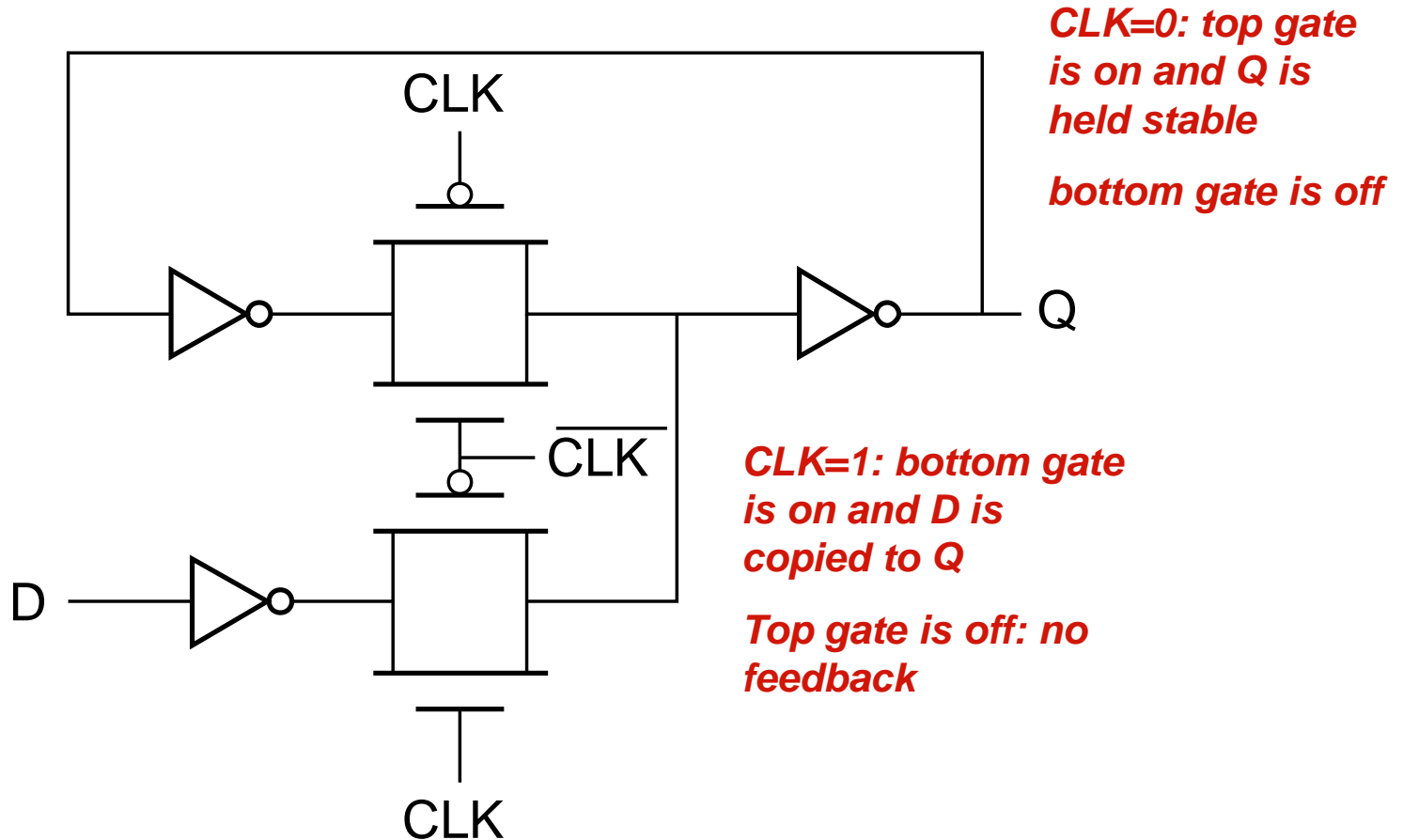
CLK is driving several transistors with activity=1 (not good from power perspective!)

Kaustav Banerjee

Mux-Based Latch with Reduced Load
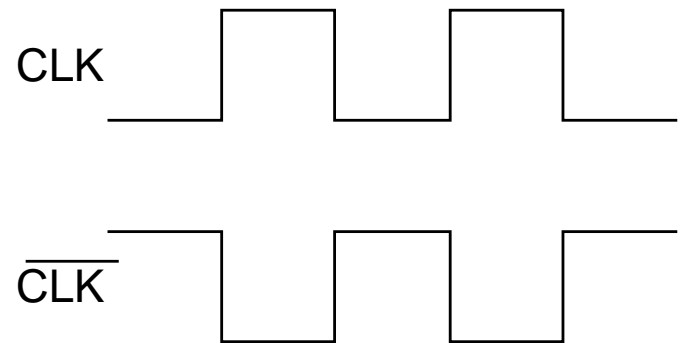
NMOS only Pass Transistor

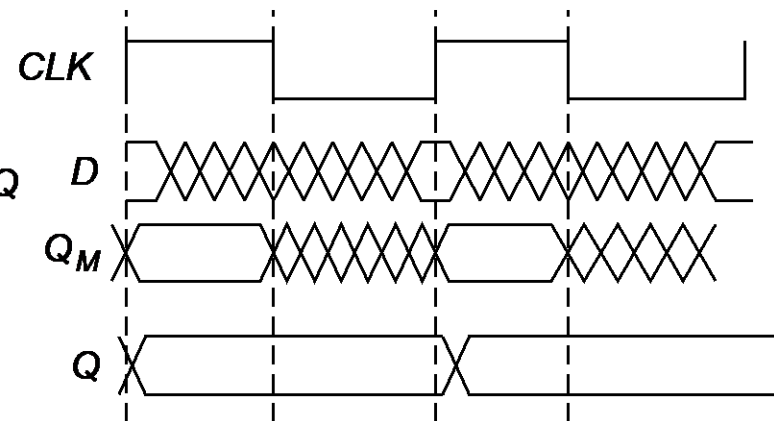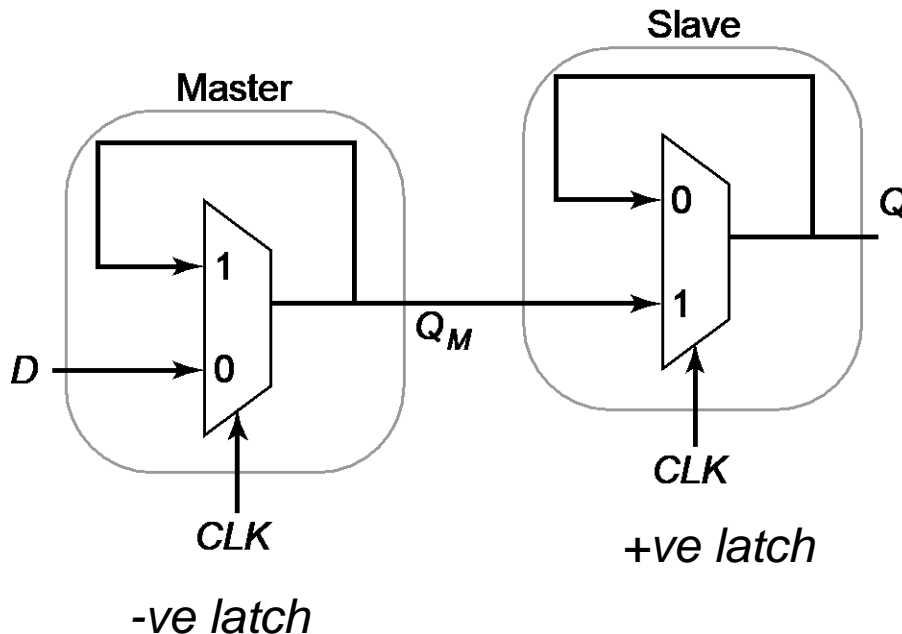Need Non-overlapping clocks

Reduces CLK load

When CLK=1, latch samples input D

CLK=0 enables feedback loop, puts latch in hold mode

Use of PT degrades NM and switching performance by passing V_{dd}-V_{Tn} to the input of first inverter + increases static power (PMOS of inverter is never fully turned off)

Master-Slave (Edge-Triggered) Register

CLK=0: master is transparent and D is copied to QM

During this time slave is in hold mode

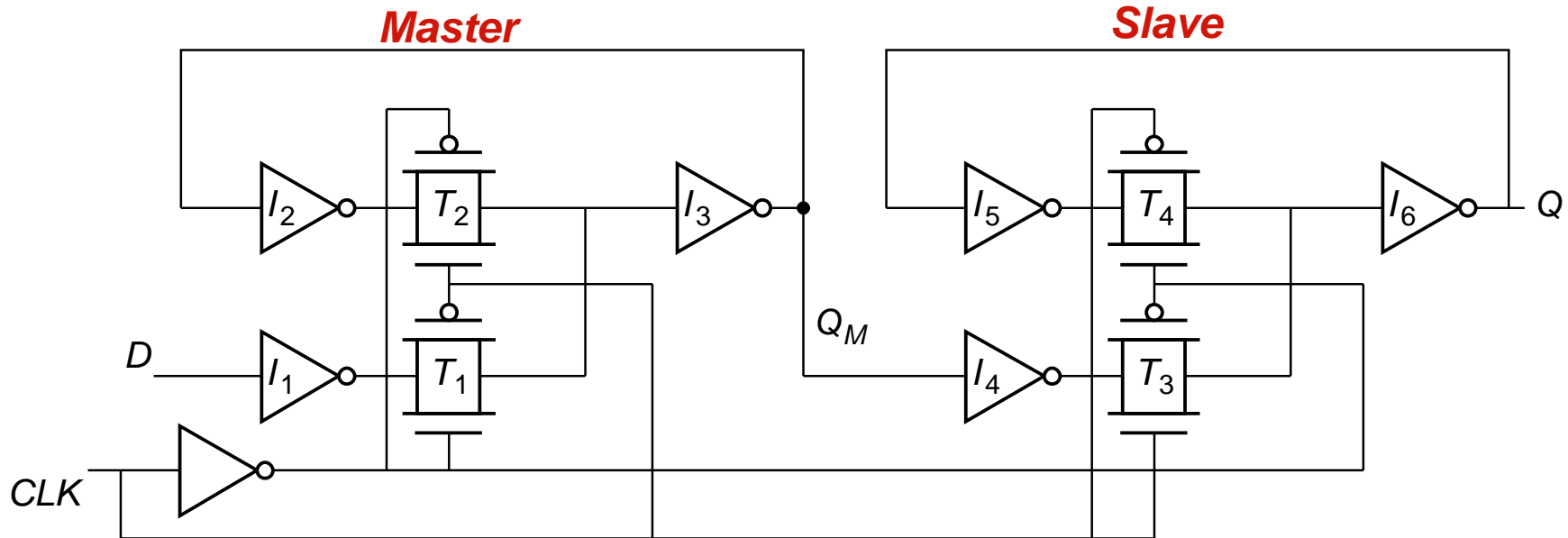**As CLK=1: slave starts sampling, master in hold mode**

Value of Q=Value of D right before the rising edge of the CLK: +ve edge triggered effect

Two opposite latches trigger on edge
Also called master-slave latch pair

Kaustav Banerjee

Master-Slave +ve Edge Triggered Register

Transistor Level Implementation

X-gate Multiplexer-based latch pair
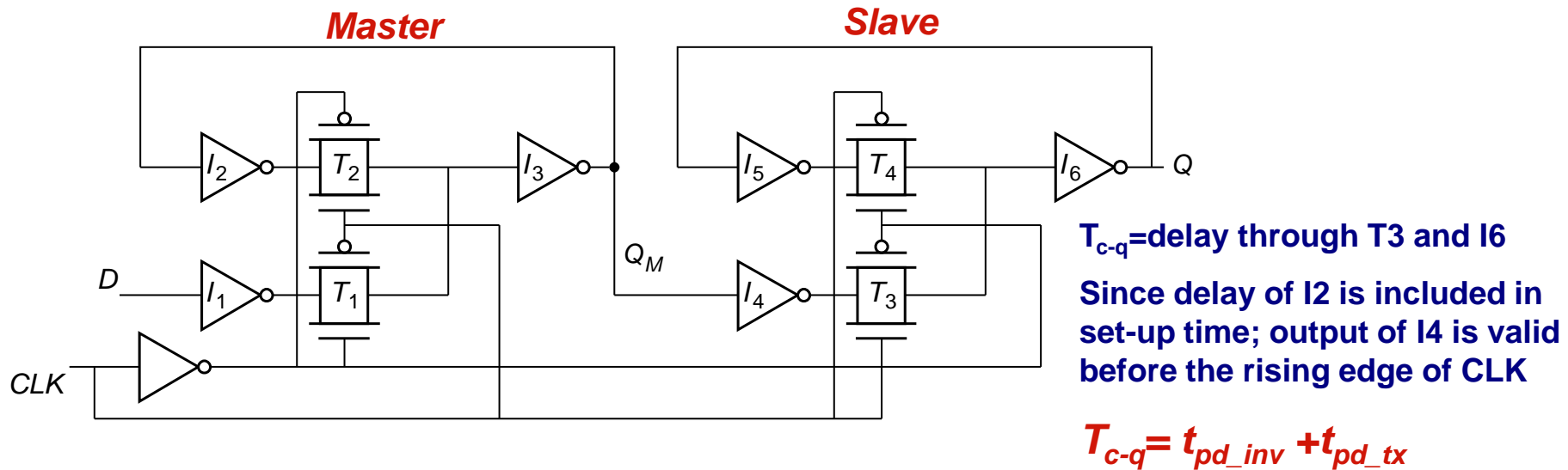

CLK=0: T1 is on, T2 is off, D input sampled onto QM

T3 off and T4 on: I5 and I6 hold the state of the Slave

CLK=1: T3 is on, T4 is off, QM sampled onto Q

T2 on and T1 off: I2 and I3 hold the state of QM

Kaustav Banerjee

Master-Slave +ve Edge Triggered Register

Transistor Level Implementation

Master

Slave

I_2 T_2 I_3

D I_1 T_1

CLK

Q_M

I_4 T_3

I_5 T_4 I_6 Q

T_{c-q}=delay through T3 and I6

Since delay of I2 is included in set-up time; output of I4 is valid before the rising edge of CLK

$$T_{c-q}= t_{pd\_inv} + t_{pd\_tx}$$

t_{su} = set-up time = time before the rising edge of the CLK during which the D input should remain stable so that QM samples the value reliably

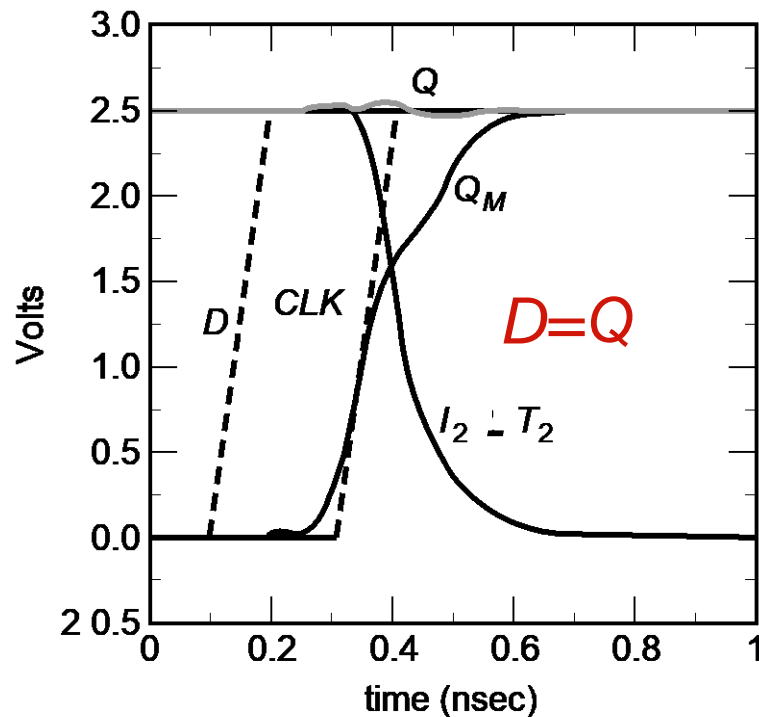**Since D must propagate through I1, T1, I3, and I2 before the rising edge**

$$t_{su}= 3t_{pd\_inv} + t_{pd\_tx}$$

t_{hold}=0 **(since T1 is cut off after CLK edge)**

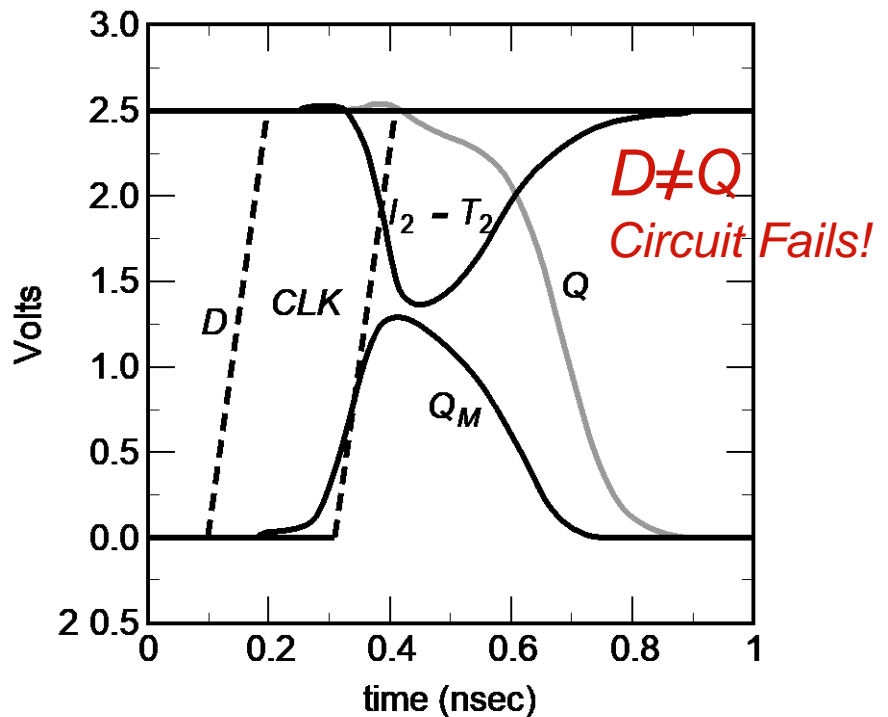*To ensure equal node voltages on both sides of the Xgate*

Kaustav Banerjee

Timing Analysis: Setup Time

SPICE Simulations: progressively skew the input w.r.t CLK edge until the circuit fails

(a) $T_{setup} = 0.21$ nsec

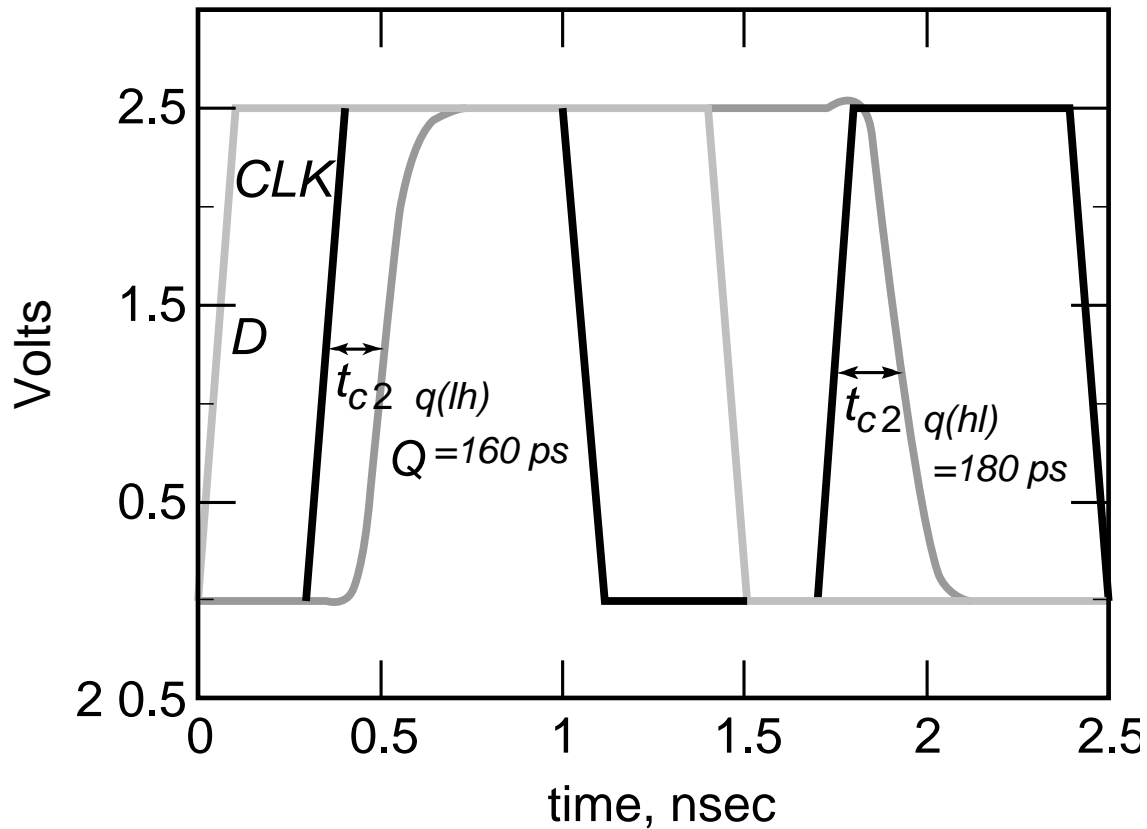(b) $T_{setup} = 0.20$ nsec

CLK is enabled before the voltage across T2 settles to the same value

Set-up time for this register = 210 ps and hold time =0

Clk-Q Delay

t_{c-q} = 50% point of CLK to 50% point of Q

Reduced Clock Load Master-Slave Register

Note: X-gate register presents high capacitive load to the CLK signal

Minimum sized devices are desired for X-gates….why? (CLk power)

However, input to I1 must be brought below its switching threshold….to make a transition. Hence, for minimum sized X-gate, I2 should be made even weaker…..by increasing L_{ch}.

**Ratioed circuit:** *provides reduced load at the cost of NM*
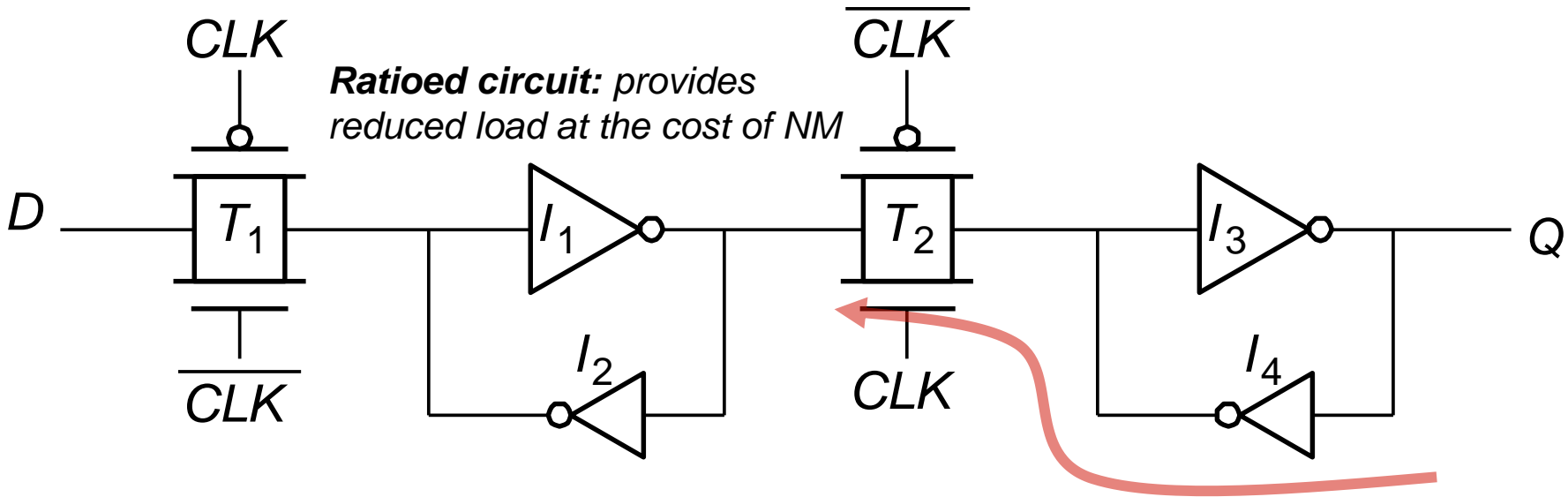
Cons: 1) T1 and its source driver must overpower I2 to switch the state of the cross-coupled inverter

2) Reverse conduction---second stage (T2 and I4) can affect the state of the first latch (I1-I2) when slave stage is ON…..not a major problem if I4 is weak.
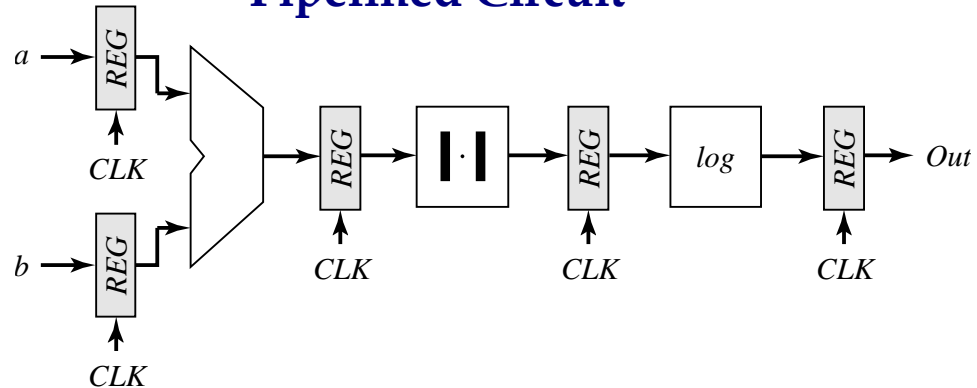
Kaustav Banerjee

Pipelining: Optimizing Sequential Circuits

Widely used to accelerate the operation of datapaths in digital microprocessors…

Reference Circuit: computes log (|a+b|)
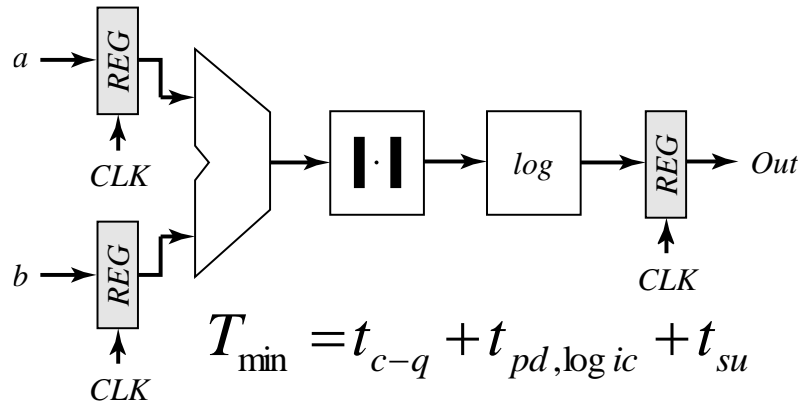
Pipelined Circuit

$$T_{\min} = t_{c-q} + t_{pd,\log ic} + t_{su}$$

$$T_{\min,\,pipe} = t_{c-q} + \max\left(t_{pd,adder} + t_{pd,abs} + t_{pd,\log}\right) + t_{su}$$

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$|a_1 + b_1|$	
3	$a_3 + b_3$	$|a_2 + b_2|$	$\log(|a_1 + b_1|)$
4	$a_4 + b_4$	$|a_3 + b_3|$	$\log(|a_2 + b_2|)$
5	$a_5 + b_5$	$|a_4 + b_4|$	$\log(|a_3 + b_3|)$

Computation of one set of input data spreads over several clock cycles.

Pipelining improves resource utilization and increases functional throughput.

Kaustav Banerjee

Register vs Latch Based Clocking...

❑ In an edge-triggered system, the worst case logic path between two registers determines the minimum CLK period for the entire system….

❑ If the logic block finishes before the end of the CLK period, it has to sit idle until the next CLK edge…

❑ Latch based design offers more flexibility…. one stage can *pass slack* or *borrow time* from other stages…

Kaustav Banerjee