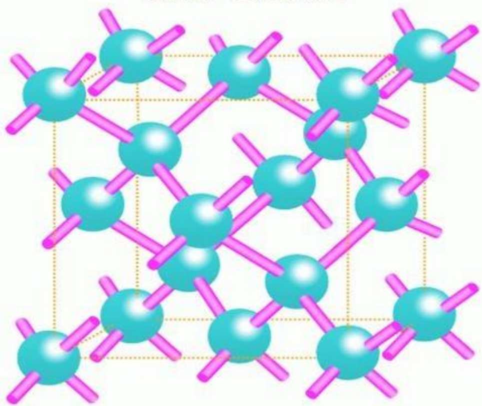

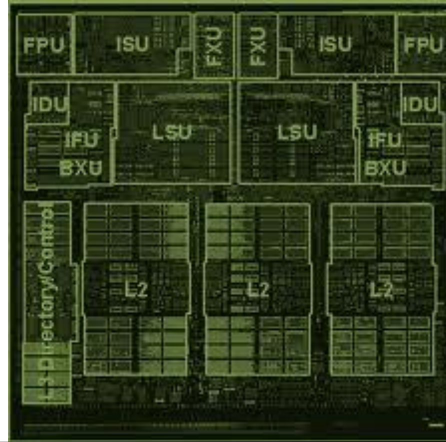

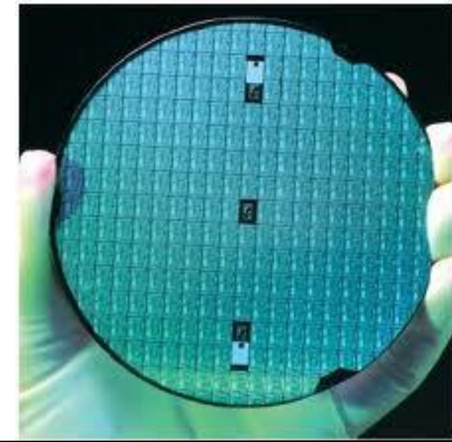

ECE 122A

VLSI Principles

Lecture 16

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University of California, Santa Barbara
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6-transistor CMOS SRAM Cell - Review

SRAM cell should be as small as possible…..but reliable operation requires careful sizing…

READ Operation:

Sizing M1-M5 & M3-M6

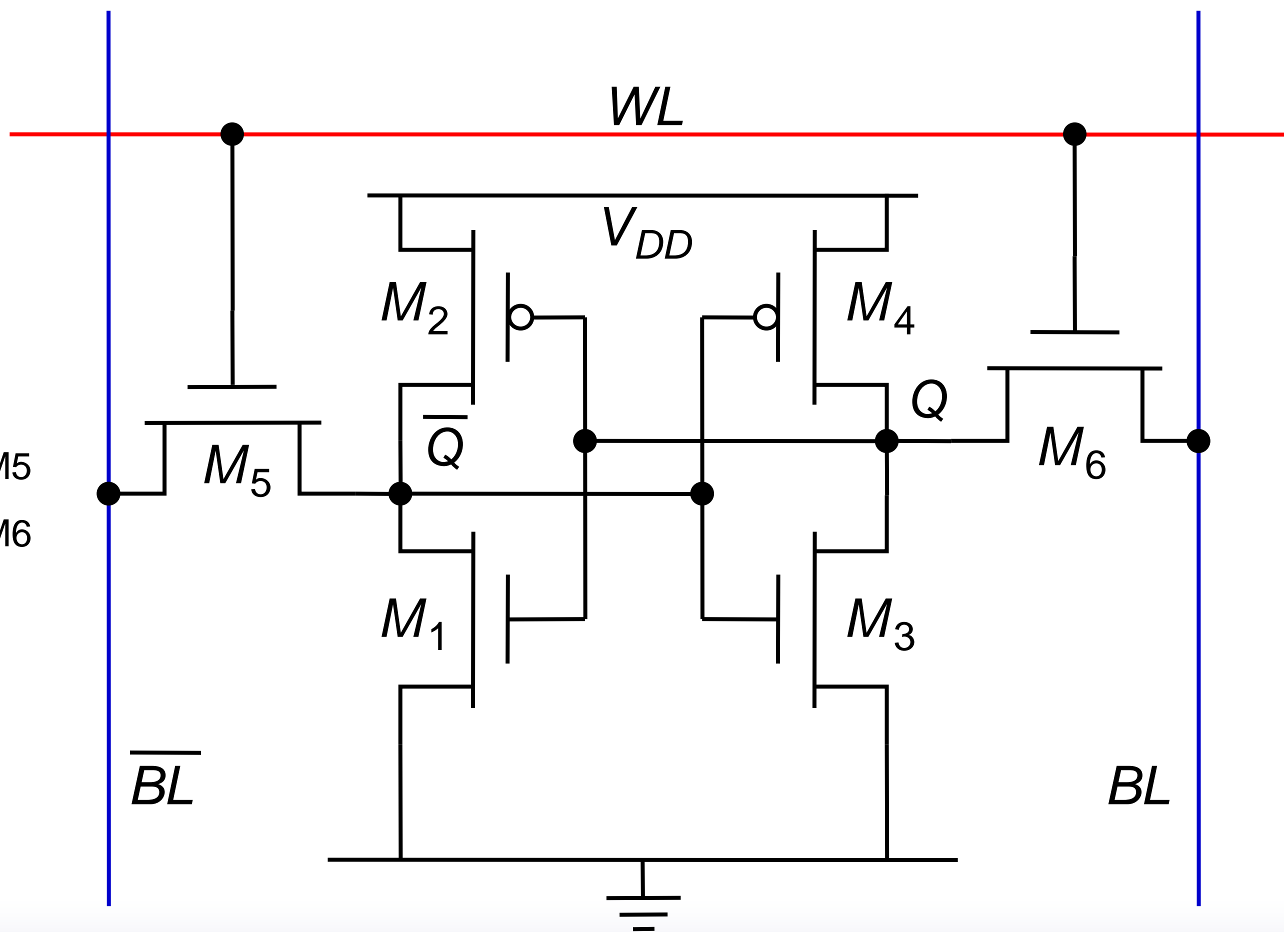
M1 slightly stronger than M5

M3 slightly stronger than M6

Write Operation:

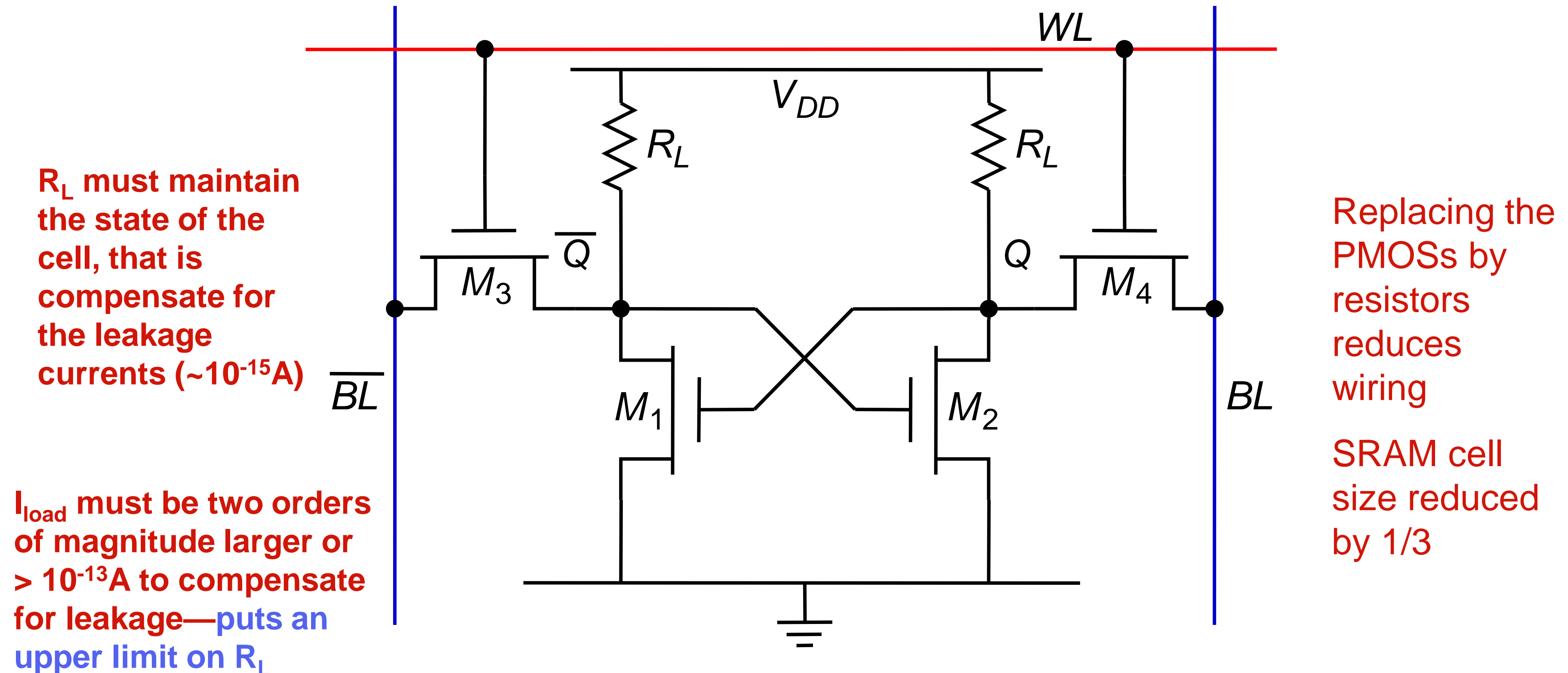
Sizing M4-M6 and M2-M5

M4-to-M6 (and M2-to-M5) Pull-up ratio < 1.8



Resistive-load (4T) SRAM Cell

Reduce area using resistive load inverters…simplifies writing



Static power dissipation -- Want R_L large (use undoped poly)
Bit lines precharged to V_{DD} to address t_p problem

SRAM Characteristics

Instead of PMOS devices, use parasitic devices on top of cell structure using thin-film transistors (TFTs)

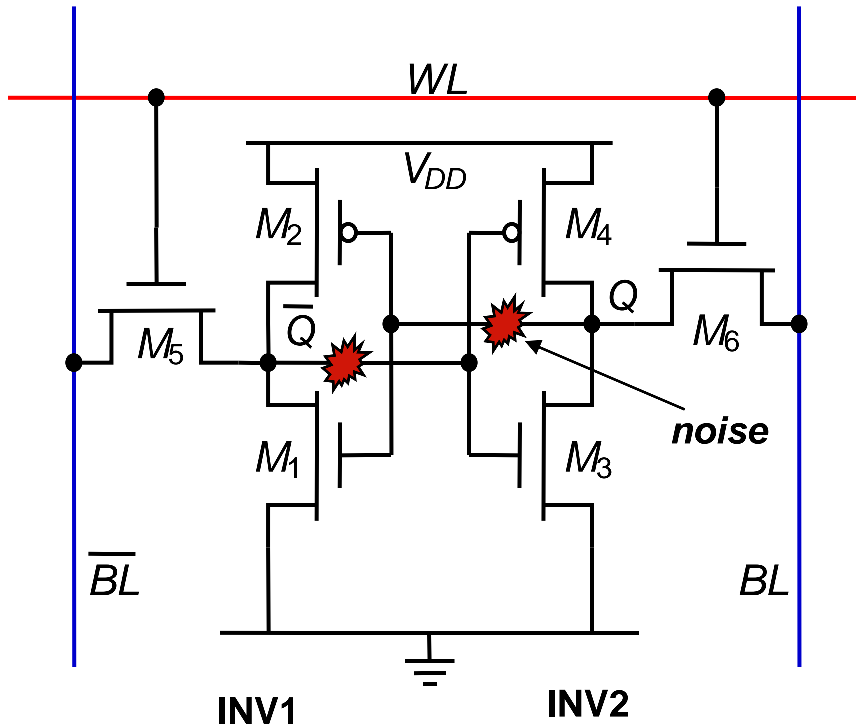
Table 12-2 Comparison of CMOS SRAM cells used in 1-Mbit memory (from [Takada91])

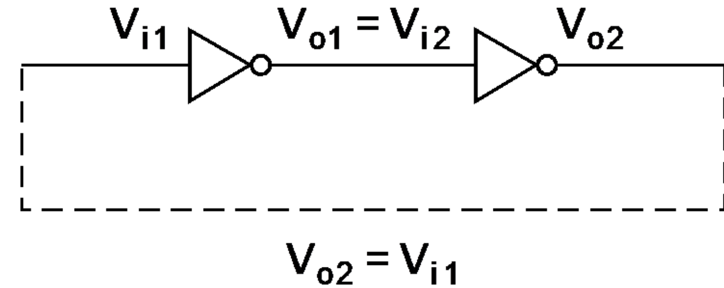
	Complementary CMOS	**Resistive Load**	**TFT Cell**
Number of transistors	6	4	4 (+2 TFT)
Cell size	58.2 μm^2 (0.7-μm rule)	40.8 μm^2 (0.7-μm rule)	41.1 μm^2 (0.8-μm rule)
Standby current (per cell)	10^{-15} A	10^{-12} A	10^{-13} A

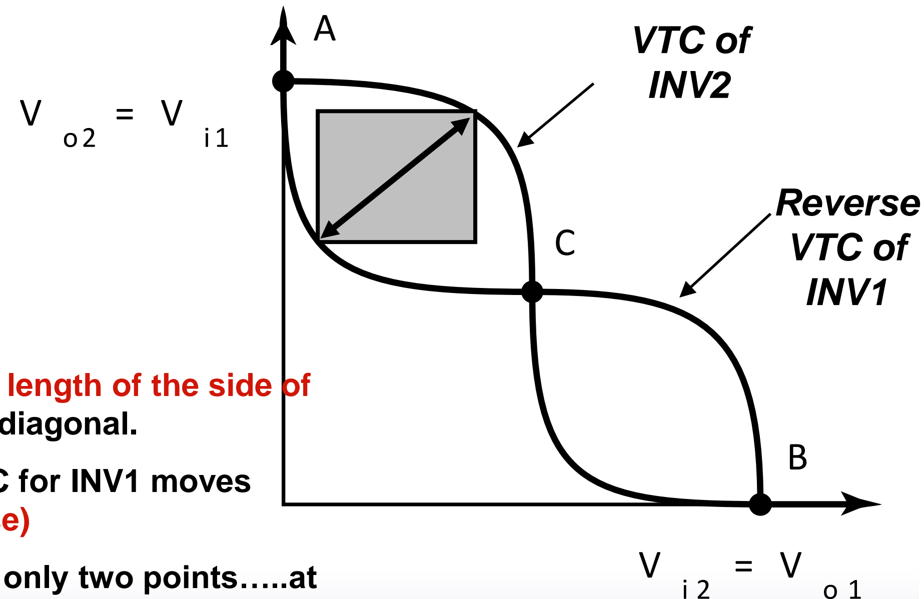
Use high Vt

However, embedded SRAM cells---used in microprocessor caches, employ 6T cells.

6-T CMOS SRAM Cell: Static Noise Margin







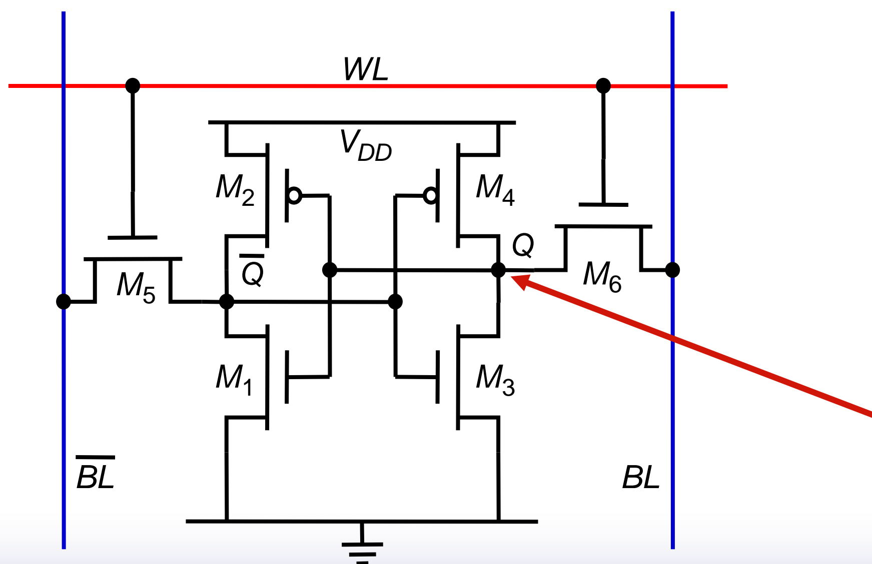
The SNM (hold margin) can be estimated graphically by the length of the side of the square fitted between the VTCs and having the longest diagonal.

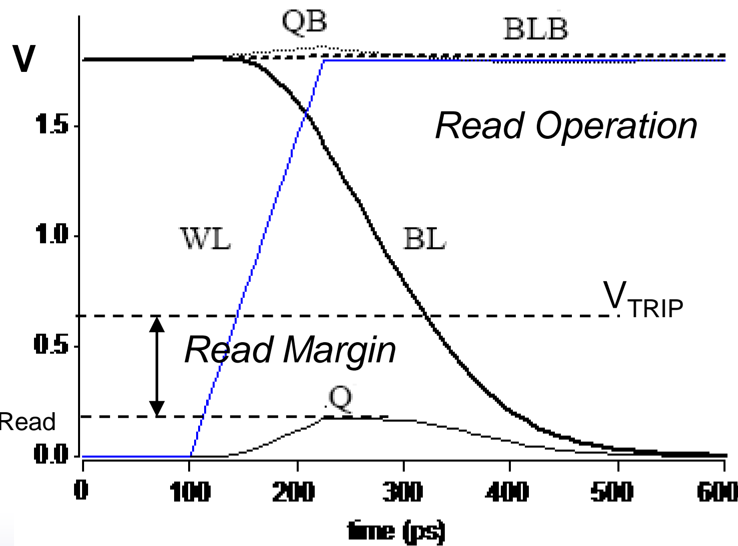
As noise increases at the two nodes above, the reverse VTC for INV1 moves upward, while the VTC for INV2 moves to the left (worst case)

Once they both move by the SNM value, the curves meet at only two points…..at A' and B'…… and any further noise flips the data.

Static Noise Margin (SNM)

- **Hold Margin:** How strongly the node storing ‘1’ and the node storing ‘0’ are coupled to V_{DD} and V_{SS} respectively.
- **Read Margin:** The difference between V_{TRIP} and V_{READ} (max. voltage at Q)
- **Write Margin***:* The maximum voltage on a bit-line (above “0”) that allows writing to the cell, while the other bit-line is at V_{DD}. (not determined by the butterfly curve)

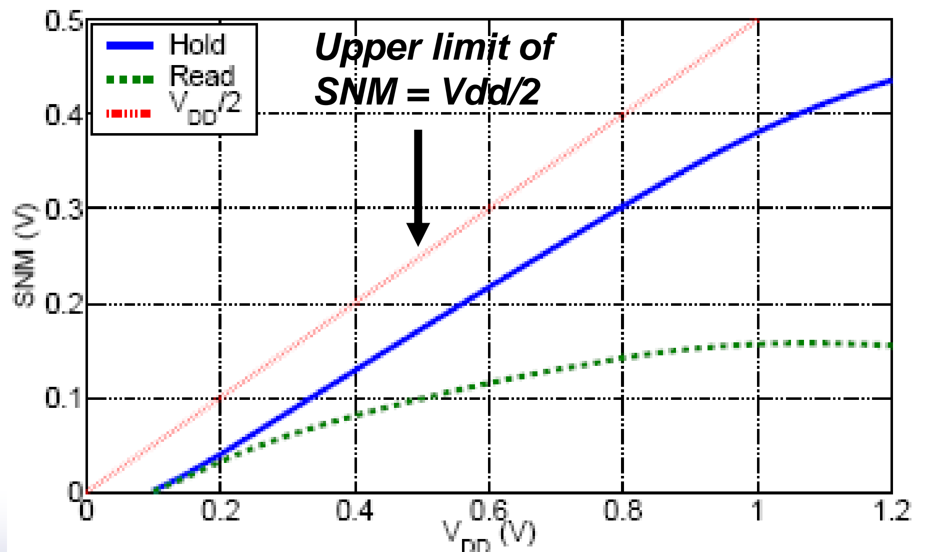




SNM Dependencies

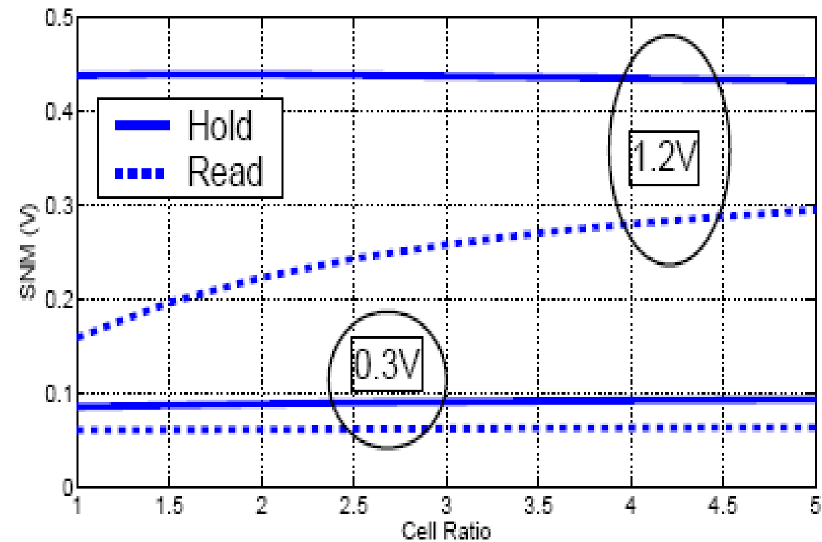
- Dependence on V_{dd} : SNM for a bitcell with ideal VTCs is still limited to Vdd/2. Any noise > Vdd/2 will flip the inverters.

Read margin increases with Vdd since Vtrip (=Vdd/2) increases…



- Dependence on sizing

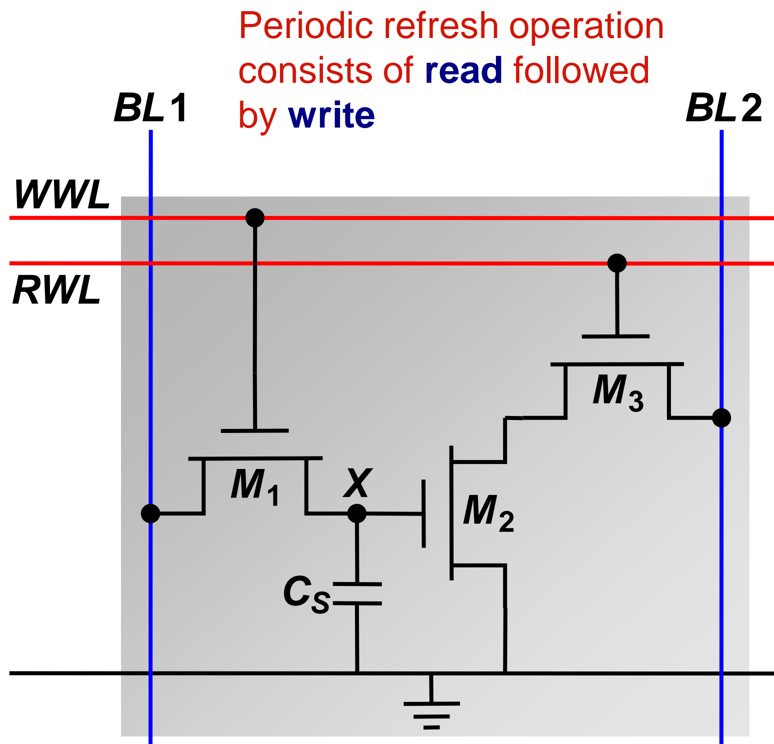
Here, Cell ratio = size of PD device over size of access device



Read-SNM increases with cell ratio (increasing Pull-down device) since bigger PD device reduces the V_Q

At very small Vdd, the PU device is not fully off

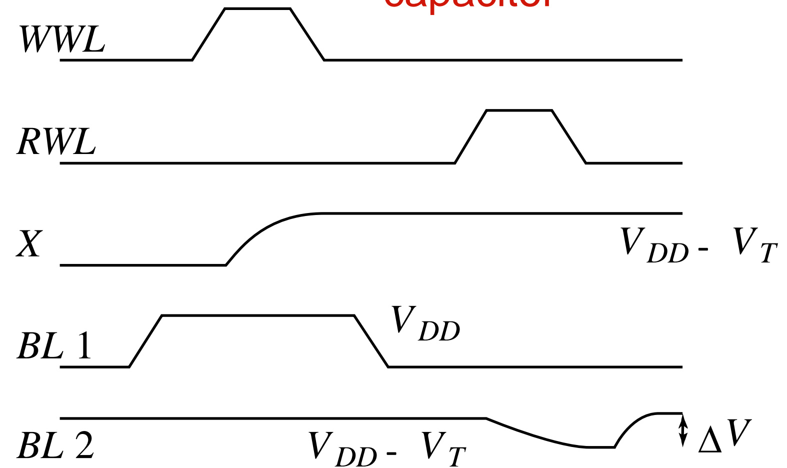
3-Transistor DRAM Cell (Early Days)



1 Kbit memory: Intel

Still used in some ASICs

Dynamic: since it involves charge storage on a capacitor



Cell is written by placing value on BL1 and asserting Write Word Line (WWL=1)

Data retained as charge stored on Cs once WWL=0

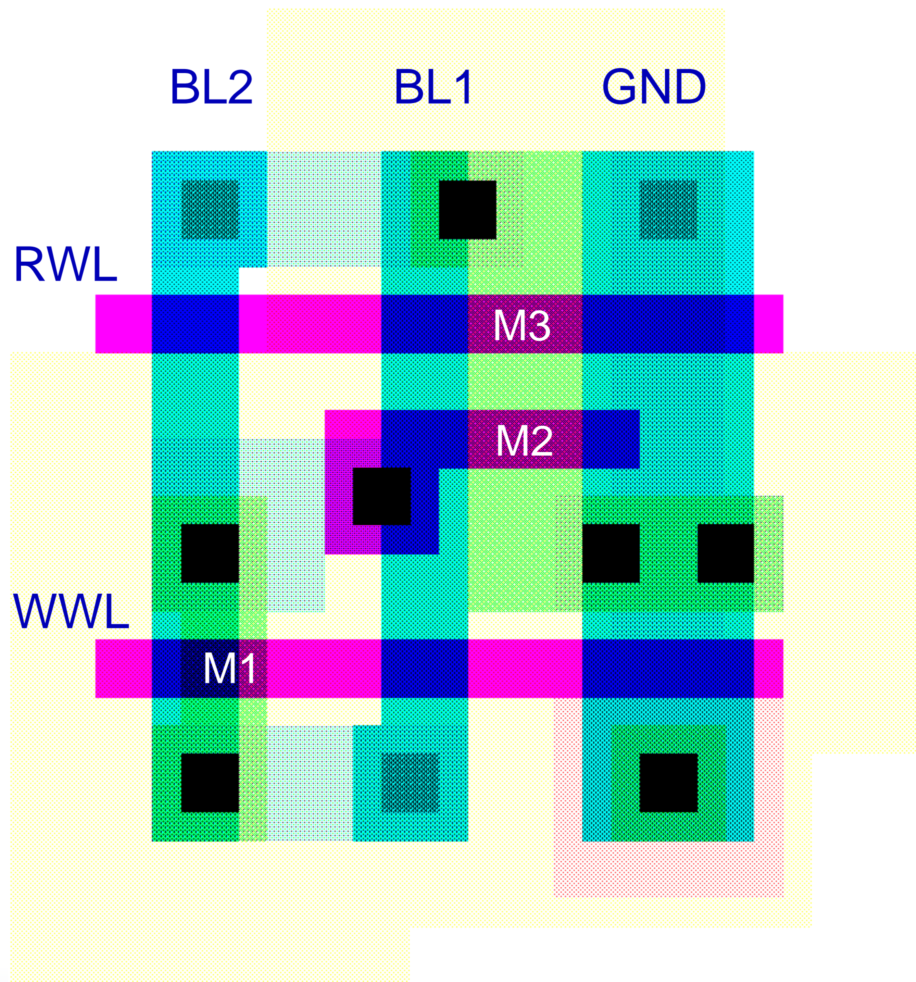
For reading the cell, RWL=1

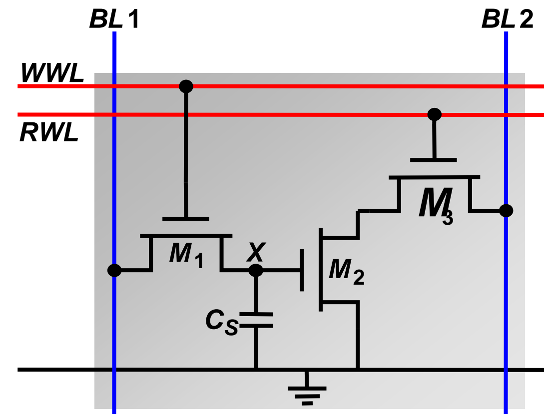
M2 can be on or off depending on stored value

BL2 is either clamped to Vdd or is precharged to either Vdd or Vdd-Vt

M2-M3 pulls BL2 low when X=1, otherwise BL2 remains high (cell is inverting: senses the inverse value of the stored signal)

3T-DRAM — Layout





Unlike SRAM, no constraint on device sizes

Read operation is non-destructive

No special process steps needed

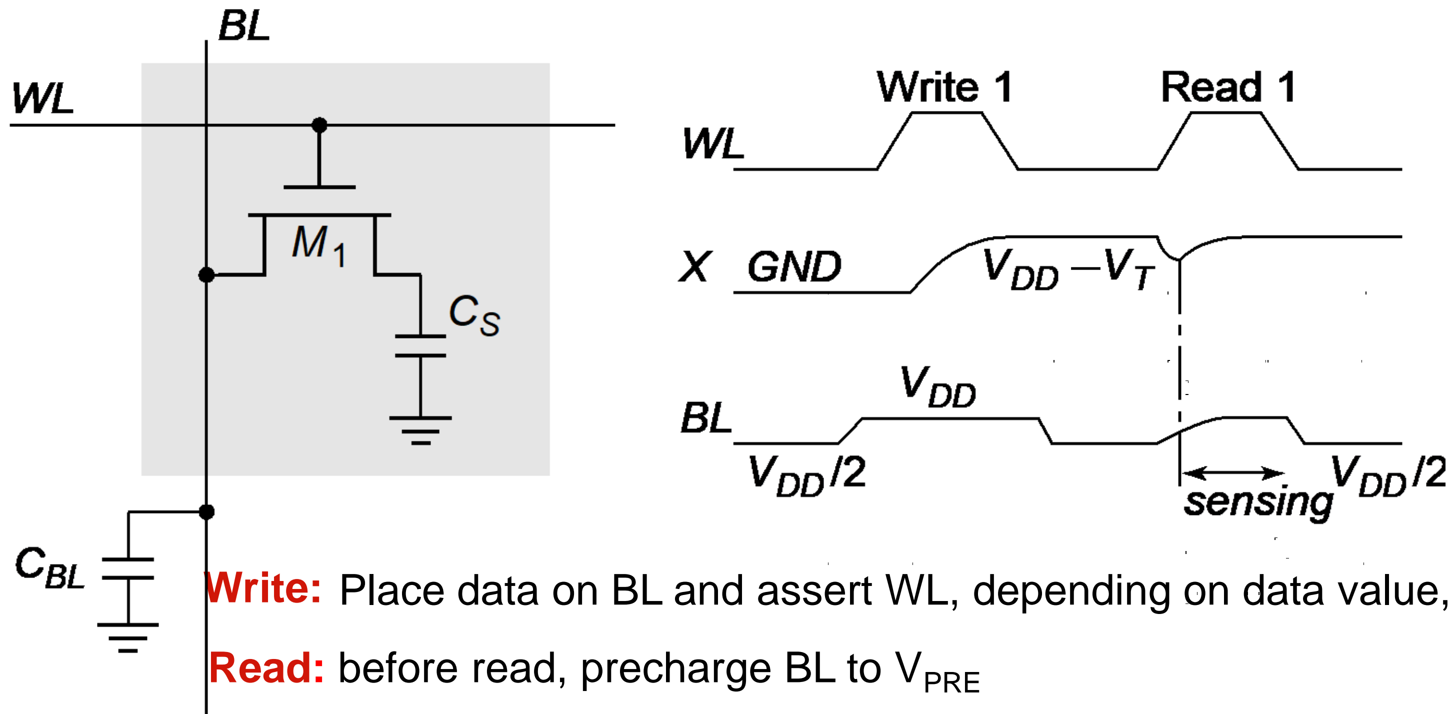
Value at node X = V_{WWL} - V_{tn}

This reduces the current through M2 during read operation and increases read access time: can use a higher value of V_{WWL} to avoid this

Kaustav Banerjee

1-Transistor DRAM Cell

Most pervasive in commercial memory design



Write: Place data on BL and assert WL, depending on data value, Cs is 1 or 0

Read: before read, precharge BL to V_{PRE}

After WL=1, charge redistribution takes places between bit line and storage capacitance resulting in a voltage change on BL

$$\Delta V = V_{BL} - V_{PRE} = (V_{BIT} - V_{PRE}) \frac{C_S}{C_S + C_{BL}}$$

← Charge transfer ratio (1-10%)

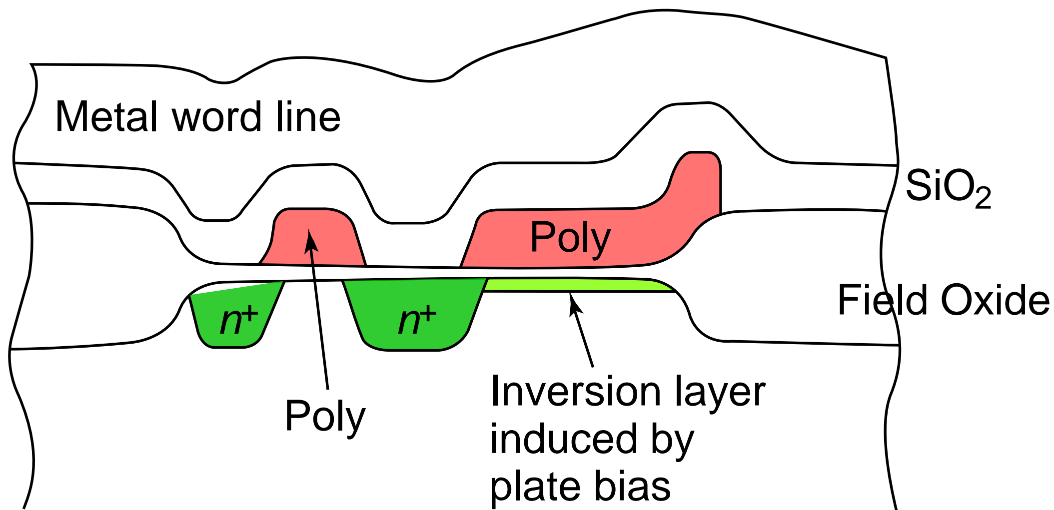
V_{BIT} is initial voltage on C_s. V_{BL} is final voltage on BL after charge redistribution. Voltage swing is small since $C_s \ll C_{BL}$; typically around 250 mV.

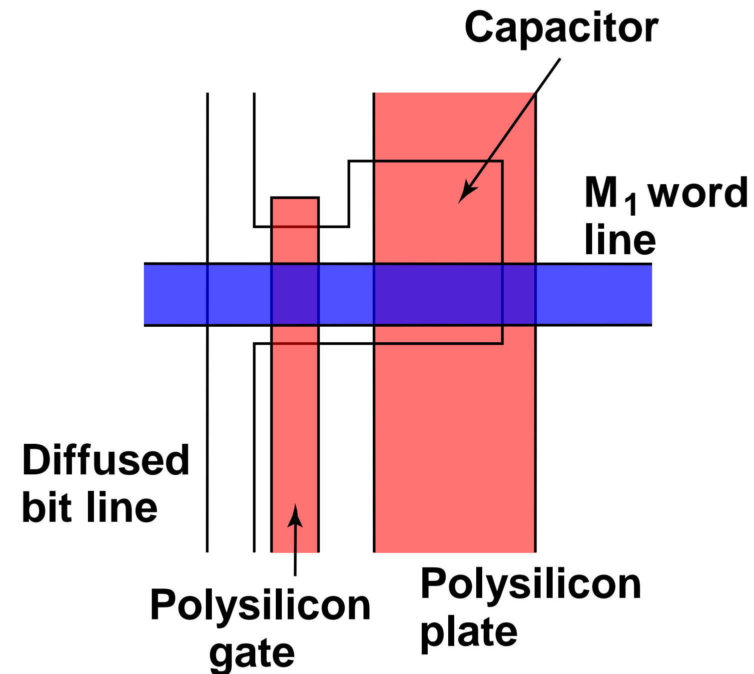
***Note:** From charge conservation, $C_S V_{BIT} + C_{BL} V_{PRE} = (C_S + C_{BL}) V_{final}$, and V_{final} (= $\mathbf{V_{BL}}$)*

DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

1-T DRAM Cell





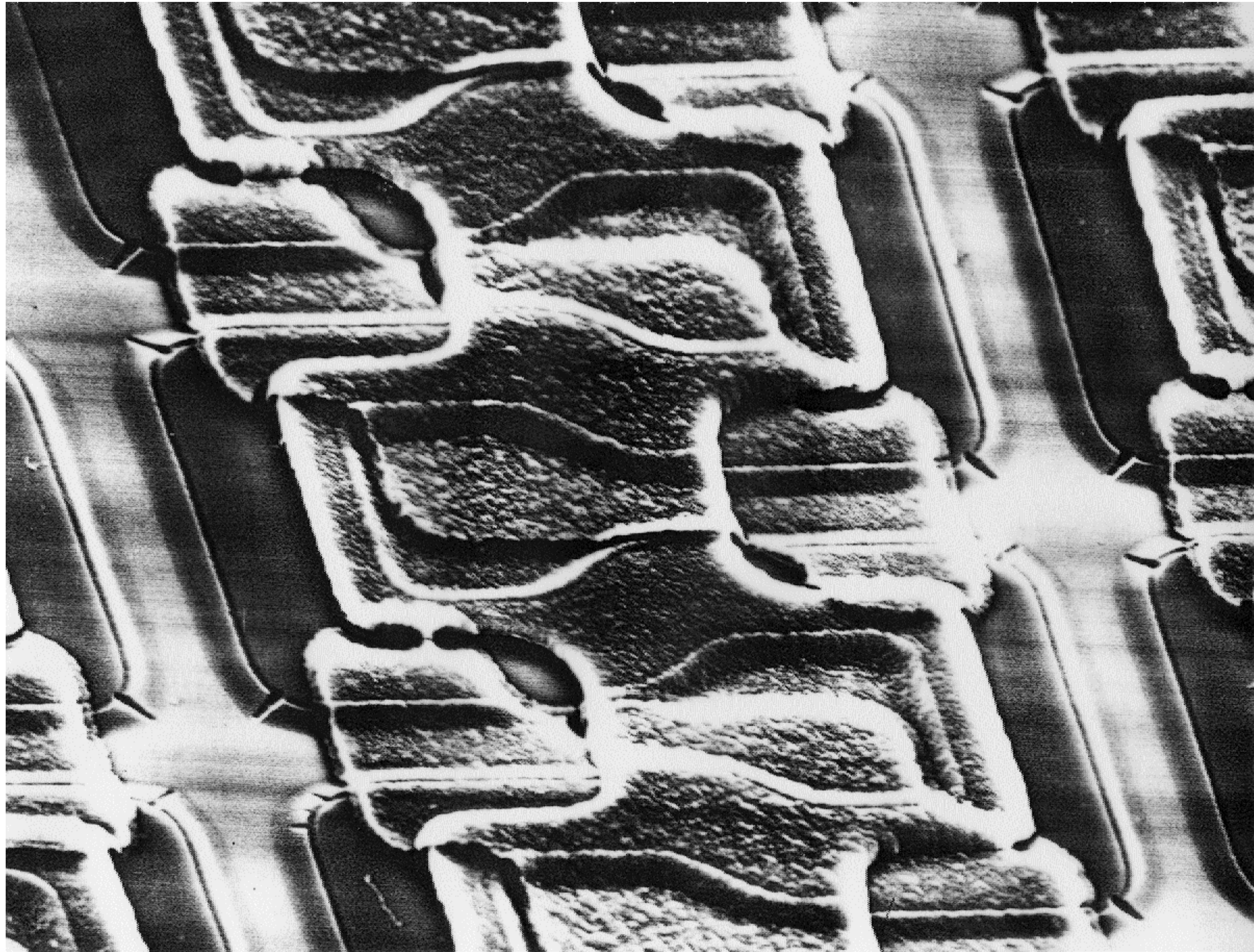
Cross-section

Layout

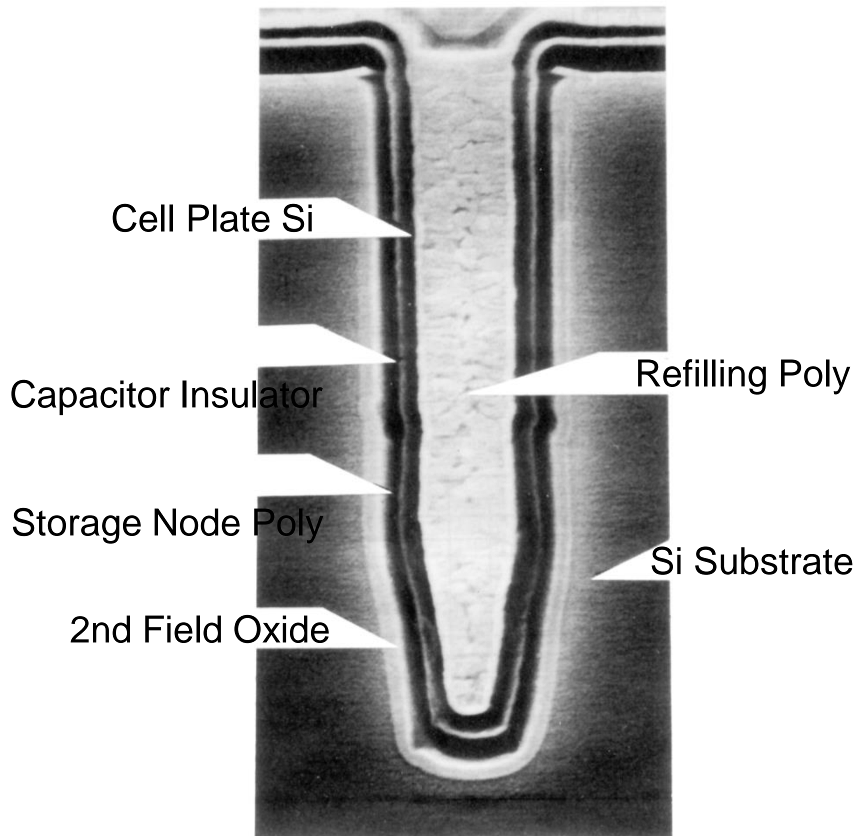
Uses Polysilicon-Diffusion Capacitance

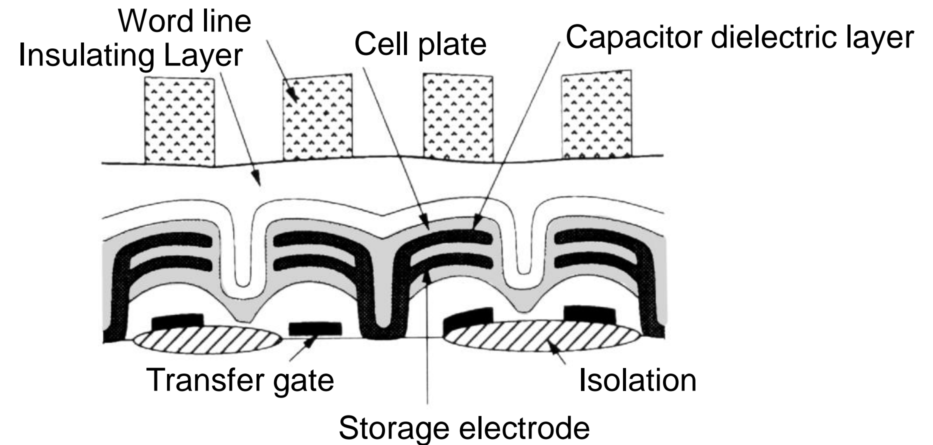
Expensive in Area

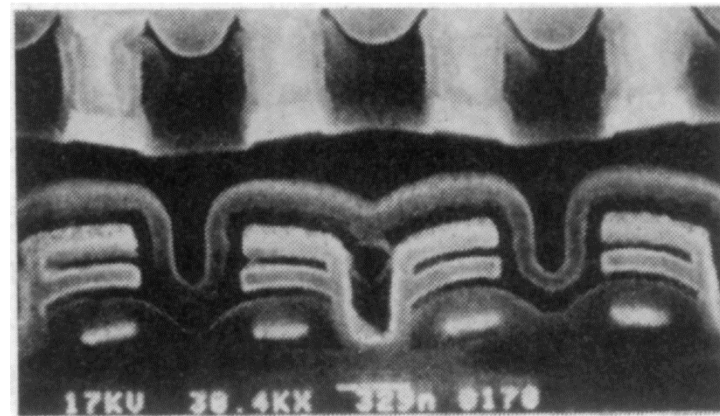
SEM of poly-diffusion capacitor 1T-DRAM



Advanced 1T DRAM Cells







Trench Cell

Stacked-capacitor Cell

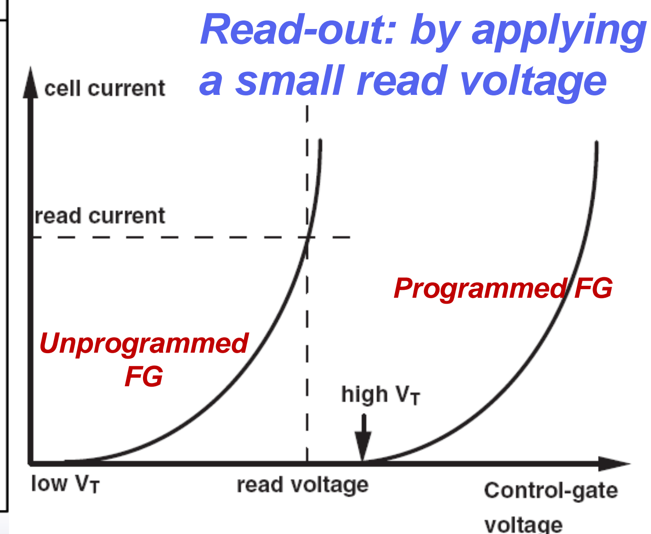
Non-Volatile Memory

Flash Memory (with Floating Gate (FG) Transistor)

	NAND	NOR
Programming	Vg (>8 V) CG COX FG TOX Channel Source Drain Tunneling Substrate	Vg (>8 V) CG COX FG Vd (>4 V) TOX Channel Source Drain Hot Carrier Injection Substrate
Erasing	Vg (<-8 V) CG COX FG TOX Channel Source Drain Tunneling Substrate	Vg (<-8 V) CG COX FG TOX Channel Source Drain Tunneling Substrate

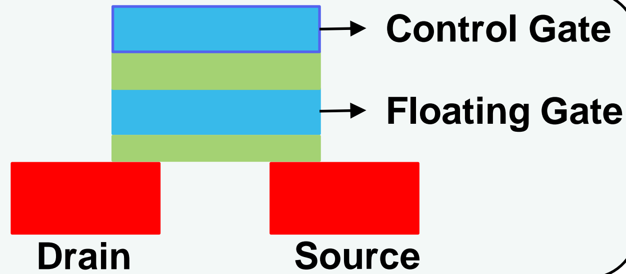
N-type device
CG: control gate
COX: control oxide
FG: floating gate
TOX: tunnel oxide

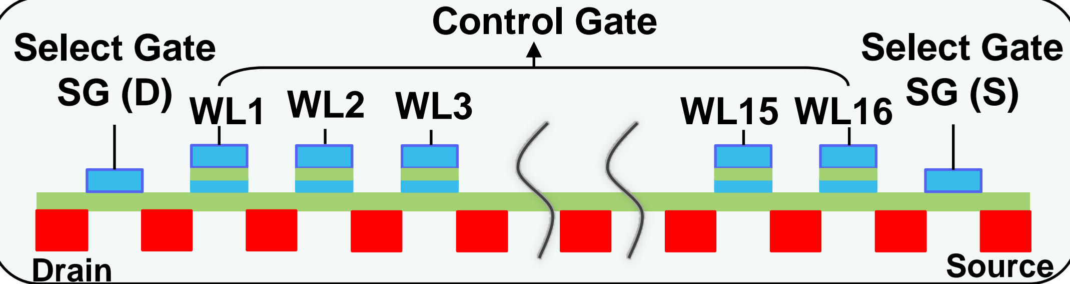
Read-out: by applying a small read voltage

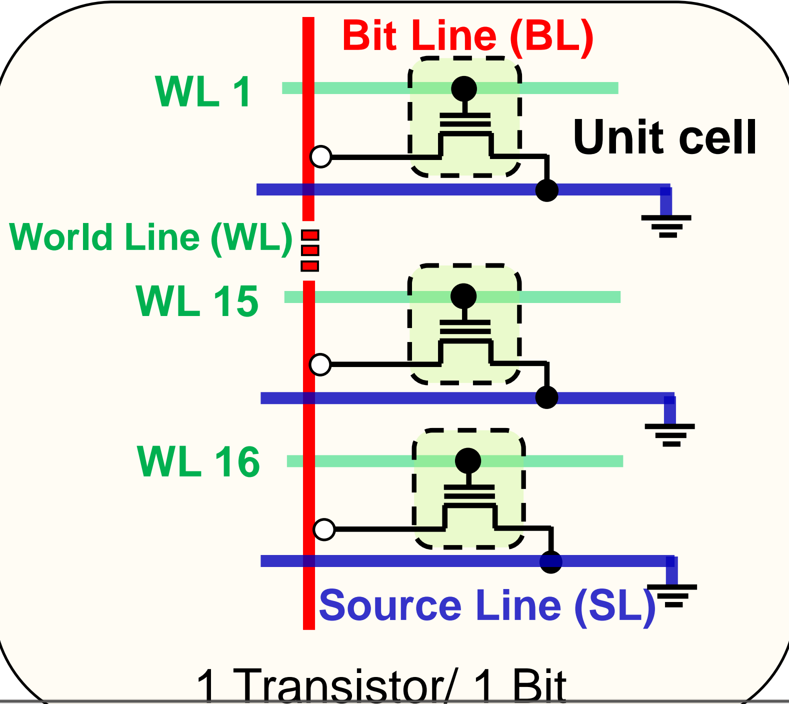


NAND vs. NOR circuit

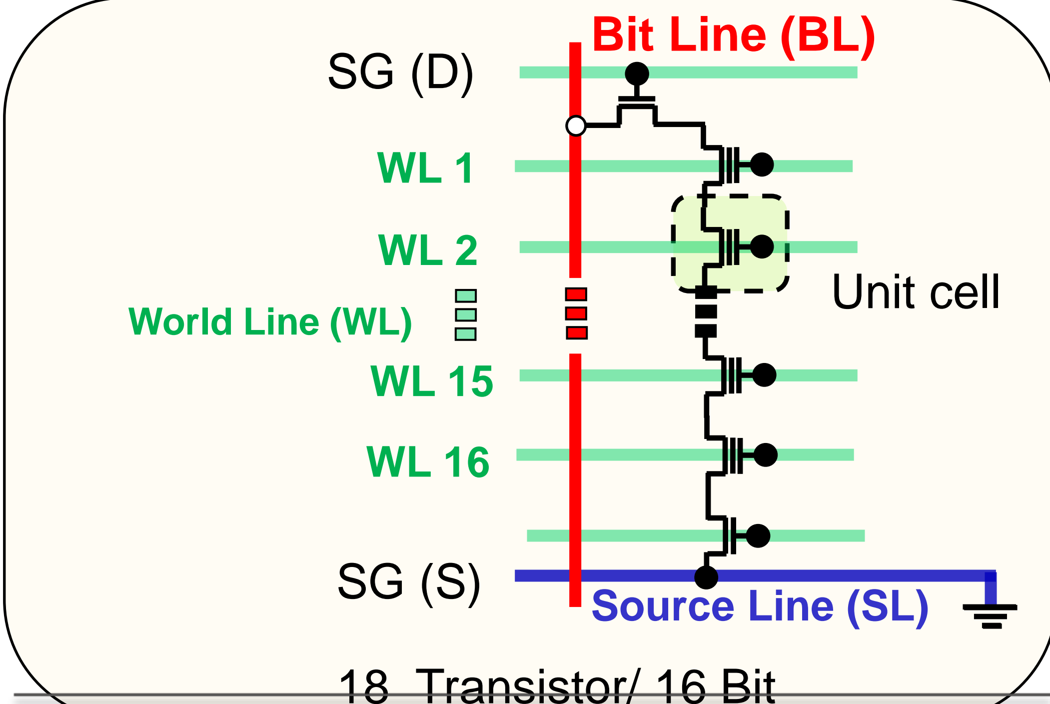
NOR-EEPROM	NAND-EEPROM







1 Transistor/ 1 Bit



18 Transistor/ 16 Bit

Devices can be Randomly accessed

Both SG devices needed for read out

NOR: It's available for random access

NAND: It's allowed to access one bit only per readout operation

NAND vs. NOR

Merits of NAND

★ *Multiple cells at once*

① **High speed programming** (★)
② **High speed erasing**
③ **High capacity**
④ **Low cost per bit**

Merits of NOR

① **High speed random access**
② **Bit programming**

(Individual bit cell for programming/erasing process)

Demerits of NAND

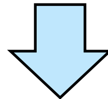
① **Slow random access**
② **Bit programming cannot be performed**
③ **Slow read operation**

(Serial access => sequential data readout)

Demerits of NOR

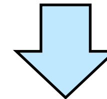
① **Slow programming**
② **Slow speed erasing**
③ **Low capacity**
④ **High cost per bit**

(NOR must be erased in large "chunks". Those chunks can often be subdivided and erased in smaller subunits resulting in a performance penalty)



- Applications -

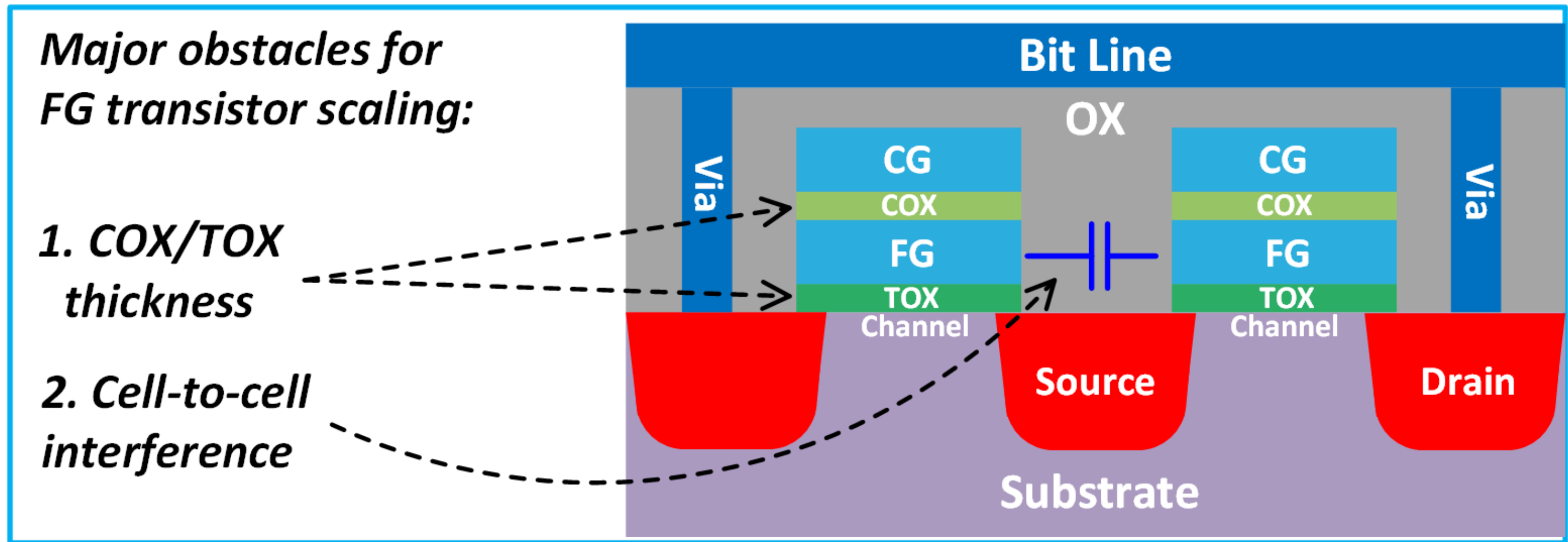
- **Suitable for Data Memory (Handy terminal, Voice recorder, DSC, Fax modem, etc)**



- Applications -

- **Suitable for replacement of EPROM**
- **Suitable for control memory (BIOS, Cellular, HDD, etc)**

Scaling issues



- ➢ thin COX/TOX -> leakage current -> short retention time
- ➢ small cell-to-cell distance -> Vth perturbation by adjacent cells

Promising solution: 2D materials….

Can 2D-Nanocrystals Extend the Lifetime of Floating-Gate Transistor Based Nonvolatile Memory?
Wei Cao, Jiahao Kang, Simone Bertolazzi, Andras Kis and Kaustav Banerjee
IEEE Transactions on Electron Devices, vol. 61, No. 10, pp.3456-3464, 2014.

3-D ICs : Multiple Active Si Layers

K. Banerjee et al., Proceedings of the IEEE, 2001

- **Advantages**
  - Reduce Interconnect Length by Vertically Stacking Multiple Si Layers
  - Reduce Chip Area, power dissipation and improve Chip Performance
  - Heterogeneous integration possible, e.g., memory, digital, analog, optical, etc. using different substrates (Si, III-V etc)