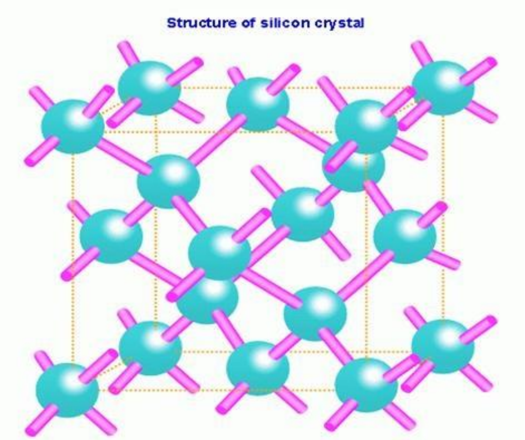

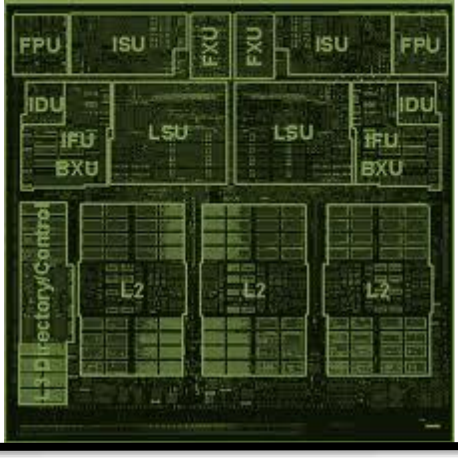

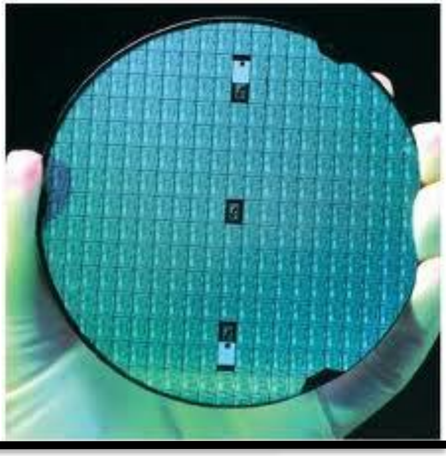

ECE 122A

VLSI Principles

Lecture 6

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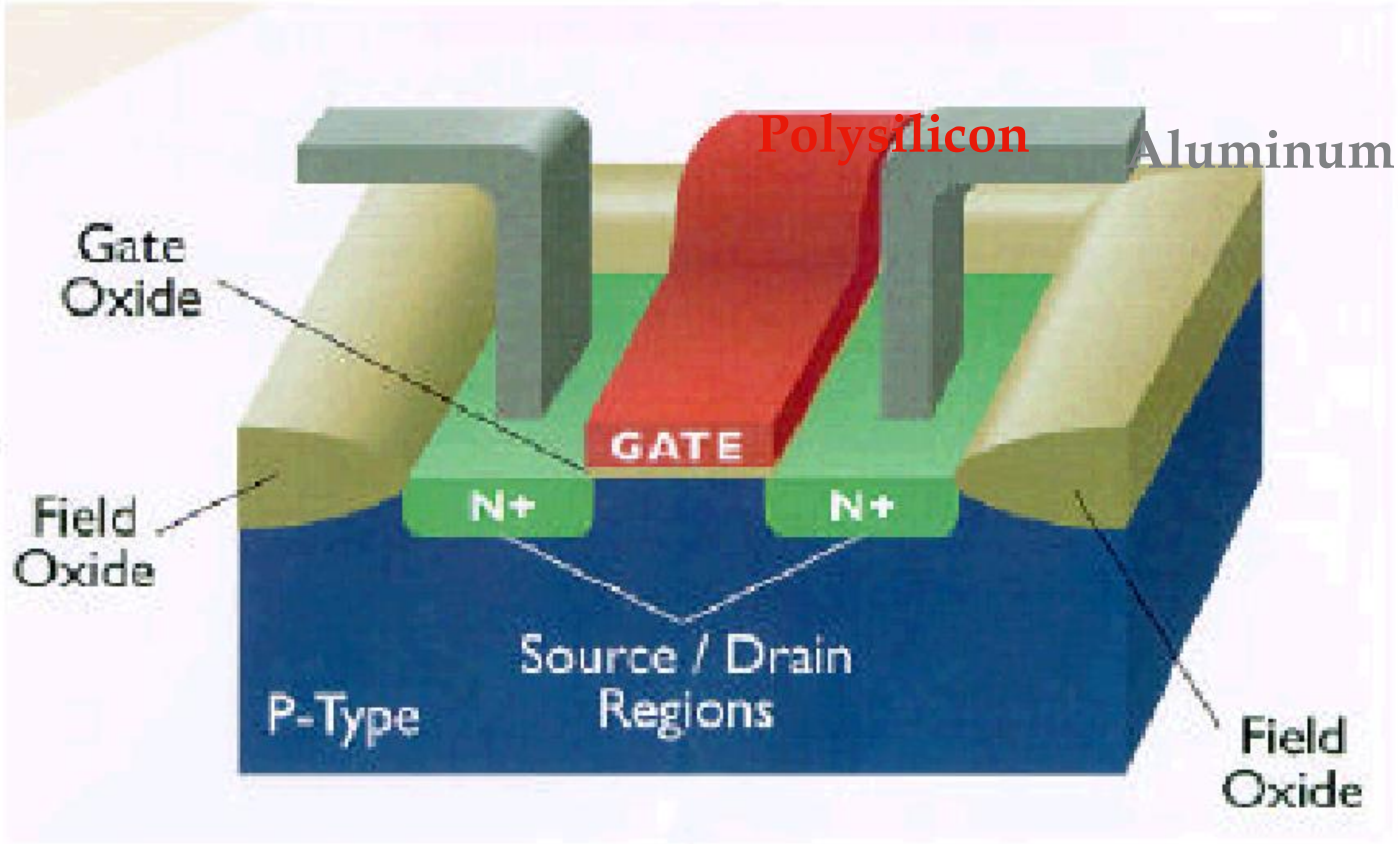
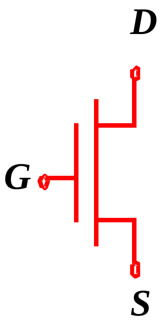
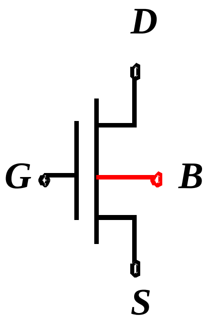
The MOS Transistor



MOS Transistors - Types and Symbols

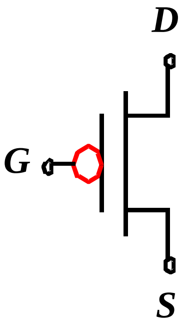
NMOS





NMOS with Body Contact

PMOS



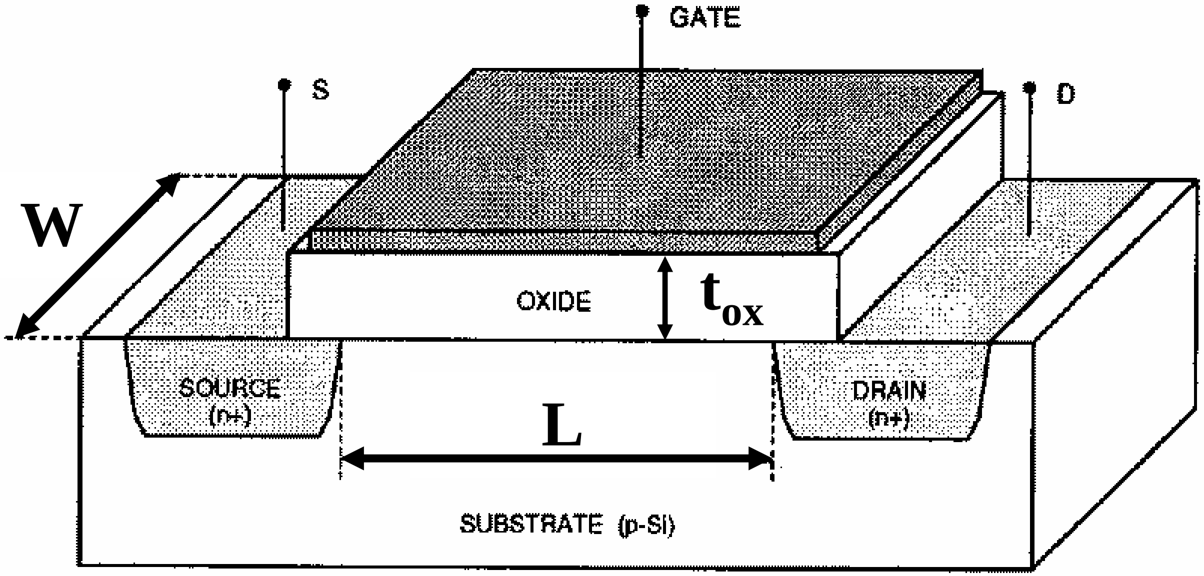
For NMOS: Body tied to Gnd

For PMOS: Body tied to Vdd

Why?

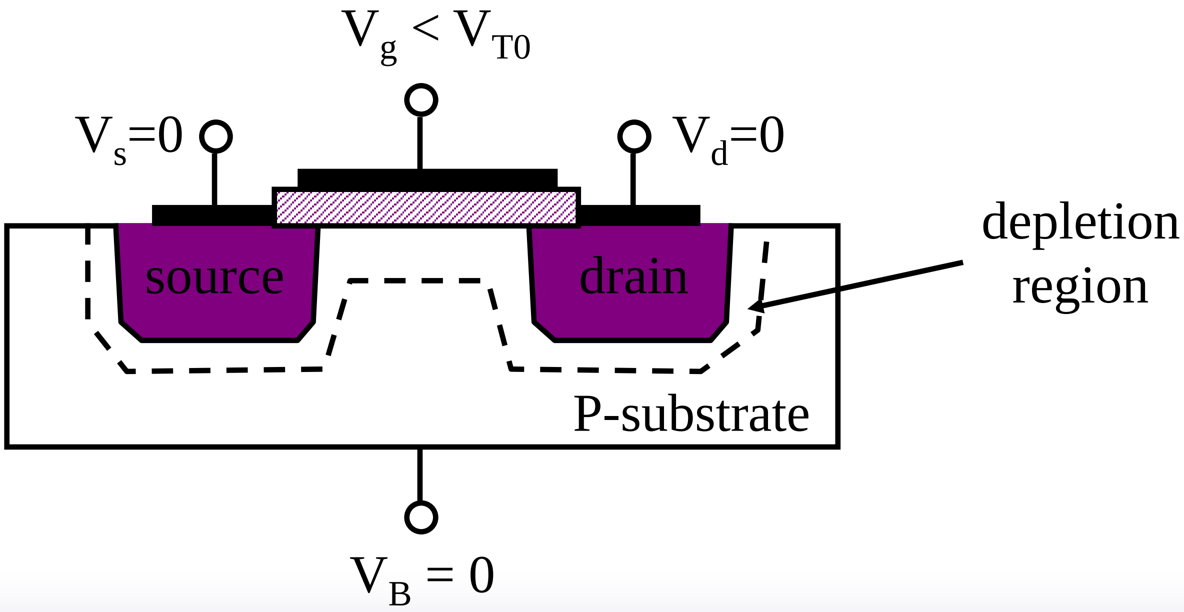
MOS Transistor

- Important transistor physical characteristics
  - Channel length L
  - Channel width W



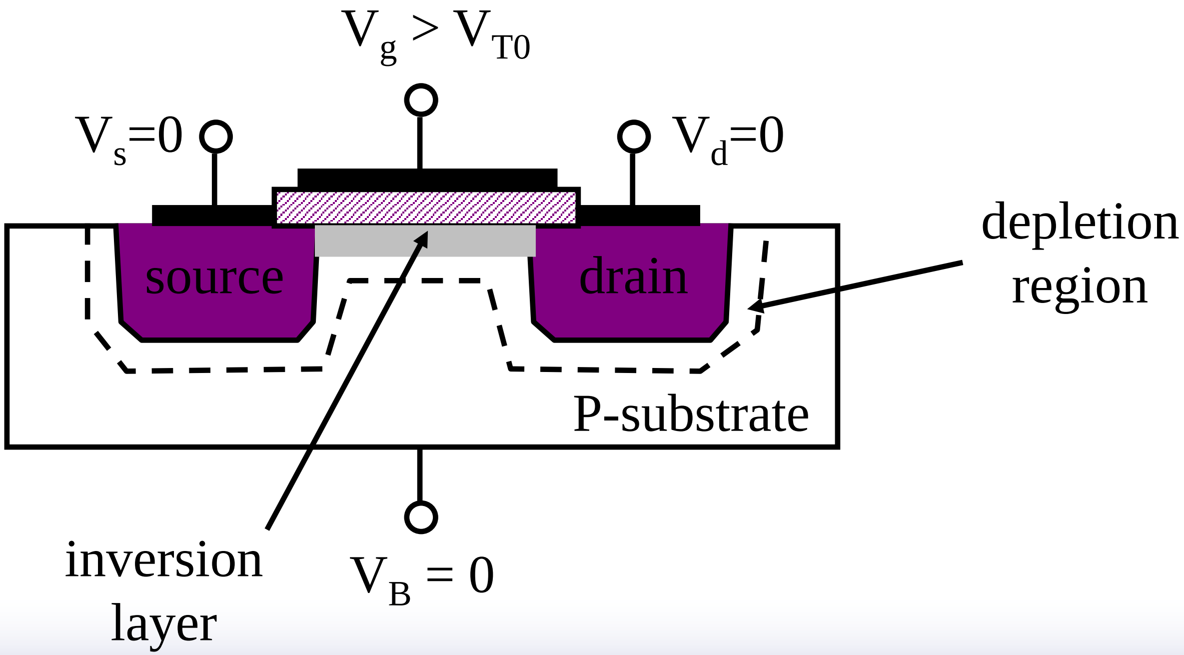
MOS Transistor Operation

- Simple case: $V_D = V_S = V_B = 0$
  - Operates as MOS capacitor
- When $V_{GS}<V_{T0}$ (but positive) , depletion region forms
  - No carriers in channel to connect S and D
- V_{T0} is known as the *threshold voltage*

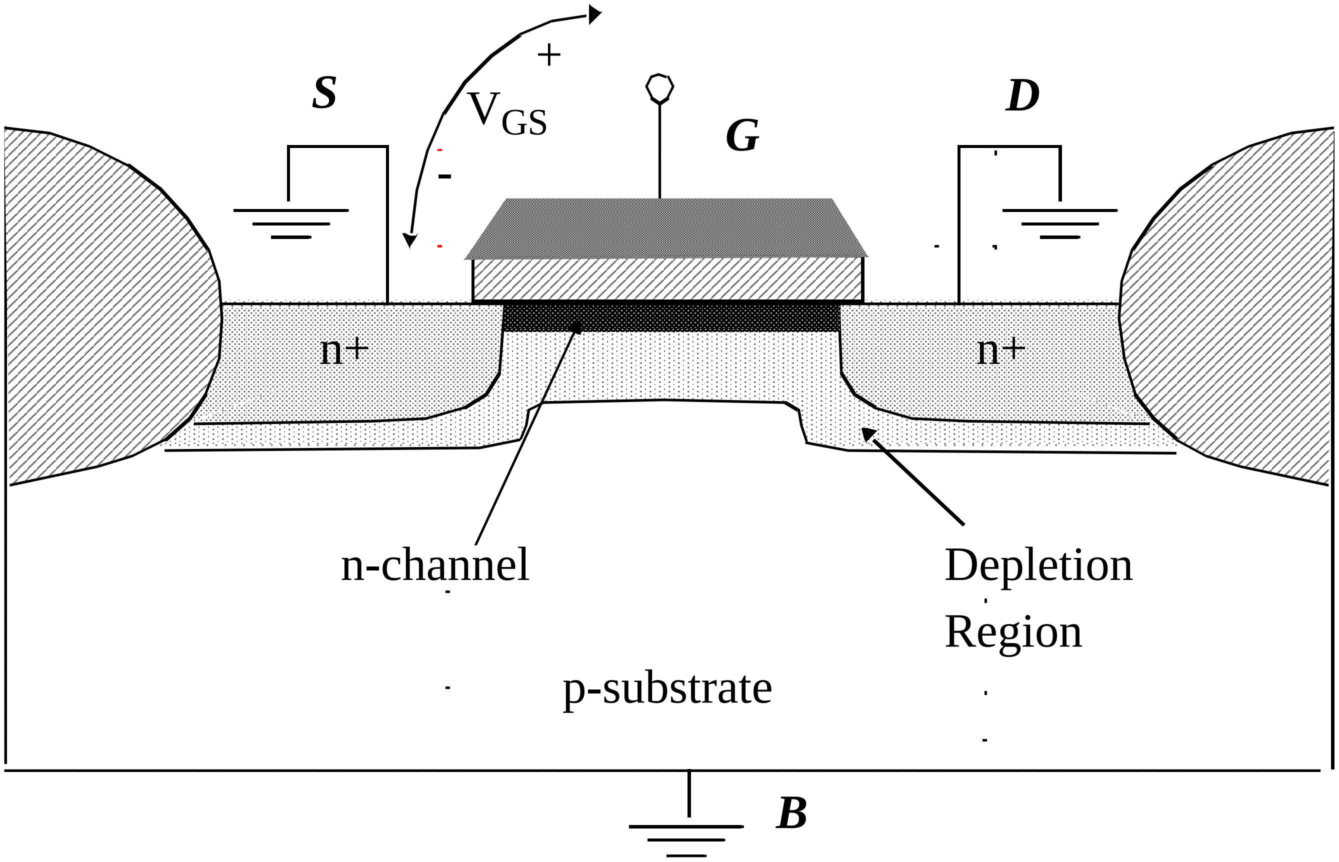


MOS Transistor Operation

- When $V_{GS} > V_{T0}$, inversion layer forms
- Source and drain connected by conducting n-type layer (for NMOS)



Threshold Voltage (V_{T0}): Concept



Note: gate is insulated from the substrate…hence no dc current flows through the oxide…channel is capacitively coupled to the gate through the electric-field in the oxide….that's how it gets the name MOS-FET (field effect transistor)

Physical Parameters that Affect V_{T0}

- Threshold voltage (V_{T0}): voltage between gate and source required for inversion
  - NMOS Transistor is “off” when $V_{GS} < V_{T0}$
- Components:
  - Work function difference between gate and channel (Flat-band voltage)
  - Gate voltage to change surface potential
  - Gate voltage to offset depletion region charge
  - Gate voltage to offset fixed charges in gate oxide and in silicon-oxide interface

Threshold voltage (1)

- Work function difference $q\Phi_{GC}$ between gate and channel
  - Represents built-in potential of MOS system
  - For metal gate: $\Phi_{GC} = \Phi_M$(metal-gate) - Φ_F(substrate) = Φ_{ms}
  - For poly gate: $\Phi_{GC} = \phi_F$(poly-Si-gate) - ϕ_F(substrate)

$$V_{T0} = \Phi_{GC} + \cdots$$

Threshold voltage (2)

- First component accounts for built-in voltage drop
- Now apply additional gate voltage to achieve inversion: change surface potential by -2ϕ_F (note that ϕ_F is negative for p-type substrate)

$$V_{T0} = \Phi_{GC} - 2\phi_F + \cdots$$

Threshold voltage (3)

- Offset depletion region charge, due to fixed acceptor ions
- Calculate charge at inversion ($\phi_S = -\phi_F$)
  - From before: $Q = -\sqrt{2qN_A\varepsilon_{Si}\left|\phi_S - \phi_F\right|}$
  - So: $Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}\left|-2\phi_F\right|}$
  - For non-zero substrate bias ($V_{SB} \neq 0$):

Depletion charge is negative….why? (acceptor ions after accepting electrons are –ve)

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si}\left|-2\phi_F + V_{SB}\right|}$$

- Due to larger depletion region

Threshold voltage (3, cont.)

- To offset this charge, need voltage $-Q_B/C_{ox}$
- Cox = gate capacitance per unit area
  - $C_{ox}=\varepsilon_{ox}/t_{ox}$
  - t_{ox} = thickness of gate oxide (normally in Å)

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} + \cdots$$

Threshold voltage (4)

- Finally, correct for non-ideal fixed charges
  - Fixed positive charged ions at boundary between oxide and substrate. Density = N_{OX}
  - Due to impurities, lattice imperfections at interface
  - Positive charge density $Q_{ox} = qN_{ox}$
  - Correct with gate voltage = $-Q_{ox}/C_{ox}$
- Final threshold voltage formula (for NMOS):

$$\boxed{V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}}$$

Threshold voltage, summary

- If $V_{SB} = 0$ (no substrate bias):

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

- If $V_{SB} \neq 0$ (non-zero substrate bias)

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right)$$

For uniform body doping….

- Body effect (substrate-bias) coefficient:

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}}$$

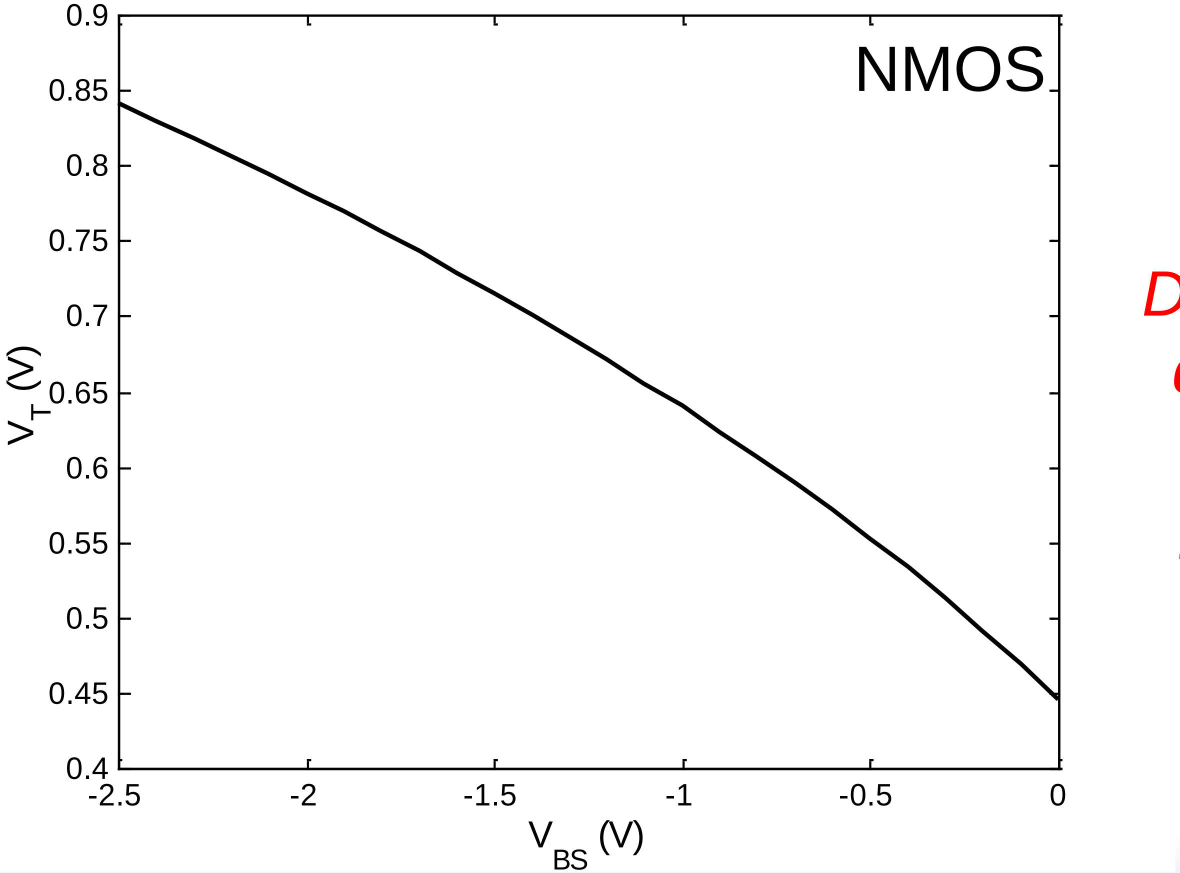
+ for NMOS
- for PMOS

For modern FETs with retrograde doping, V_T varies ~linearly with V_{SB}

- Threshold voltage increases as V_{SB} increases!

(easy to explain with a band diagram….)

The Body Effect



Draw a band diagram to convince yourself…

Threshold Voltage (NMOS vs. PMOS)

	NMOS	PMOS
Substrate Fermi potential	$\phi_F < 0$	$\phi_F > 0$
Depletion charge density	$Q_B < 0$	$Q_B > 0$
Substrate bias coefficient	$\gamma > 0$	$\gamma < 0$
Substrate bias voltage	$V_{SB} > 0$	$V_{SB} < 0$
Threshold voltage (enhancement devices)	$V_{T0} > 0$	$V_{T0} < 0$

***Remember:** You need not memorize this table but rather should be able to fill it in based on the band diagrams…*

Threshold Voltage Adjustment

- Threshold voltage can be changed by doping the channel region with donor or acceptor ions
- For NMOS:
  - V_T increased by adding acceptor ions (p-type)
  - V_T decreased by adding donor ions (n-type)
  - Opposite for PMOS
- Approximate change in V_{T0}:
  - Density of implanted ions = N_I [cm^{-2}]
  - Assume all implanted impurities are ionized

$$\Delta V_{T0} = \frac{qN_I}{C_{ox}}$$

Example: V_{T0} Adjustment

- Consider an NMOS device:
  - P-type substrate: $N_A = 2 \times 10^{16}\ \text{cm}^{-3}$
  - Polysilicon gate: $\Phi_{GC} = -0.92\text{V}$
  - $t_{ox} = 600$ Å   (1Å $= 1 \times 10^{-8}$ cm)
  - $N_{ox} = 2 \times 10^{10}$ cm-2
  - $\varepsilon_{Si} = 11.7\ \varepsilon_{0},\ \varepsilon_{ox} = 3.97\ \varepsilon_0$
- (a) Find V_{T0}
- (b) Find amount and type of channel implant to get $V_{T0} = 0.4$ V

MOS Capacitor (Review)

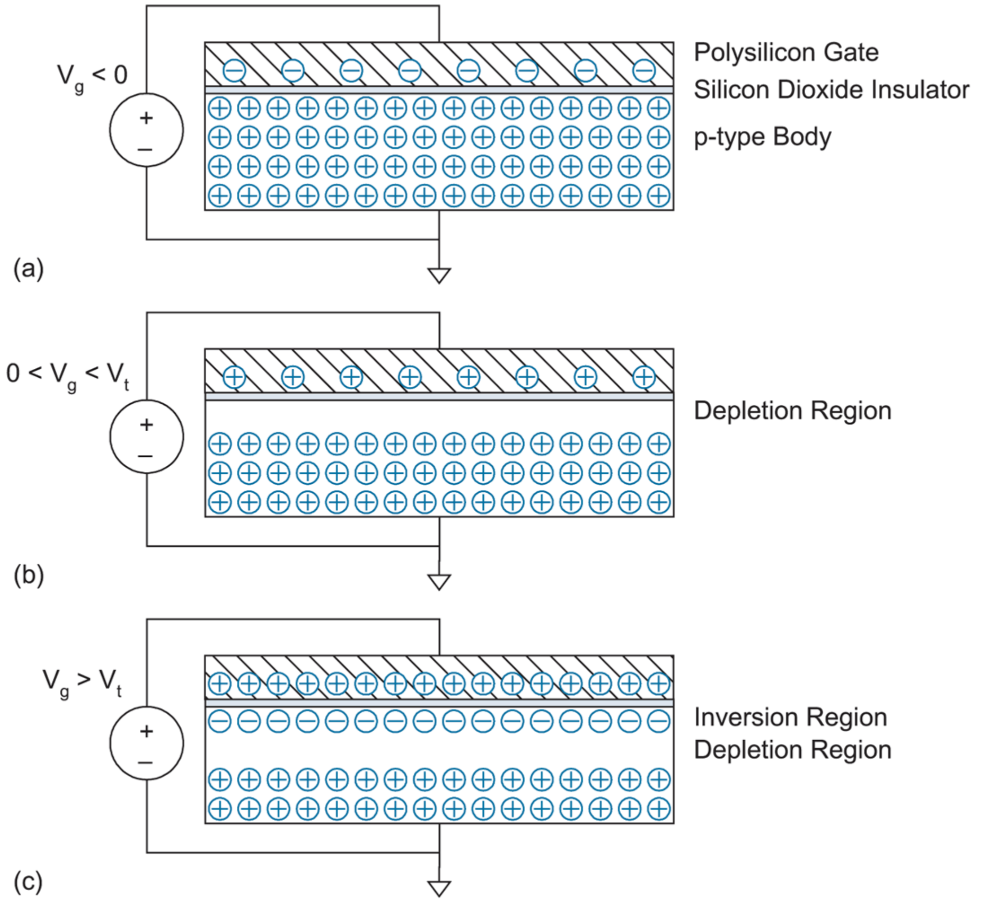


FIG 2.2 MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion

MOSFET Operation (NMOS)

Easy to understand with a band diagram across S-Ch-D…..

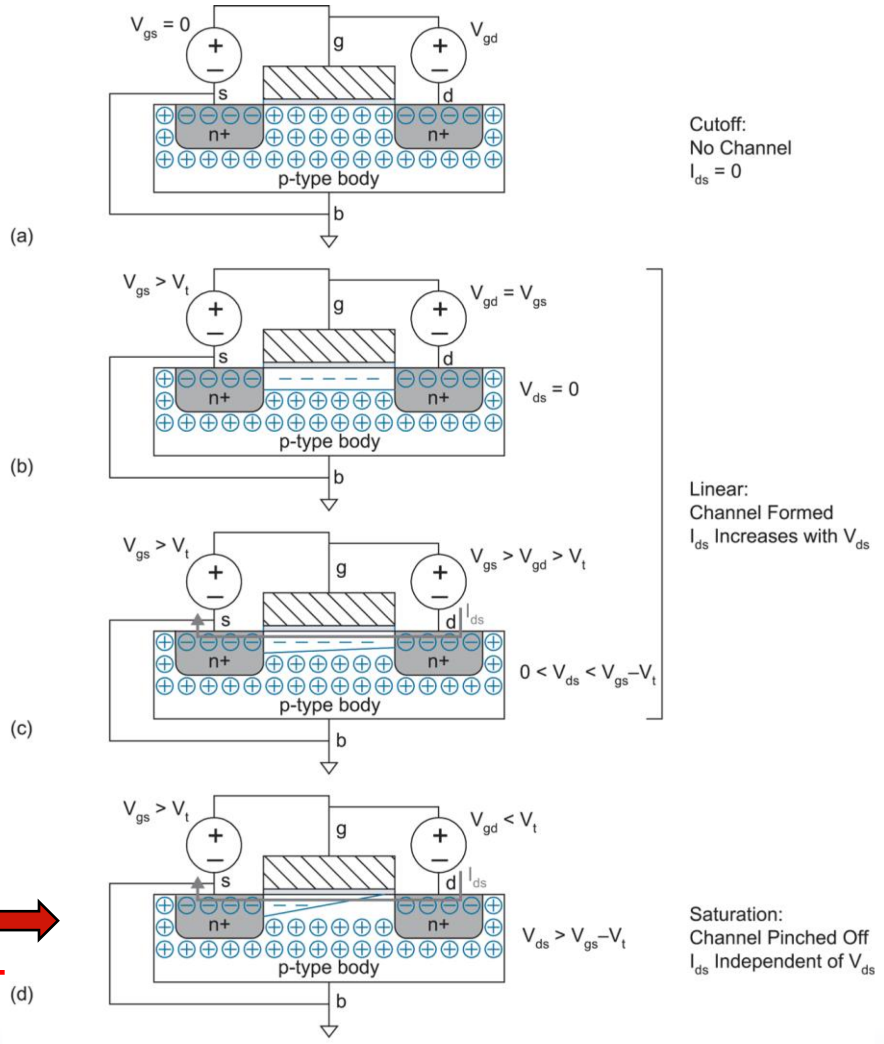


FIG 2.3 nMOS transistor demonstrating cutoff, linear, and saturation regions of operation

Remember, both drift and diffusion currents play a role…

***Pinch-off:* conduction still takes place from Source to Drain due to drift of electrons under the influence of the +ve drain voltage**

$V_{GS} - V(x) < V_t$

Conduction dominated by DRIFT

NMOS Output Characteristics

Recall that the surface channel vanishes at the drain end of the channel….when current saturates…known as "pinch-off"

Any voltage $V_{DS} > V_{D,sat}$ is dropped across the high-field pinch-off region…where inversion charge =0

Long Channel Transistor:

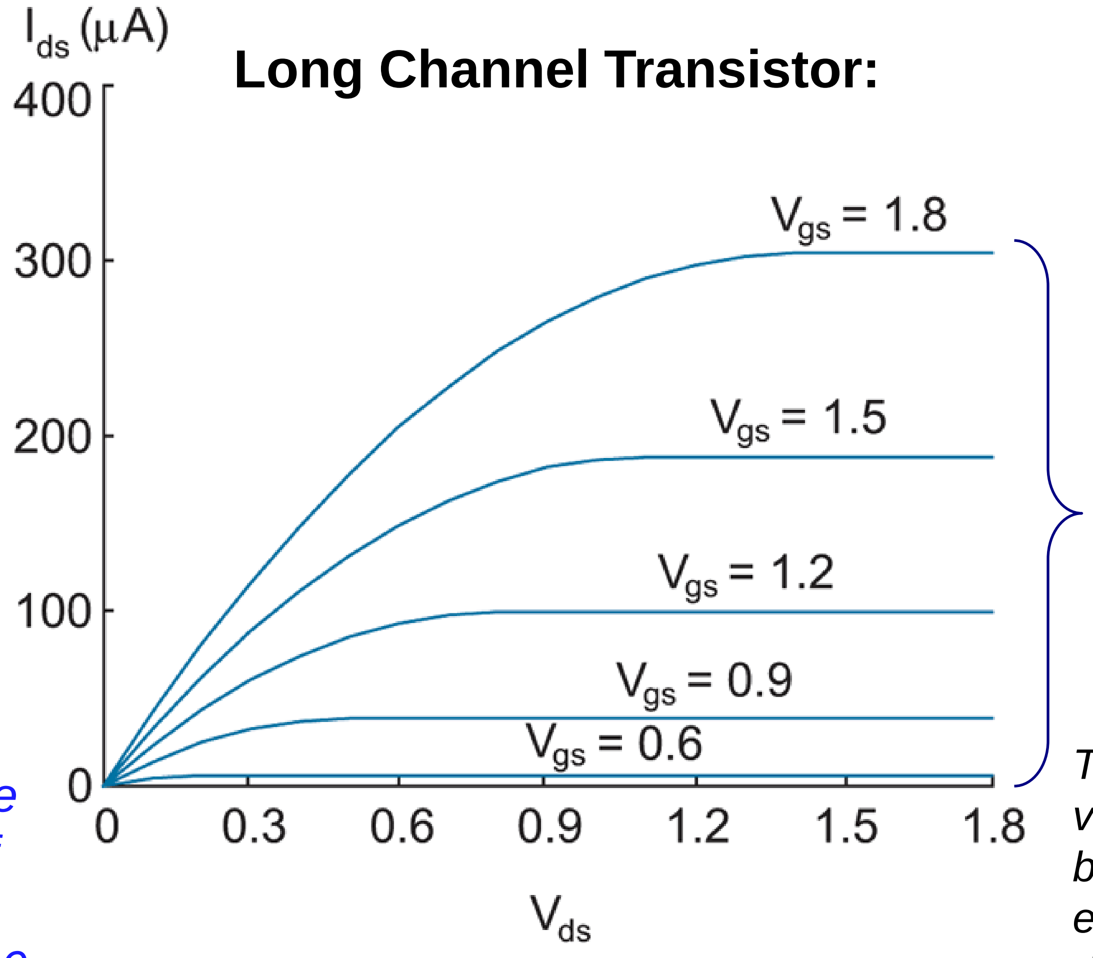


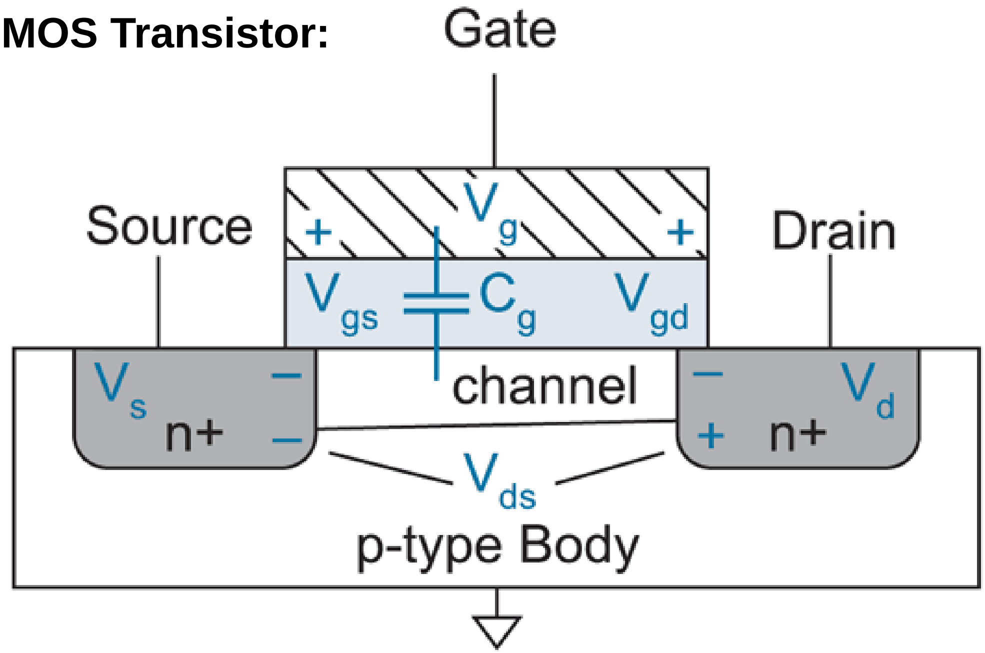
FIG 2.7 I-V characteristics of ideal nMOS transistor

Quadratic Relationship

The saturation voltage $V_{D,sat}$ can be estimated by equating dI_{ds}/dV_{ds} to zero

Channel Mobile Charge

NMOS Transistor:



Note: i) The inversion layer thickness is assumed to be zero: all charges are assumed to be located at the Si surface….like a sheet of charge….
ii) Hence, there is no potential drop or band bending across the inversion layer….

$V_{ds} = V_{gs} - V_{gd}$ *Use Kirchoff's voltage law: -Vgs + Vds + Vdg = 0*

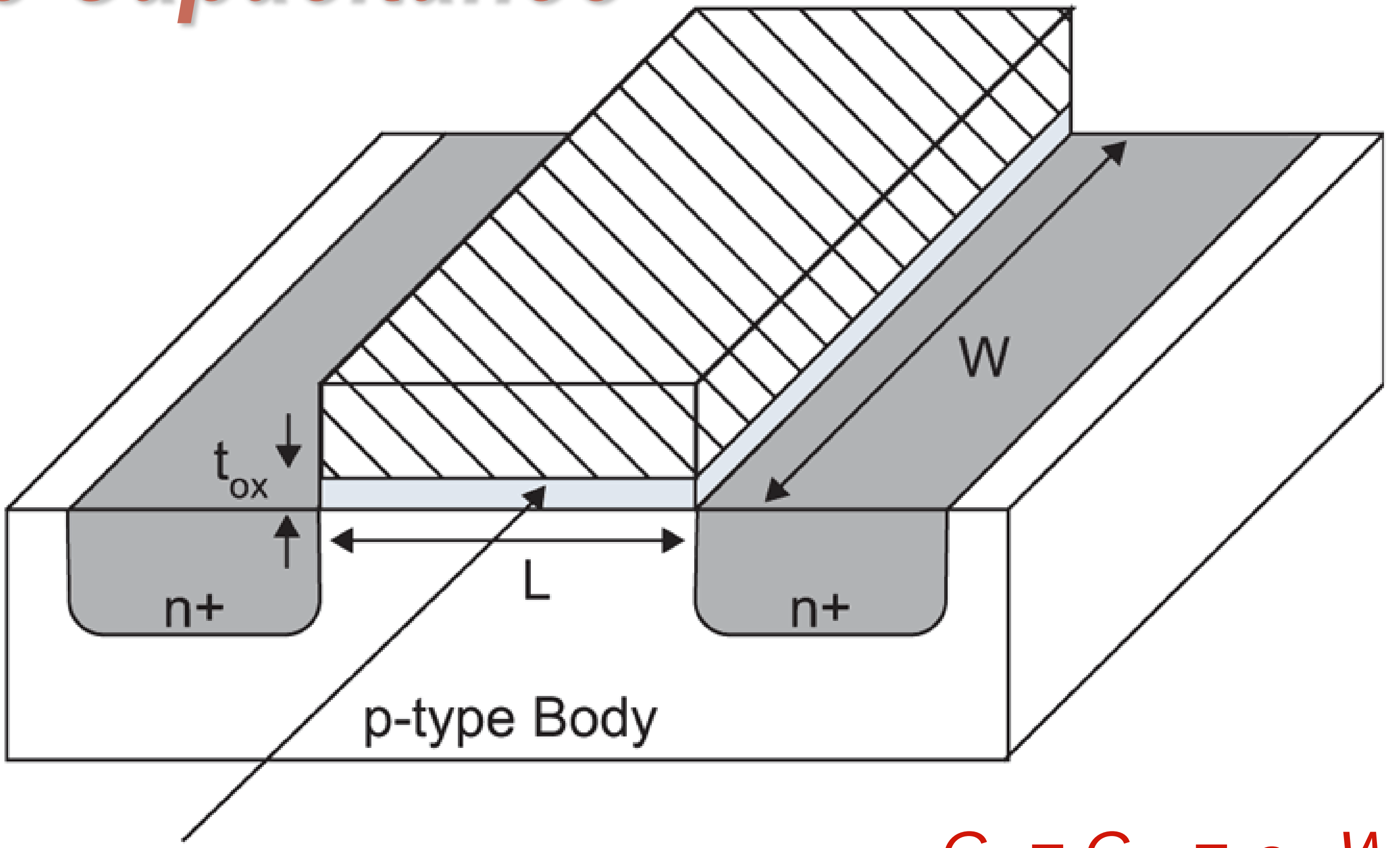
Average gate to channel potential:

$$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$$

$$Q_{channel} = C_g\,(V_{gc} - V_t)$$

FIG 2.5 Average gate to channel voltage

Gate Capacitance



SiO_2 Gate Oxide
(Good insulator, $\varepsilon_{ox} = 3.9\varepsilon_0$)

$$C_g = C_{ox} = \varepsilon_{ox} WL/t_{ox}$$

FIG 2.6 Transistor dimensions

Transistor Currents (NMOS)

Cutoff Region: $I_{ds} = 0,\ V_{gs} < V_t$

Linear Region: $V_{gs} > V_t,\ V_{ds} < V_{gs} - V_t$

$I_{ds} = W\, Q_{channel}$ .carrier velocity(v)

$I_{ds} = \mu\, C_{ox}\, W/L\, (V_{gs} - V_t - V_{ds}/2) V_{ds}$

Since Vds is small, Vds/2 can be neglected…and Ids is linearly proportional to Vds….like a resistor

$Q_{channel} = C_g\, (V_{gc} - V_t)$

$V_{gc} = V_{gs} - V_{ds}/2$

$v = \mu E$

$E_{lateral} = V_{ds}/L$

$\beta = \mu\, C_{ox}\, W/L$

Saturation Region: $V_{gs} > V_t,\ V_{ds} > V_{gs} - V_t$

Note: as Vds increases, average $Q_{channel}$ decreases…since Vgc decreases

$dI_{ds}/dV_{ds} = 0$ at $V_{ds} = V_{dsat} = V_{gs} - V_t$

Substituting V_{ds} with V_{dsat} above: $I_{ds} = \beta/2\, (V_{gs} - V_t)^2$

Note: for PMOS $V_{tp} = V_{tn}$ $\mu_p < \mu_n$, hence $(W/L)_{PMOS} \sim 2\, (W/L)_{NMOS}$

PMOS Transistor

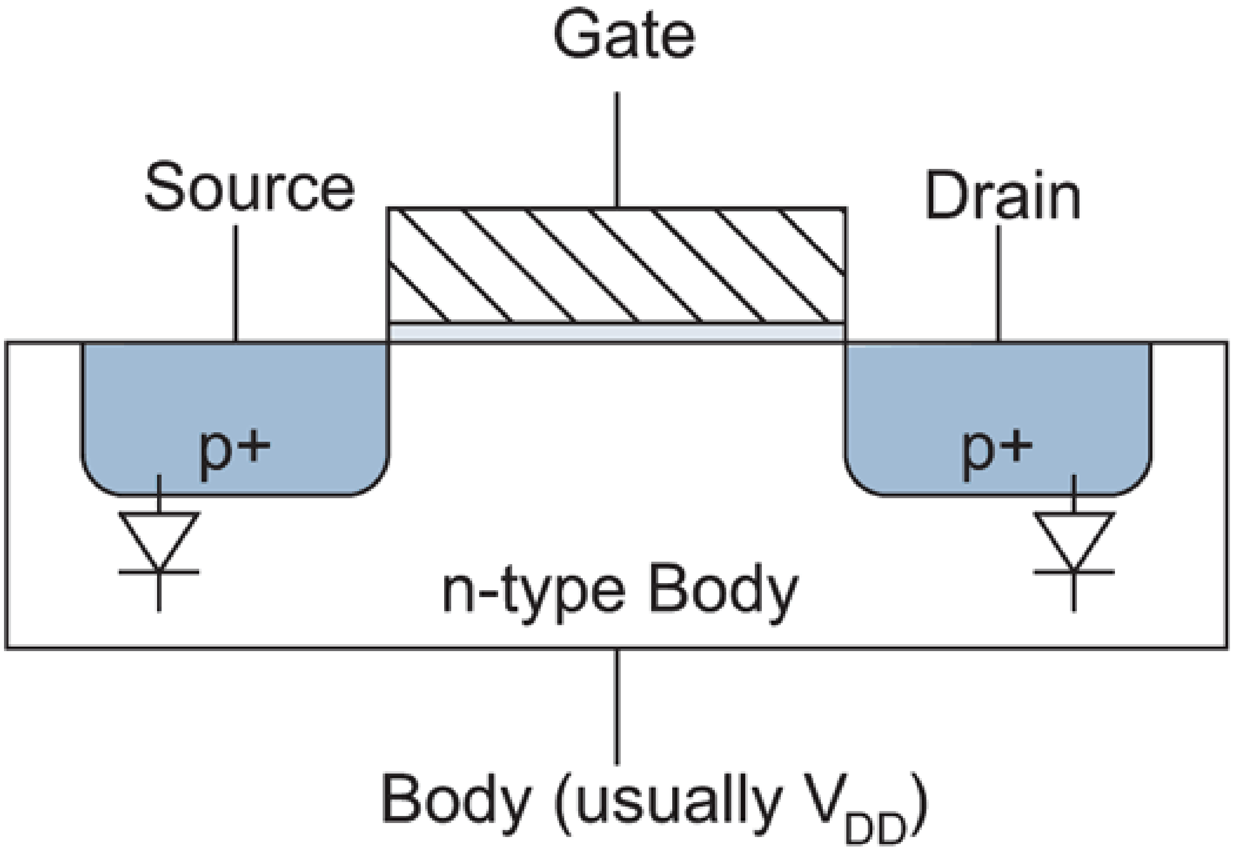


FIG 2.4 pMOS transistor

PMOS Output Characteristics

Long Channel Transistor:

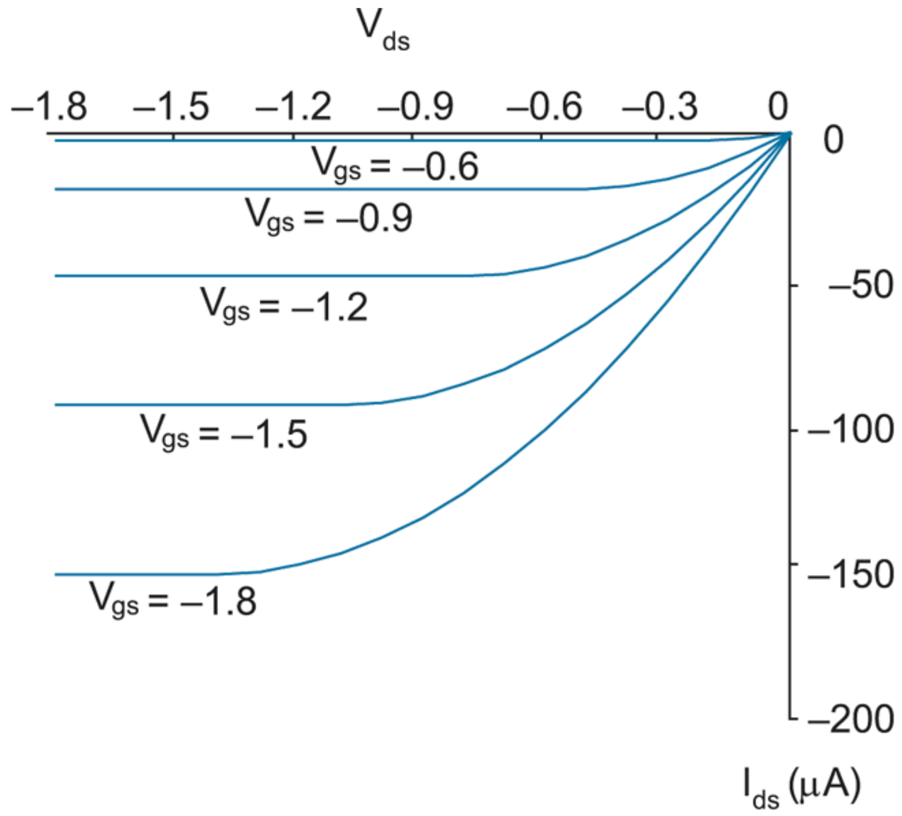


FIG 2.8 I-V characteristics of ideal pMOS transistor

Channel Length Modulation

- In saturation, pinch-off point moves
  - As V_{DS} is increased, pinch-off point moves closer to source
  - Effective channel length becomes shorter
  - Current increases due to shorter channel

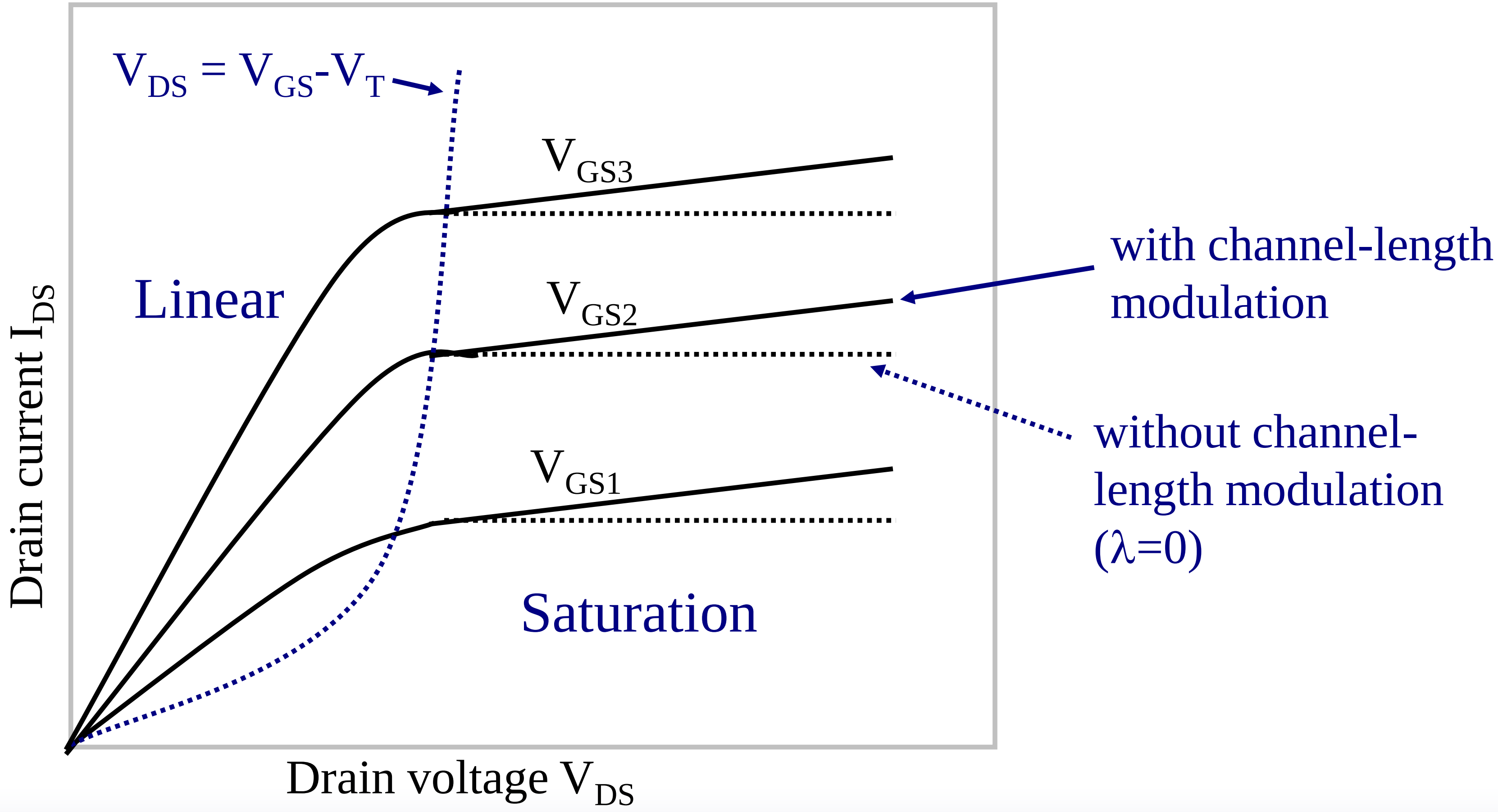
$$L' = L - \Delta L$$

$$\boxed{I_D = \tfrac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)}$$

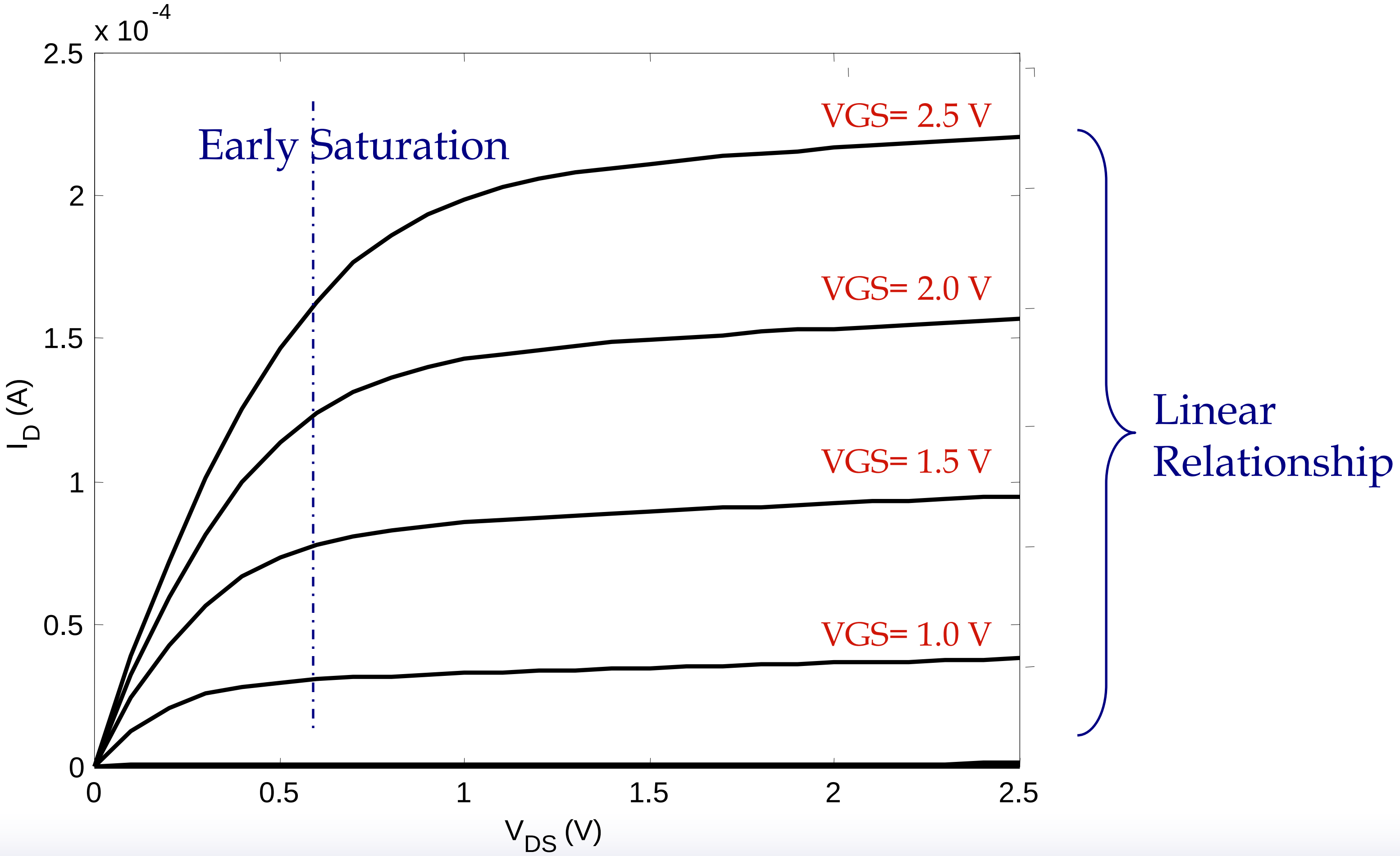
λ = channel length modulation coefficient

Summary: MOS Output I/V

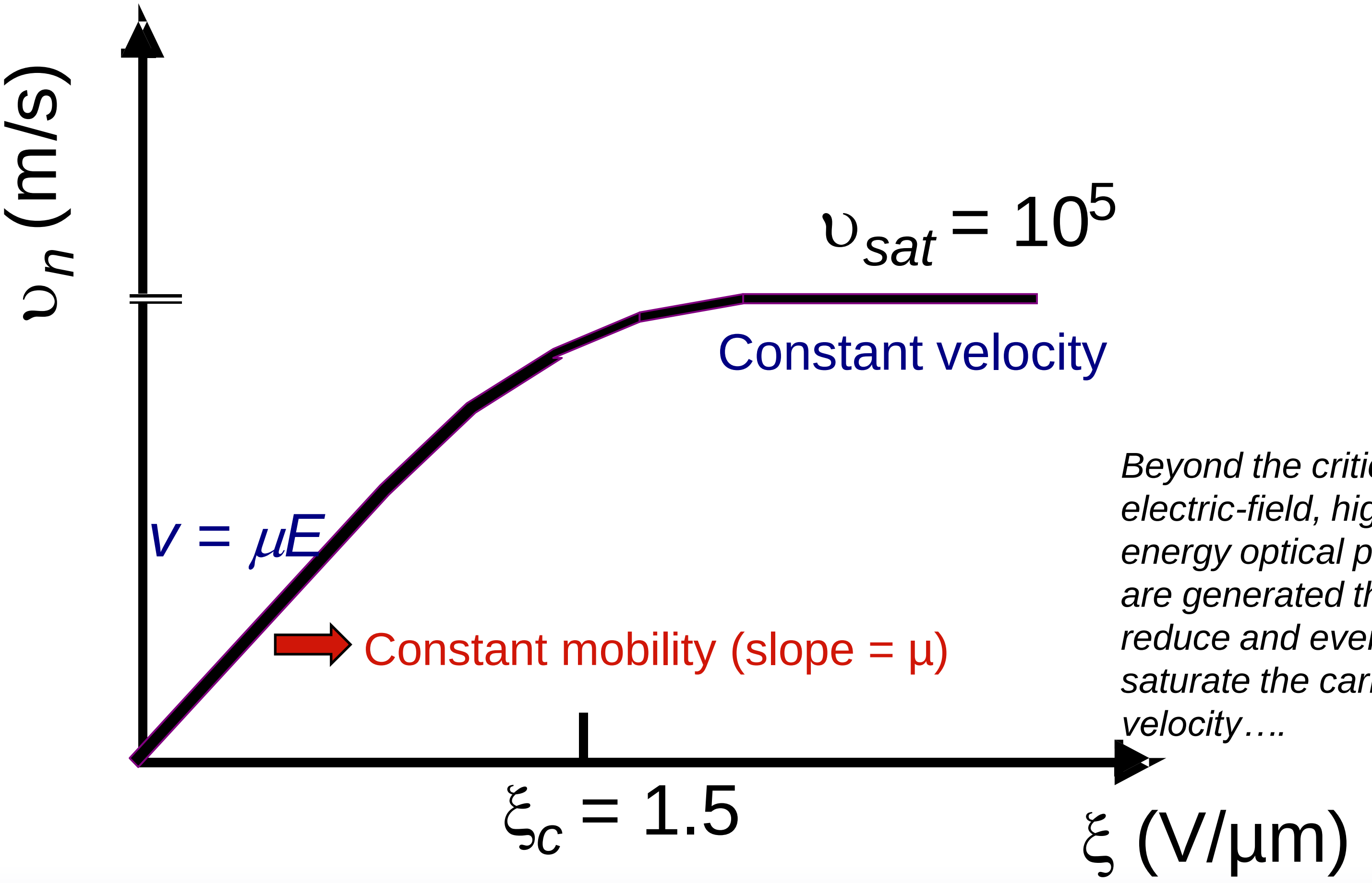
I/V curve for NMOS device:



Current-Voltage Relations Short-Channel Transistors

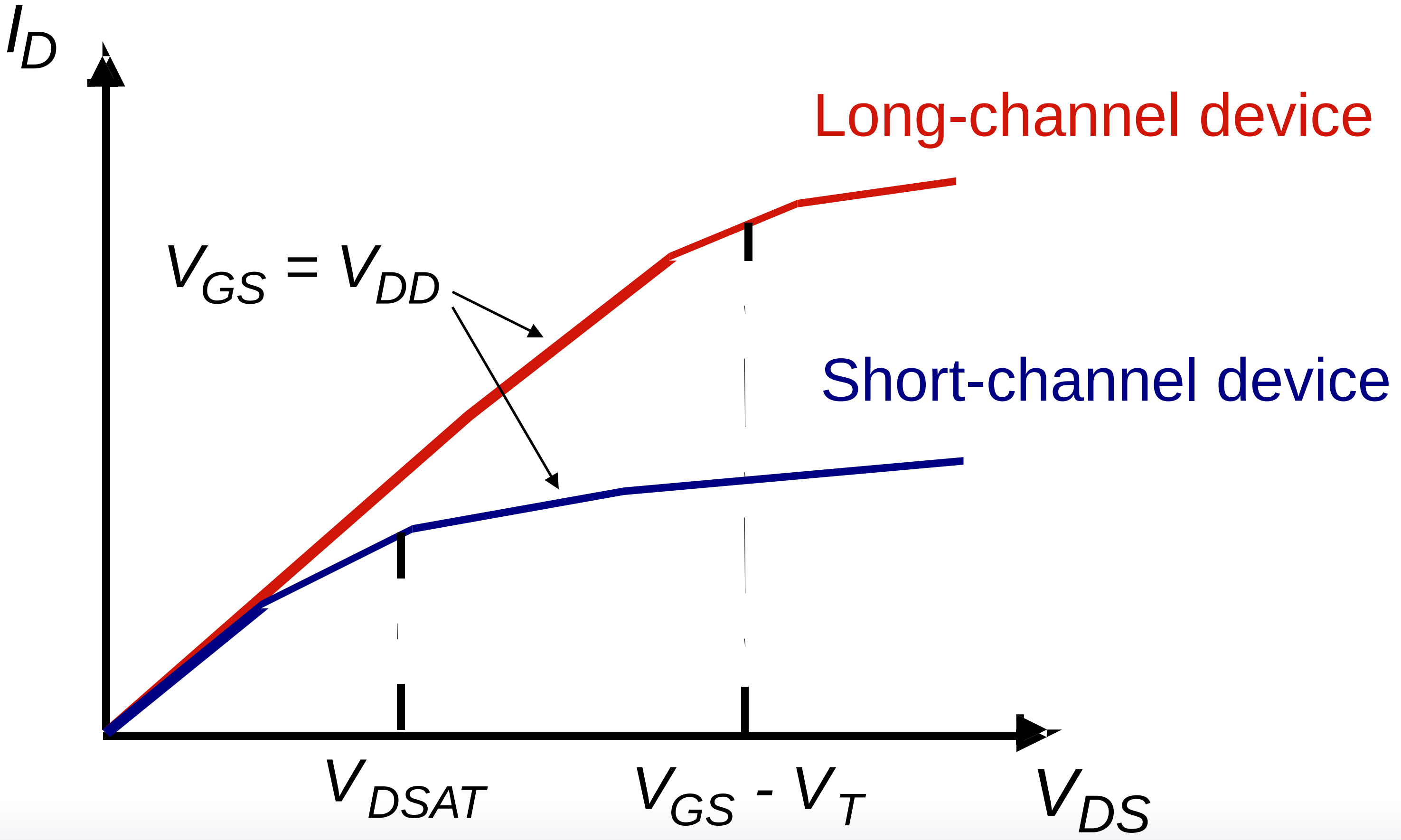


Velocity Saturation



Beyond the critical electric-field, higher energy optical phonons are generated that reduce and eventually saturate the carrier velocity….

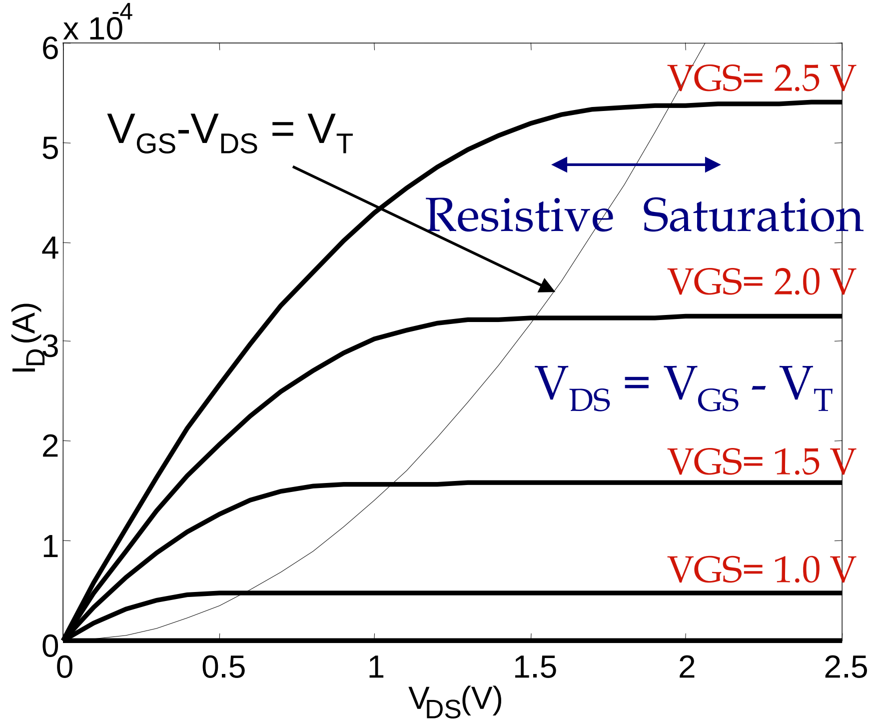
Perspective



Output Characteristics: I_D versus V_{DS}

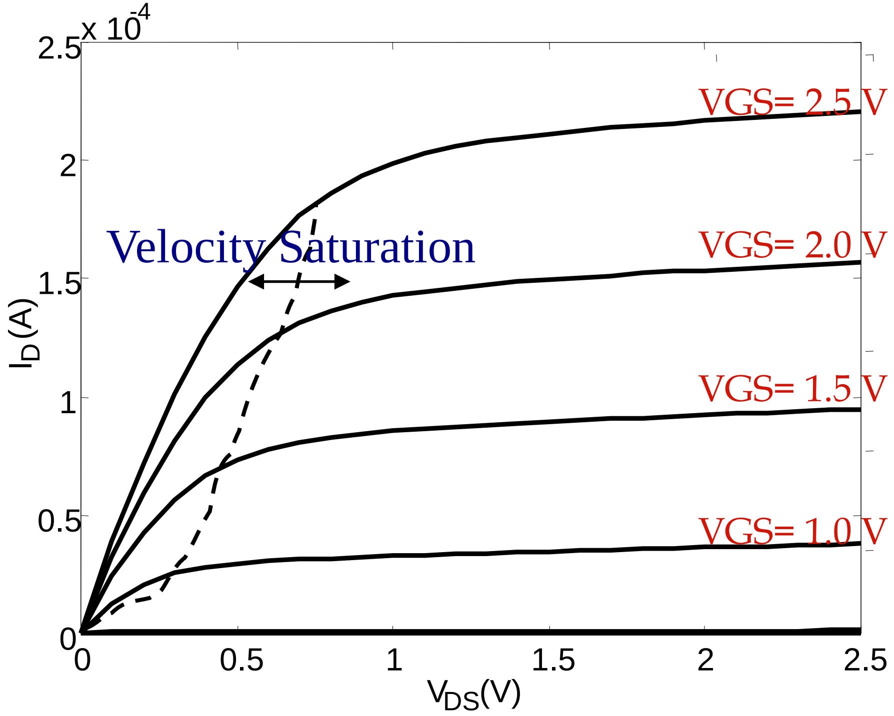
W/L = 1.5 for both cases….

L = 10 um



Long Channel

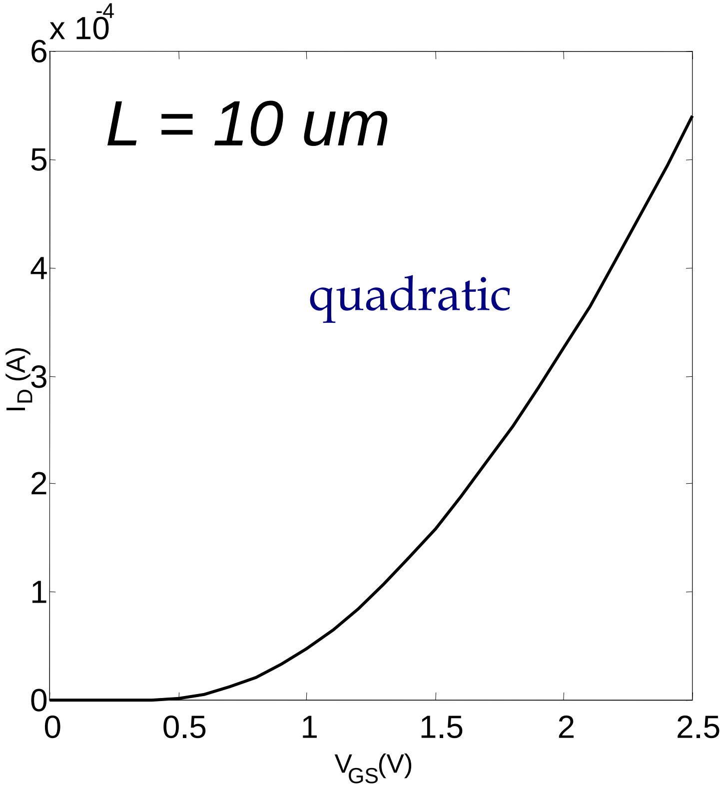
L = 0.25 um



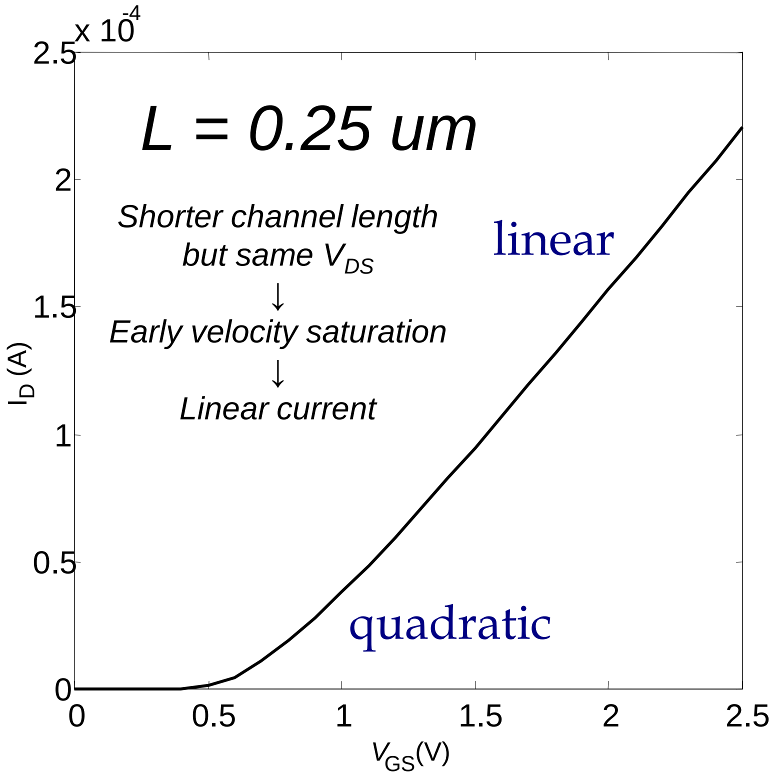
Short Channel

Input Characteristics: I_D versus V_{GS}

At small V_{GS} - current is dominated by pinch-off, hence, I_D is quadratic with V_{GS}



Long Channel



Shorter channel length
but same V_{DS}
↓
Early velocity saturation
↓
Linear current

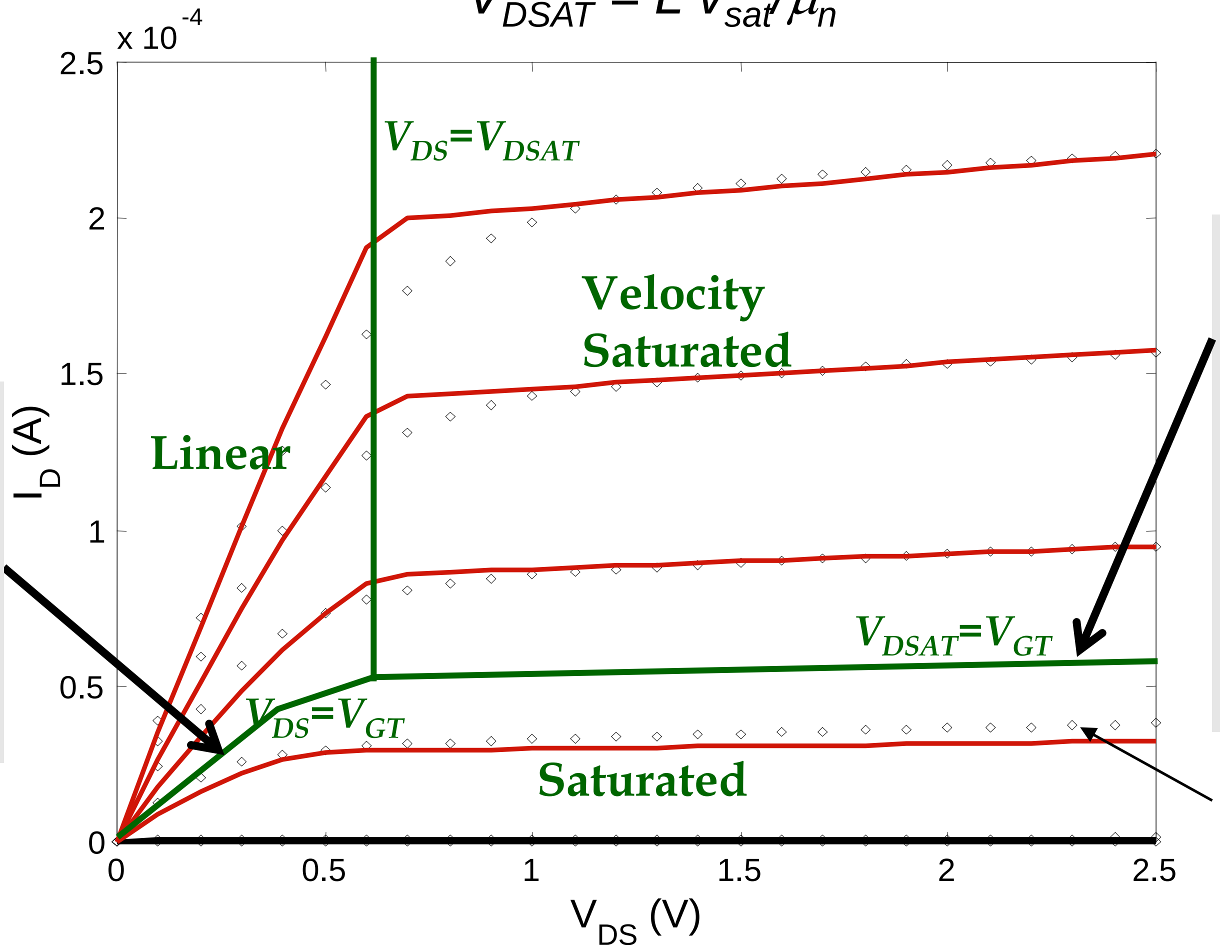
Short Channel

Note: These are Linear-Linear Plots!!

Simple Model (solid lines) versus SPICE

$V_{GT} = V_{GS} - V_T$

$V_{DSAT} = L\, v_{sat}/\mu_n$



Above this curve, *VGS-VT > VDS, hence linear*

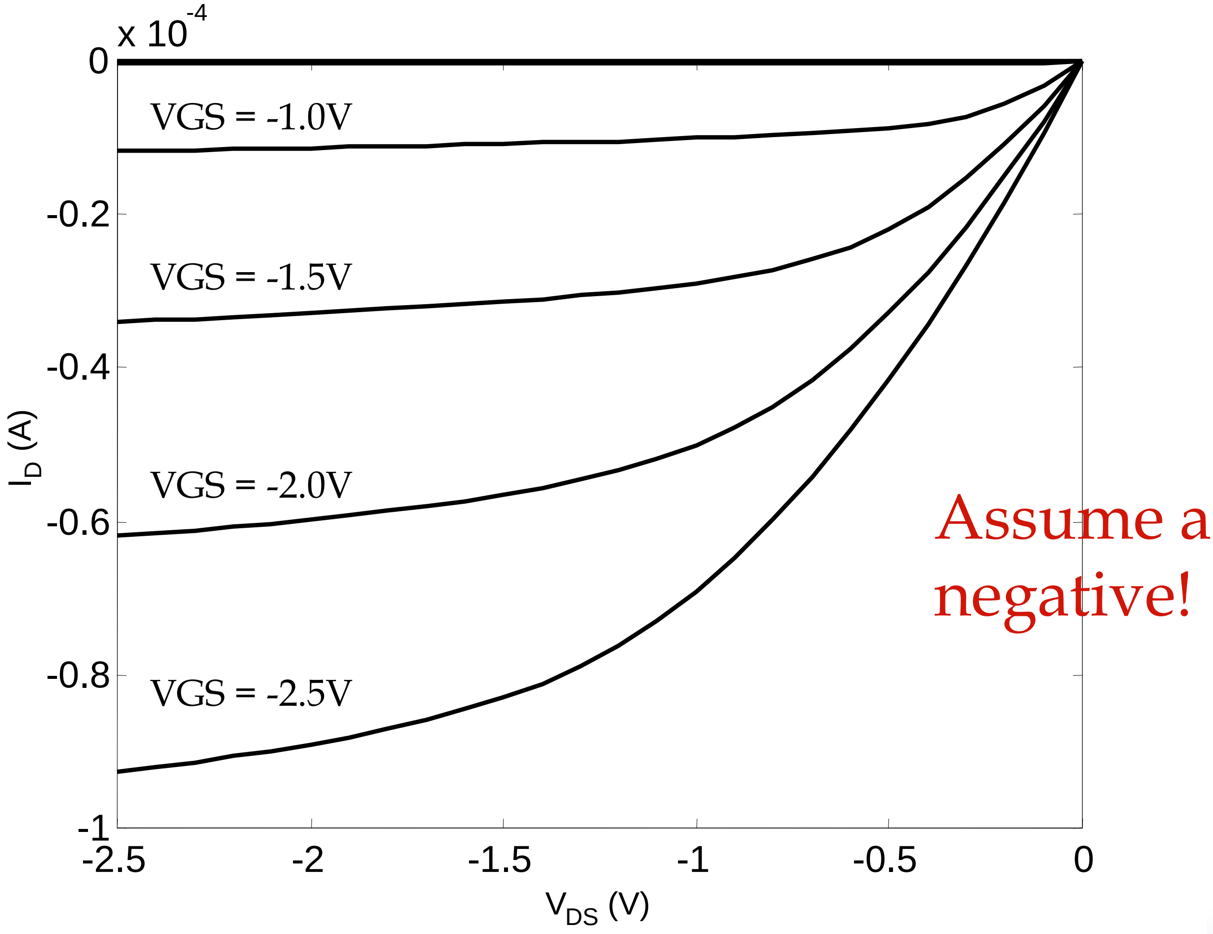
Below this curve, *VGS-VT < VDS, hence saturated*

Above this curve, *V_{GS}-V_T >V_{DSAT} High carrier concentration, hence, no pinch-off*

Below this curve, *V_{GS}-V_T < V_{DSAT} Low carrier conc. hence, pinch-off*

Spice

A PMOS Transistor (short-channel)



Assume all variables negative!

Alpha-Power MOSFET Model

Note: Shockley method is based on the drift-diffusion transport….no velocity saturation effect

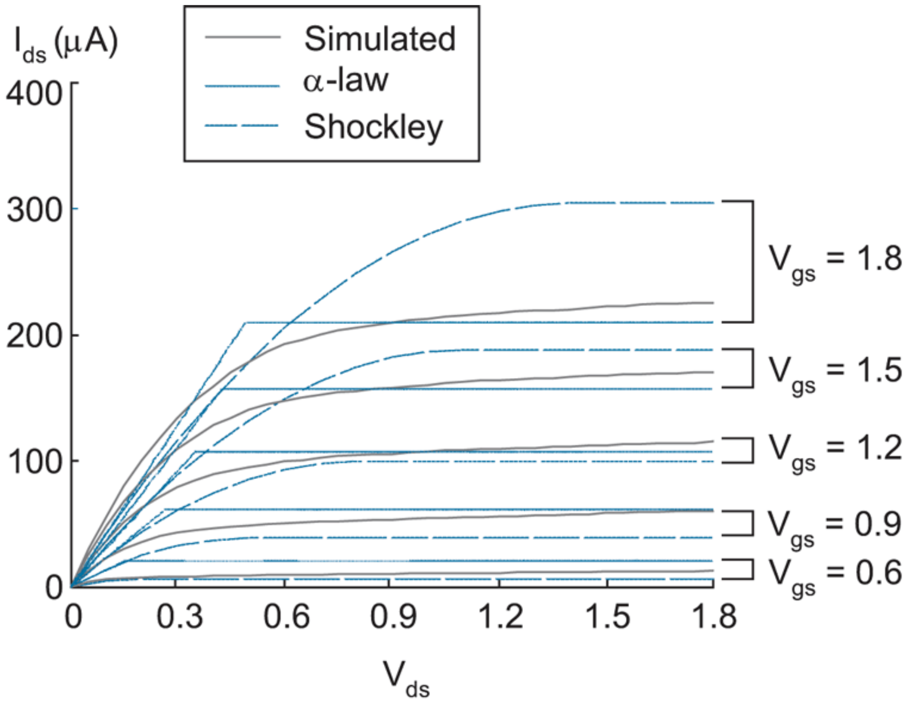


FIG 2.17 I-V characteristics for nMOS transistor with velocity saturation

At low lateral E-fields, V_{ds}/L, current increases linearly with E-field

At high fields, E= E_{sat}

Carrier velocity saturates due to carrier scattering = v_{sat} (= μ E_{sat})

$I_{ds} = \mu C_{ox} W/L (V_{gs} - V_t)^2$

---no velocity saturation

$I_{ds} = C_{ox} W (V_{gs} - V_t) v_{sat}$

---complete velocity saturation

Practical situation: carrier velocity doesn't increase linearly with field but is not completely velocity saturated….

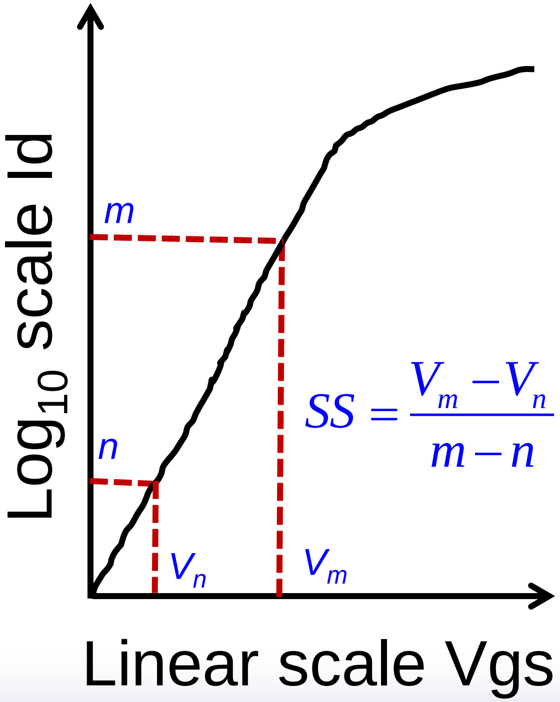
Sakurai Model: $I_{ds} \propto (V_{gs} - V_t)^{\alpha}$

$1<\alpha<2$, is the velocity saturation index, determined by curve fitting…..also accounts for mobility degradation due to high vertical field (V_{gs}/t_{ox})

How to Extract SS, G_m, and R_{out}

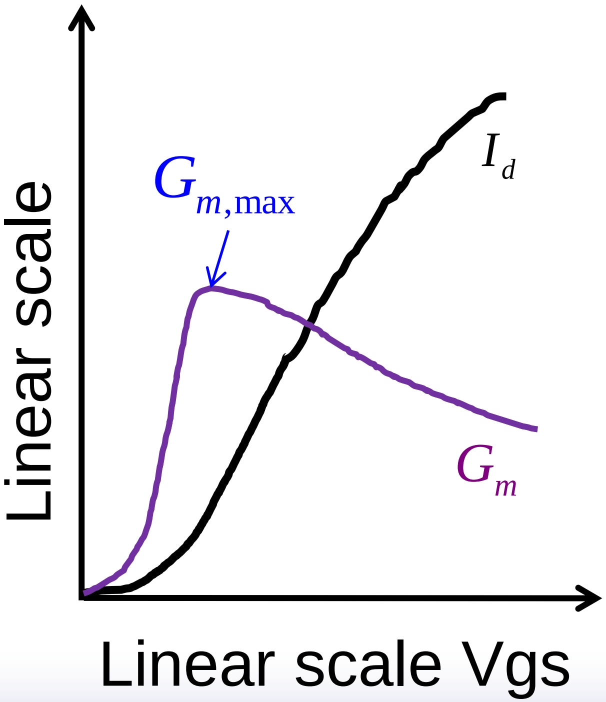
SS: Sub-threshold voltage swing

$$SS = \frac{dV_g}{d(\log_{10} I_d)}$$



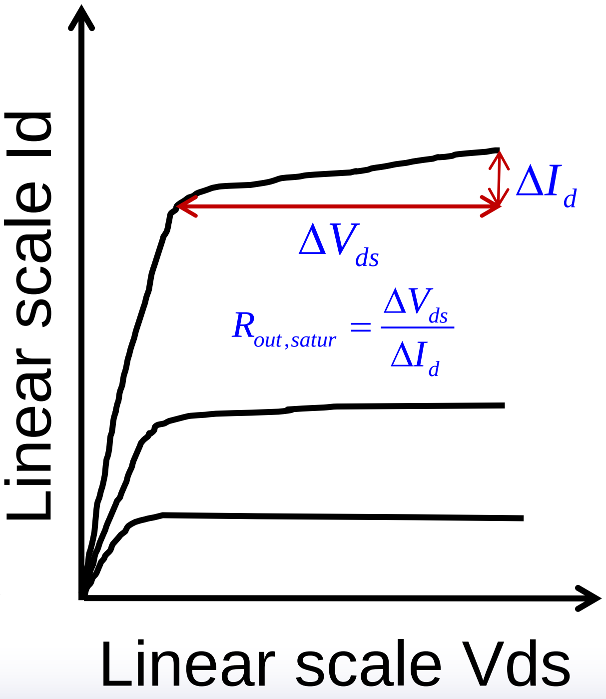
G_m: Transconductance

$$G_m = \frac{dI_d}{dV_g}$$



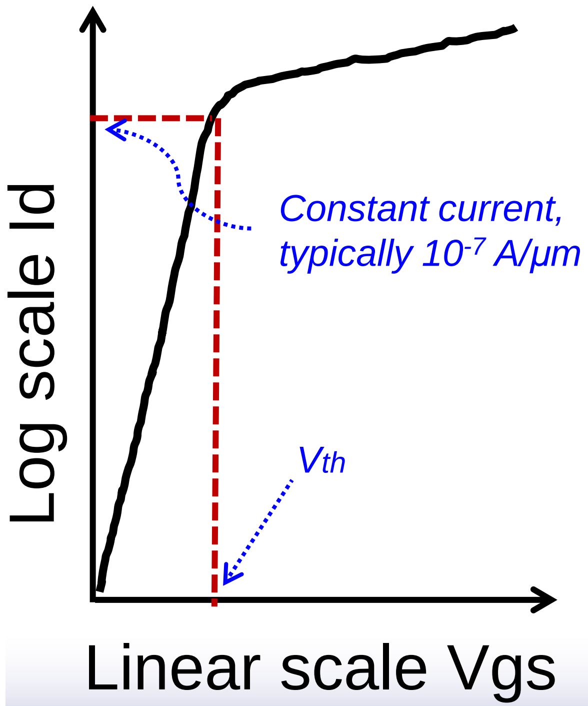
R_{out}: output resistance

$$R_{out} = \frac{dV_{ds}}{dI_d}$$



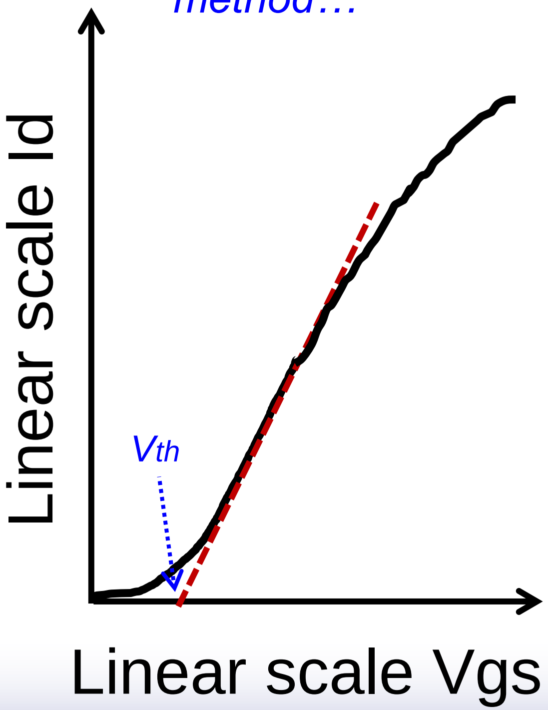
Methods to Extract Vth

① Constant current



② Tangent method

Also called maximum G_m method…



③ Second derivative of Id