ABSTRACT
A half bridge is described with at least one transistor having a channel that is capable in a first mode of operation of blocking a substantial voltage in at least one direction, in a second mode of operation of conducting substantial current in one direction through the channel and in a third mode of operation of conducting substantial current in an opposite direction through the channel. The half bridge can have two circuits with such a transistor.
Figure 2(a) (prior art)
BRIDGE CIRCUITS AND THEIR COMPONENTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application Ser. No. 61/028,133, filed on Feb. 12, 2008, which is incorporated herein for all purposes.

TECHNICAL FIELD

This invention relates to bridge circuits and the components of which they are comprised.

BACKGROUND

Bridge circuits are used in a wide range of applications. A typical 3-phase bridge circuit for a motor drive is shown in FIG. 1. Each of the three half bridges 15, 25, 35 in circuit 10 includes two switches (61-66), which are able to block current in one direction and are capable of conducting current in both directions. Because the transistors (41-46) commonly used in power circuits are inherently incapable of conducting current in the reverse direction, each of the switches 61-66 in circuit 10 comprises a transistor (41-46) connected anti-parallel to a freewheeling diode 51-56. The transistors 41-46 are each capable of blocking a voltage at least as large as the high voltage (HV) source of the circuit 10 when they are biased in the OFF state, and diodes 51-56 are each capable of blocking a voltage at least as large as the high voltage (HV) source of the circuit 10 when they are reverse biased. Ideally, the diodes 51-56 have good switching characteristics to minimize transient currents during switching, therefore Schottky diodes are commonly used. The transistors 41-46 may be enhancement mode (normally off, Vgs=0), i.e., E-mode, or depletion mode (normally on, Vgs=0), i.e., D-mode devices. In power circuits enhancement mode devices are typically used to prevent accidental turn on in order to avoid damage to the devices or other circuit components. Nodes 17, 18, and 19 are all coupled to one another via inductive loads, i.e., inductive components such as motor coils (not shown in FIG. 1).

FIG. 2a shows half bridge 15 of the full 3-phase motor drive in FIG. 1, along with the winding of the motor (inductive component 21) between nodes 17 and 18 and the switch 64 which the motor current feeds into. For this phase of power, transistor 44 is continuously on (Vgs=Vdb) and transistor 42 is continuously off (Vgs=Vdh, i.e., Vgs=0V if enhancement mode transistors are used), while transistor 41 is modulated with a pulse width modulation (PWM) signal to achieve the desired motor current. FIG. 2b, which is a simplified version of the diagram in FIG. 2a, indicates the path of the current 27 during the time that transistor 41 is biased on. For this bias, the motor current flows through transistors 41 and 44, while no current flow through switch 62 because transistor 42 is biased off and diode 52 is reverse biased. Referring to FIG. 2c, during the time that transistor 41 is biased off, no current can flow through transistor 41 or diode 51, and so the motor current flows through diode 52. During this portion of operation, the inductive component 21 forces the voltage at node 17 to a sufficiently negative value to cause diode 52 to conduct.

Currently, insulated gate bipolar transistors (IGBTs) are typically used in high power bridge circuits, and silicon MOS transistors, also known as MOSFETs, are used in low power applications. Traditional IGBTs inherently conduct in only one direction, and so a freewheeling diode is required for proper operation of a switch with an IGBT. A standard MOS transistor inherently contains an anti-parallel parasitic diode. As seen in FIG. 3a, if the gate and source of a MOS device 50 are biased at the same voltage and the drain is biased at a lower voltage, such as occurs in transistor 42 when transistor 41 is off (FIG. 2c), parasitic diode 60 prevents the intrinsic MOS transistor 71 from turning on. Therefore, the path of the reverse current 37 is through the parasitic diode 60. Because the parasitic diode 60 inherently has poor switching characteristics, the parasitic diode 60 experiences large transients when MOS device 50 is switched on or off.

To completely prevent turn on of the parasitic diode 60, the 3-component solution illustrated in FIG. 3b is often employed. In FIG. 3b, diode 69 is added to the switch to prevent any current from flowing through the parasitic diode 60, and a Schottky diode 68 is added to carry the current during the time that current flows in the direction shown in FIG. 3b, i.e., from the source side to the drain side of MOS device 50.

SUMMARY

A half bridge comprising at least one transistor having a channel that is capable in a first mode of operation of blocking a substantial voltage in at least one direction, in a second mode of operation of conducting substantial current in the at least one direction through the channel and in a third mode of operation of conducting substantial current in an opposite direction through the channel is described.

A method of operating a circuit comprising a half bridge circuit stage comprising a first transistor, a second transistor, and an inductive component, wherein the inductive component is coupled between the first transistor and second transistor, the first transistor is between a voltage source and the second transistor, and the second transistor is between a ground and the first transistor is described. The first transistor is biased on and the second transistor is biased off, allowing current to flow through the first transistor and the inductive component and blocking voltage across the second transistor. The first transistor is changed to an off bias, allowing the current to flow through the second transistor and the inductive component and causing the second transistor to be in diode mode.

A method of operating a circuit comprising an inductive component and a half bridge comprising a first transistor and second transistor, wherein the inductive component is coupled between the first transistor and second transistor and the first transistor is coupled to a voltage source and the second transistor is coupled to ground is described. The first transistor is biased off and the second transistor is biased on, allowing current to run through the inductive component and through the second transistor, wherein the first transistor blocks a first voltage. The second transistor is changed to an off bias, causing the first transistor to operate in a diode mode to carry freewheeling current and the second transistor to block a second voltage.

Embodiments of the devices and methods described herein can include one or more of the following. The half bridge can include at least two transistors and each transistor can be configured to perform as a switching transistor and as an anti-parallel diode. A bridge circuit can be formed of the half bridges described herein. A gate drive circuit can be configured to independently control a gate voltage of each of the transistors. The transistor can be a first transistor of a bridge component, the bridge component can further include a second transistor. A gate of the first transistor can be electrically connected to a source of the second transistor and a source of
the first transistor can be electrically connected to a drain of the second transistor. The first transistor can be a depletion mode device and the second transistor can be an enhancement mode device. The first transistor can be a high voltage device and the second transistor can be a low voltage device. The first transistor can be configured to block a voltage at least equal to a circuit high voltage. The second transistor can be configured to block a voltage at least equal to a threshold voltage of the first transistor. The second transistor can be configured to block a voltage of about twice the threshold voltage. The first transistor can be a high voltage depletion mode transistor and the second transistor can be a low voltage enhancement mode transistor. The first transistor can be a III-N HEMT or a SiC JFET. The second transistor can be a III-N HEMT. The second transistor can be a nitrogen face III-N HEMT. The second transistor can be a silicon based or SiC based device. The second transistor can be a vertical silicon MOSFET or a SiC JFET or a SiC MOSFET. The half bridge can include at least two of the bridge components. The second transistor can include a parasitic diode and the half bridge can include a low voltage diode connected in parallel to the parasitic diode. The low voltage diode can be configured to block at least as much voltage as the second transistor. The low voltage diode can have a lower turn-on voltage than the parasitic diode. The half bridge can include a low voltage diode, where the low voltage diode is configured to block a maximum voltage that is less than a circuit high voltage. A half bridge can consist of two transistors, wherein the transistors are each a FET, HEMT, MESFET, or JFET device. The second transistor can be an enhancement mode transistor. The transistors can be enhancement mode III-N or SiC JFET transistors. The transistors can be nitrogen face III-N HEMTs. The two transistors can have a threshold voltage of at least 2 V. The two transistors can have an internal barrier from source to drain of 0.5 to 2 V. The two transistors can have an on resistance of less than 5 mohm-cm and a breakdown voltage of at least 600 V. The two transistors can have an on resistance of less than 10 mohm-cm and a breakdown voltage of at least 1200 V. A node can be between the two transistors of each half bridge and each of the nodes can be coupled to one another by way of an inductive load. A bridge circuit including the half bridges described herein can be free of diodes. The half bridge can be free of diodes. The second transistor can be changed to an on bias after changing the first transistor to an off bias. The time between the step of changing the first transistor to an off bias and changing the second transistor to an on bias can be sufficient to prevent shoot-through currents from the high-voltage supply to ground. The time between the step of changing the second transistor to an off bias and changing the first transistor to an on bias can be sufficient to prevent shoot-through currents from the high-voltage supply to ground.

The devices and methods described herein may provide one or more of the following advantages. A switch can be formed with only a single transistor device. The transistor device can perform as either a switching transistor or as a diode. The transistor’s ability to perform the dual roles can eliminate the need for a separate anti-parallel diode in the switch. A switch including only a single transistor is a simpler device than devices that also require a diode to carry free-wheeling current. The device may be operated in a manner that keeps power dissipation to a minimum. Further, the timing and bias on the transistors can allow a device, such as a motor, formed of half bridges using single-device switches to operate in a manner that reduces the total power loss while simultaneously avoiding shoot-through currents from a high-voltage supply to ground.

Fig. 1 is a schematic of a 3-phase bridge circuit. Fig. 2a-c shows schematics and current paths when the 3-phase bridge circuit is powered. Fig. 3a-b shows schematics of MOS devices and their current paths. Fig. 4 shows a schematic diagram of a bridge circuit with single device switches. Fig. 5a-d shows schematics of current paths through single transistor switches. Fig. 6 shows a timing diagram for gate signals. Fig. 7-9 show schematics of switches that can be used in the bridge circuit of Fig. 4.

Like reference symbols in the various drawings indicate like elements.

Detailed Description

Fig. 4 shows a schematic diagram of a bridge circuit, where each of the six switches includes a single transistor device (81-86). The transistors 81-86 can be enhancement mode devices, where the threshold voltage $V_{th} > 0$, or depletion mode devices, where the threshold voltage $V_{th} < 0$. In high power applications, it is desirable to use enhancement mode devices with threshold voltages as large as possible, such as $V_{th} > 2V$ or $V_{th} > 3V$, a high internal barrier from source to drain of at least 0.5 V (such as 0.5 to 2 V), and a high access region conductivity (such as sheet resistance < 750 ohms/square) along with high breakdown voltage (600/1200 Volts) and low on resistance (< 10 mohm-cm$^2$) for 600/1200 V respectively. The gate voltages $V_{gs}$, $V_{gs}$, $V_{gs}$ for each independently controlled by a gate drive circuit. The devices 81-86 are each able to block current from flowing when the voltage at the terminal closest to ground is lower than the voltage at the terminal closest to the DC high voltage source. In some embodiments, the devices are able to block current in both directions. The devices 81-86 are also each capable of conducting current in both directions through the same conduction path/channel. Nodes 17, 18, and 19 are all coupled to one another via inductive loads, i.e., inductive components such as motor coils (not shown in Fig. 4).

Fig. 5a and 5b illustrate the operation of one of the three half-bridges of the circuit in Fig. 4 for a bridge circuit comprising enhancement mode devices which fulfill the requirements described above. For the purpose of this example, the devices are assumed to have a threshold voltage $V_{th} > 2V$. Device 84 is continuously biased on, such as by setting $V_{gs} > V_{th}$, such as $V_{gs} > V_{th} > -5V$. Device 82 is continuously biased off, such as by setting $V_{gs} < V_{th}$, such as $V_{gs} < -2V$. As shown in Fig. 5a, during the time that device 81 is biased on, such as by setting $V_{gs} > V_{th}$, such as $V_{gs} > V_{th} > -5V$, the current flows along current path 27 through device 81, through the inductive component (motor coil) 21, and through device 84. During this time the voltage at node 17 is higher than the voltage at the source of device 82 but never exceeds a high voltage (HV) value from the high-voltage supply to the circuit. Device 82 is biased off and therefore blocks a voltage $V_{gs}$ across it, where $V_{gs}$ is the voltage at node 17. As used herein, “blocking a voltage” refers to the ability of a transistor to prevent significant current, such as current that is greater than 0.001 times the operating current during regular conduction, from flowing through the transistor when a voltage is applied across the transistor. In other words, while a transistor is blocking a voltage that is applied across it, the total current passing through the transistor will not be greater than 0.001 times the operating current during regular conduction.
FIG. 5b illustrates the current path 27 during the time that device 81 is turned off, such as by setting $V_{GSH}$<sub>1</sub> ≈ $V_{DS}$, such as $V_{DSH}$≈0V. During this time the motor current flows through the channel of device 82, through the inductive component (motor coil) 21, and through device 84. Because the gate and source terminals of device 82 are both at 0V, when current flows through device 82 in this direction, device 82 effectively acts as a diode and is said to be in “diode mode”. That is, device 82 conducts current in the direction shown in FIG. 5b even when the gate of device 82 is biased below the threshold voltage of device 82, thus it behaves in the same way as a traditional transistor equipped with a reverse free-wheeling diode. The voltage $V_a$ at node 17 is negative, approximately a threshold voltage ($V_{th}$) below the source voltage of device 82, and device 81 must now block a voltage $H$<sub>2</sub>, where $H$<sub>2</sub>. Note that current/voltage blocking in one direction and diode action in the opposite direction is achieved with the same device (82).

Device 82 can be used as an actively switched device to achieve current flow in the opposite direction through the inductive component (motor coil) 21, as shown in FIGS. 5c and 5d. When device 82 is on (FIG. 5c), current 27 flows through device 82, and device 81 blocks a voltage $H$<sub>1</sub>. When device 82 is off (FIG. 5d), device 81 operates in the diode mode to carry the freewheeling current, while device 82 blocks a voltage $H$<sub>2</sub>. Thus, in the full circuit devices 81-86 perform the same function as traditional unidirectional transistors with antiparallel freewheeling diodes (61-66 in FIG. 1).

Depending on the current level and the threshold voltages of devices 81-86 (see FIG. 4), the power dissipation in the devices could be unacceptable high when operating in the diode mode. In this case, a lower power mode of operation may be achieved by applying gate signals of the form shown in FIG. 6. For example, when device 81 is switched as shown in FIGS. 5a and 5b, during the time device 82 conducts the freewheeling current (when device 81 is off), the gate of device 82 is driven high, allowing the drain-source voltage of device 82 to be simply the on-state resistance (Rds-on) times the motor current. To avoid shoot-through currents from the high-voltage supply (HV) to ground, some dead time must be provided between turn-off of device 81 and turn-on of device 82 and again between turn-off of device 82 and turn-on of device 81. The dead times are labeled “A” in FIG. 6. During these dead times, device 82 operates in the diode mode described above. Since this is a short time in comparison with the entire switching cycle, the power dissipation is not significant. Term “B” provides the dominant loss factor for device 82, and this corresponds to the low-power mode when device 82 is fully enhanced.

Referring back to FIG. 4, the diode mode of operation of devices 81-86 provides a current path at all times for the inductor current. Even if transient currents and realistic impedances are considered, the circuit will operate as desired. If, for example, the gate-drain capacitance of devices 81-86 and the source resistance of the gate drive circuit are nonzero, the high slew rate at node 17 will force the potential at the gate of device 82 below ground during the fall time of $V_a$. The result will simply be that $V_{DSH}$ is driven by the inductive component 21 to an even lower voltage than in the ideal case, but device 82 will conduct.

The devices 81-86 can be any transistor which can conduct a substantial current, such as a current at least as large as the maximum operating current of the circuit in which they are used, in both directions through the same primary channel and is capable of blocking a substantial voltage, such as a voltage larger than the circuit DC high voltage HV, in at least one direction. Each device must be capable of blocking a voltage in at least one direction which is at least between zero volts and a voltage larger than the HV, such as HV+1V, HV+5V, or HV+10V. The value of HV, and thus the range of voltages that the device must be capable of blocking, depends on the specific circuit application. For example, in some low power applications HV may be 10V, and the devices are each at least capable of blocking voltages between 0V and 10V, as well as a voltage larger than 10V, such as 11V, 20V, or 30V. In some high power applications, HV may be 1000V, and so the devices are each at least capable of blocking all voltages between 0V and 1000V, as well as a voltage larger than 1000V, such as 1100V, 1150V, or 1200V. Thus, selecting a suitable transistor capable of blocking a sufficient amount of voltage can depend on the application of the circuit. A transistor that is able to block a sufficient amount of current may allow some small amount of current to leak through the primary channel or other parts of the device than the primary channel. However, the transistor may be able to block a sufficient amount of current, which is a significant percentage of the maximum current which passes through the transistor during regular operation, such as >90%, >95%, >99% or >99.9% of the maximum current.

Examples of devices that meet these criteria are metal-semiconductor field effect transistors (MESFETs) of any material system, junction field effect transistors (JFETs) of any material system, and high electron mobility transistors (HEMTs or HFETs) of any material system, including vertical devices such as current aperture vertical electron transistors (CAVETs) as well as devices in which the channel charge has a 3-dimensional distribution, such as polarization-doped field effect transistors (POLFETs). Common material systems for HEMTs and MESFETs include GaAlIn$_{1-x}$As, InP, or III-V materials, such as III-N materials, III-As materials, and III-P materials. Common materials for JFETs include III-V materials, SiC, and Si, i.e. silicon that is substantially free of carbon. In some embodiments, the devices are enhancement mode devices (threshold voltage $V_{th}$<sub>1</sub>≈0V), while in others they are depletion mode devices ($V_{th}$<sub>1</sub>≈0).

In some embodiments, the devices 81-86 consist of enhancement mode III-nitride (III-N) devices with threshold voltages as large as possible, such as $V_{th}$<sub>1</sub>≈2V or $V_{th}$<sub>2</sub>≈3V, a high internal barrier from source to drain at 0 bias (such as 0.5-2 eV), and a high access region conductivity (such as sheet resistance <750 ohms/square) along with high breakdown voltage (at least 600 or 1200 Volts) and low on resistance (<5 or <10 mohm-cm<sup>2</sup>) for 600/1200V, respectively. In some embodiments, the devices are ferrite-oxide III-N HEMTs, such as those described in U.S. patent application Ser. No. 11/856,687, filed Sep. 17, 2007, and U.S. patent application Ser. No. 12/324,574, filed Nov. 26, 2008, both of which are hereby incorporated by reference. The devices can also include any of the following: a surface passivation layer, such as SiN, a field plate, such as a slant field plate, and an insulator underneath the gate. In other embodiments, the devices consist of SiC JFETs.

In some embodiments, device 91, illustrated in FIG. 7, is used in a half bridge or a bridge circuit in place of any or all of the devices 81-86 of FIG. 4. Device 91 includes a low-voltage E-mode transistor 92, such as a III-N E-mode transistor, connected as shown to a high voltage D-mode transistor 90, such as a III-N D-mode transistor. In some embodiments, E-mode transistor 92 is a nitrogen-face III-N device, and D-mode transistor 90 is a III-face III-N device. When E-mode transistor 92 conducts current in either direction, substantially all of the current conducted through the same primary device channel of the transistor 92. The gate of
D-mode transistor 90 is electronically connected to the source of E-mode transistor 92, and the source of D-mode transistor 90 is electronically connected to the drain of E-mode transistor 92. In some embodiments, the gate of D-mode transistor 90 is not directly connected to the source of E-mode transistor 92. Instead, the gate of D-mode transistor 90 and the source of E-mode transistor 92 are each electronically connected to opposite ends of a capacitor. The device 91 in FIG. 7 can operate similarly to a single high-voltage E-mode transistor with the same threshold voltage as that of E-mode transistor 92. That is, an input voltage signal applied to node 96 relative to node 97 can produce an output signal at node 94 which is the same as the output signal produced at the drain terminal of an E-mode transistor when an input voltage signal is applied to the gate of the E-mode transistor relative to its source. Nodes 97, 96, and 94 are hereby referred to as the source, gate, and drain, respectively, of device 91, analogous to the terminology used for the three terminals of a single transistor. When device 91 is in blocking mode, most of the voltage is blocked by the D-mode transistor 90, while only a small portion is blocked by E-mode transistor 92, as is described below. When device 91 conducts current in either direction, substantially all of the current conducts both through the channel of E-mode transistor 92 and the channel of D-mode transistor 90.

Device 91 in FIG. 7 operates as follows. When node 94 is held at a higher voltage than node 97, current flows from node 94 to node 97 when a sufficiently positive voltage (i.e., a voltage greater than the threshold voltage of E-mode transistor 92) is applied to node 96 relative to node 97, the current flowing both through the channel of E-mode transistor 92 and the channel of D-mode transistor 90. When the voltage at node 96 relative to node 97 is switched to a value less than the threshold voltage of E-mode transistor 92, such as 0 V, device 91 is blocking, blocking the voltage between nodes 97 and 94, and no substantial current flows through device 91. If the voltage at node 94 is now switched to a value less than that at nodes 97 and 96, which are being held at the same voltage, device 91 switches into diode mode, with all substantial current conducting both through the channel of E-mode transistor 92 and the channel of D-mode transistor 90. When a high voltage (HV) is applied to node 94 relative to node 97, and node 96 is biased at 0 V relative to node 97, E-mode transistor 92 blocks a voltage which is equal to or slightly larger, where Vshock is the magnitude of the threshold voltage of D-mode transistor 90. A value for Vshock can be about 5 to −10 V. The voltage at node 95 is therefore about equal to or slightly larger, therefore D-mode transistor 90 is in the OFF state and blocks a voltage which is equal to about HV minus Vshock, i.e., D-mode transistor 90 blocks a substantial voltage. When a positive voltage is applied to node 94 relative to node 97, and node 96 is biased at a voltage greater than the threshold voltage of E-mode transistor 92, such as 2Vshock, current flows from node 94 to node 97 through both the channel of E-mode transistor 92 and through the channel of D-mode transistor 90, and the voltage drop Vp across E-mode transistor 92 is much less than Vshock, such as less than about 0.2 V. Under these conditions, the voltage at node 95 relative to node 97 is Vp, and the gate-source voltage Vgshock of D-mode transistor 90 is about −Vp.

The D-mode transistor 90 can be a high voltage device capable of blocking large voltages, such as at least 600 V or at least 1200 V or other suitable blocking voltage required by the circuit applications. The D-mode transistor is at least capable of blocking a substantial voltage, such as a voltage larger than the circuit DC high voltage HV, when device 91 is in blocking mode, as described above. Furthermore, the threshold voltage Vshock of D-mode transistor 90 is sufficiently less than −Vp such that when the assembly is in the ON state, D-mode transistor 90 conducts the current flowing from node 94 to node 97 with sufficiently low conduction loss for the circuit application in which it is used. Thus, the gate-source voltage of D-mode transistor 90 is sufficiently larger than Vshock, such that conduction losses are not too large for the circuit applications. For example, Vshock can be less than −3V, −5V, or −7V, and when the gate-source voltage Vgshock of D-mode transistor 90 is about −Vp, D-mode transistor 90 is capable of conducting 10 A of current or more with less than 7 W conduction loss.

E-mode transistor 92 is at least capable of blocking a voltage larger than Vshock, where Vshock is the magnitude of the threshold voltage of D-mode transistor 90. In some embodiments, E-mode transistor 92 can block about 2Vshock. High voltage D-mode III-N transistors, such as III-N HEMTs, or SiC JFETs, can be used for D-mode transistor 90. Because the typical threshold voltage for high voltage D-mode III-N transistors is about −5 to −10 V, E-mode transistor 92 can be capable of blocking about 10-20 V or more. In some embodiments, E-mode transistor 92 is a III-N transistor, such as a III-N HEMT. In other embodiments, E-mode transistor 92 is a SiC transistor, such as a SiC JFET.

When device 91 in FIG. 7 is used in place of devices 81-86 in the bridge circuit of FIG. 4, the circuit operates as follows. Devices 81-86 will be referred to as 81'-86' when device 91 is used in place of these devices. In some embodiments, all of the devices 81'-86' are the same as one another. Even if the device are not all the same, they each have a threshold voltage greater than 0. Referring to the switching sequence shown in FIGS. 5a and 5b, when the gate-source voltages of devices 81' and 84' are greater than the threshold voltage of E-mode transistor 92, and the gate-source voltage of device 82' is less than the threshold voltage of E-mode transistor 92, such as 0 V, the current flows through the channels of both transistors of device 81' and through the channels of both transistors of device 84' from the high voltage source to ground. Device 82' blocks a voltage Vp, where again Vp is the voltage at node 17. Referring to FIG. 5b, when device 81' is switched off, the inductive component 21 forces Vp, the voltage at node 17, to a negative value and device 81' now blocks a voltage HV minus Vp. Device 82' now operates in diode mode, with current flowing through device 82' from ground to node 17. Substantially all of the current through device 82' conducts both through the channel of E-mode transistor 92 and the channel of D-mode transistor 90. When the bridge circuit is operated under the conditions shown in FIG. 5c, that is, when current flows through inductive component from node 18 to node 17, device 81' is switched off, and the gate-source voltage of device 82' is greater than the threshold voltage of E-mode transistor 92, current flows through device 82' from node 17 to ground. Substantially all of the current through device 82' conducts both through the channel of E-mode transistor 92 and the channel of D-mode transistor 90.

Thus, for the mode of operation shown in FIG. 5a, the D-mode transistor in device 82' blocks a substantial voltage, for the mode of operation shown in FIG. 5b, the D-mode transistor of device 82' conducts a substantial current flowing from source to drain through its channel, and for the mode of operation shown in FIG. 5c, the D-mode transistor of device 82' conducts a substantial current flowing from drain to source through its channel.

Referring back to FIG. 7, when device 91 operates in diode mode, the voltage at node 95 must be less than that at node 97. Therefore, the gate of D-mode transistor 90 is at a higher
The operation of Si MOS transistor 103 is different from that of E-mode transistor 92 when device 111 is in diode mode. When device 111 operates in diode mode, the voltage at node 94 is lower than that at node 97, the gate-source voltage of Si MOS transistor 103 is below threshold, and current flows from node 97 to node 94. Under these conditions, the electric field at node 95 must be less than that at node 97. Parasitic diode 101, which is forward biased, turns on and prevents the intrinsic transistor 102 from turning on. Therefore, when device 111 is in diode mode, most of the current flowing through Si MOS transistor 103 flows through parasitic diode 102 rather than through the channel of Si MOS transistor 103. However, substantially all of the current still flows through the channel of D-mode transistor 90 when device 111 is in diode mode.

When device 111 operates in diode mode, the voltage at node 95 must be less than that at node 97. Therefore, the gate of D-mode transistor 90 is at a higher voltage than the source of D-mode transistor 90 and the channel of D-mode transistor 90 is enhanced. Depending on the current level and the forward conduction characteristics of parasitic diode 101, the power dissipation in the parasitic diode 101 could be unacceptably high when device 111 operates in the diode mode. In this case, a lower power mode of operation can be achieved by applying gate signals of the form shown in FIG. 6. As an example, consider the bridge circuit of FIG. 4, but with each of the devices 81-86 replaced by device 111. In this example, the devices in the bridge circuit are referred to as devices 81'-86'. When device 81' is switched as shown in FIGS. 5a and 5b, the device 82' conducts the freewheeling current (when device 81' is off), the gate of device 82' is driven high, allowing the drain-source voltage of device 82' to be simply the effective on-state resistance (Rds-on) of device 82' times the motor current. To avoid shoot-through currents from the high-voltage supply (HV) to ground, some dead time must be provided between turn-off of device 81' and turn-on of device 82'. The dead times are labeled “A” in FIG. 6. During these dead times, device 82' operates in the diode mode described above. Since this is a short time in comparison with the entire switching cycle, the power dissipation is not significant. Time “B” provides the dominant loss factor for device 82', and this corresponds to the low-power mode when E-mode transistor 92 is fully enhanced.

In some embodiments, device 111, illustrated in FIG. 8, is used in a half bridge or a bridge circuit in place of any or all of the devices 81-86 of FIG. 4. Device 111 is similar to device 91 of FIG. 7, except that E-mode transistor 92 has been replaced with a low-voltage E-mode transistor, such as a silicon (Si) based vertical Si MOS field-effect transistor (FET) referred to herein as Si MOS transistor 103. In some embodiments, the low-voltage E-mode transistor is a SiC JFET or a SiC MOSFET. Si MOS transistor 103 has the same voltage blocking requirements as E-mode transistor 92 in FIG. 7. That is, Si MOS transistor 103 is at least capable of blocking a voltage larger than $V_{th, MOS}$, where $V_{th, MOS}$ is the magnitude of the threshold voltage of D-mode transistor 90. In some embodiments, Si MOS transistor 103 can block about $2V_{th, MOS}$. High voltage D-mode III-N transistors can be used for D-mode transistor 90. Because the typical threshold voltage for high voltage D-mode III-N transistors is about $5$ to $10$ V, Si MOS transistor 103 can be capable of blocking about 10-20 V or more.

Si MOS transistors inherently contain a parasitic diode 101 anti-parallel to the intrinsic transistor 102, as indicated in FIG. 8. Si MOS transistor 103 operates in the same way as E-mode transistor 92 when device 111 is in blocking mode as well as during standard forward conduction mode (i.e., when current flows from node 94 to node 97). That is, when a high voltage is applied to node 94 relative to node 97 and the gate-source voltage of Si MOS transistor 103 is below threshold, such that device 111 is in blocking mode, Si MOS transistor 103 blocks a voltage which is about equal to $V_{th, MOS}$ or slightly larger, with the remainder of the high voltage being blocked by D-mode transistor 90, i.e., D-mode transistor 90 blocks a substantial voltage. When the voltage at node 94 is larger than that at node 97 and the gate-source voltage of Si MOS transistor 103 is above threshold, device 111 is in standard forward conduction mode with current flowing from node 94 to node 97. Substantially all of the current conducts through the channel of Si MOS transistor 103 and through the channel of D-mode transistor 90. The voltage difference between node 95 and node 97 is between 0 V and $V_{th, MOS}$, where $V_{th, MOS}$ is the threshold voltage of D-mode transistor 90. In this mode of operation, parasitic diode 101 is reverse biased and blocks a voltage less than $V_{th, MOS}$.
parasitic diode 101. Diodes that can be used for diode 104, such as low voltage Schottky diodes, can have lower switching and conduction losses than parasitic diode 101. Consequently, conduction and switching losses during device operation can be smaller for device 112 than for device 111. Depending on the current level and the forward conduction characteristics of diode 104, the power dissipation in diode 104 could be unacceptably high when device 112 operates in the diode mode. Again, a lower power mode of operation can be achieved by applying gate signals of the form shown in FIG. 6. When the gate of device 112 is driven high while device 112 conducts the freewheeling current, the current flows primarily through the enhanced intrinsic transistor 102 rather than through diode 104, allowing the drain-source voltage of Si MOS transistor 103 to be simply the effective on-state resistance (Rds-on) of Si MOS transistor 103 times the current.

Although the device 112 in FIG. 9 does contain a diode, the diode does not need to be able to block the entire circuit DC voltage 11V, it only needs to block a voltage slightly larger than 1Vdss. Therefore, low voltage diodes can be used. This can be preferable to using the high voltage diodes which are typically included in bridge circuits, because low voltage diodes can be made to have lower switching and conduction losses than high voltage diodes. Therefore, power loss in the circuit can be reduced as compared to half bridges and bridge circuits in which high voltage diodes are used.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, a half bridge can include one switch that uses a single transistor and no diode and a second switch with a transistor and a diode. In some embodiments a half bridge consists of two transistors and does not include any diodes. In some embodiments, instead of current flowing from one half bridge through an inductor and onto a transistor of another half bridge, the current flowing out of the inductor runs to another electrical component, such as a capacitor, or directly to a ground terminal or a DC voltage supply. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:
1. A half bridge comprising at least one transistor having a gate, source, drain and channel, the device being capable in a first mode of operation of blocking a substantial voltage in at least one direction, in a second mode of operation of conducting substantial current in the at least one direction through the channel, and in a third mode of operation of conducting substantial current in an opposite direction through the channel, wherein in the third mode of operation the gate is biased relative to the source at a voltage lower than a threshold voltage of the transistor.
2. The half bridge of claim 1, wherein the half bridge includes at least two transistors and each transistor is configured to perform as a switching transistor and as an anti-parallel diode.
3. A bridge circuit comprising a plurality of half bridges of claim 1.
4. The bridge circuit of claim 3, further comprising a gate drive circuit configured to independently control a gate voltage of each of the transistors.
5. The half bridge of claim 1, wherein the transistor is a first transistor of a component, the component further comprising a second transistor having a terminal, wherein the terminal of the second transistor is connected to the first transistor.
6. The half bridge of claim 5, wherein the terminal of the second transistor is a source, the gate of the first transistor is electrically connected to the source of the second transistor, and the source of the first transistor is electrically connected to a drain of the second transistor.
7. The half bridge of claim 5, wherein the first transistor is a depletion mode device and the second transistor is an enhancement mode device.
8. The half bridge of claim 5, wherein the first transistor is a high voltage device and the second transistor is a low voltage device.
9. The half bridge of claim 5, wherein the first transistor is configured to block a voltage at least equal to a circuit high voltage.
10. The half bridge of claim 5, wherein the second transistor is configured to block a voltage at least equal to a threshold voltage of the first transistor.
11. The half bridge of claim 10, wherein the second transistor is configured to block a voltage of about 1000V.
12. The half bridge of claim 5, wherein the first transistor is a high voltage depletion mode transistor and the second transistor is a low voltage enhancement mode transistor.
13. The half bridge of claim 12, wherein the first transistor is an III-N HEMT or a SiC JFET.
14. The half bridge of claim 12, wherein the second transistor is an III-N HEMT.
15. The half bridge of claim 14, wherein the second transistor is a nitrogen face III-N HEMT.
16. The half bridge of claim 12, wherein the second transistor is a silicon based or SiC based device.
17. The half bridge of claim 16, wherein the second transistor is a vertical silicon MOSFET or a SiC JFET or a SiC MOSFET.
18. The half bridge of claim 5, wherein the half bridge includes at least two of the components.
19. A bridge circuit comprising a plurality of half bridges of claim 18.
20. The half bridge of claim 5, wherein the second transistor includes a parasitic diode and the half bridge includes a low voltage diode connected in parallel to the parasitic diode.
21. The half bridge of claim 20, wherein the low voltage diode is configured to block at least as much voltage as the second transistor.
22. The half bridge of claim 20, wherein the low voltage diode has a lower turn-on voltage than the parasitic diode.
23. The half bridge of claim 1, further including a low voltage diode having a terminal, wherein the terminal of the low voltage diode is connected to the transistor, and the low voltage diode is configured to block a maximum voltage that is less than a circuit high voltage.
24. The half bridge of claim 1, consisting of two transistors, wherein the transistors are each a FET, HEMT, MESFET, or JFET device.
25. The half bridge of claim 24, wherein the two transistors are enhancement mode transistors.
26. The half bridge of claim 25, wherein the transistors are enhancement mode III-N transistors or SiC JFET transistors.
27. A bridge circuit comprising a plurality of half bridges of claim 26.
28. The half bridge of claim 25, wherein the transistors are nitrogen face III-N HEMTs.
29. The half bridge of claim 25, wherein the two transistors have a threshold voltage of at least 2V.
30. The half bridge of claim 25, wherein the two transistors have an internal barrier from source to drain of 0.5 to 2 eV.
31. The half bridge of claim 25, wherein the two transistors have an on resistance of less than 5 mohm-cm² and a breakdown voltage of at least 600V.
32. The half bridge of claim 25, wherein the two transistors have an on resistance of less than 10 mohm-cm² and a breakdown voltage of at least 1200V.

33. A bridge circuit comprising a plurality of half bridges of claim 24.

34. The bridge circuit of claim 33, wherein a node is between the two transistors of each half bridge and each of the nodes are coupled to one another by way of an inductive load.

35. The bridge circuit of claim 33, wherein the bridge circuit is free of diodes.

36. The half bridge of claim 1, wherein the half bridge is free of diodes.

37. A method of operating a circuit comprising a half bridge circuit stage comprising a first transistor, a second transistor having a channel, and an inductive component, wherein the inductive component is coupled between the first transistor and second transistor, the first transistor is between a high-voltage supply and the second transistor, and the second transistor is between a ground and the first transistor, the method comprising:

biasing the first transistor on and biasing the second transistor off, allowing current to flow through the first transistor and the inductive component, whereby a blocking voltage is present across the second transistor; and changing the first transistor to an off bias, allowing the current to flow through the channel of the second transistor and through the inductive component.

38. The method of claim 37, further comprising changing the second transistor to an on bias after changing the first transistor to an off bias.

39. The method of claim 38, wherein the time between the step of changing the first transistor to an off bias and changing the second transistor to an on bias is sufficient to prevent shoot-through currents from the high-voltage supply to ground.

40. The method of claim 39, further comprising:
changing the second transistor to an off bias after changing the second transistor to an on bias, causing the second transistor to be in diode mode; and changing the first transistor to an on bias, allowing the current to flow through the first transistor and blocking current through the second transistor.

41. The method of claim 40, wherein the time between the step of changing the second transistor to an off bias and changing the first transistor to an on bias is sufficient to prevent shoot-through currents from the high-voltage supply to ground.

42. A method of operating a circuit comprising a half bridge comprising a first transistor and a second transistor, wherein the inductive component is coupled between the first transistor and second transistor and the first transistor is coupled to a voltage source and the second transistor is coupled to ground, the method comprising:

biasing the first transistor off and the second transistor on, allowing current to run through the inductive component and through the second transistor, wherein the first transistor blocks a first voltage; and changing the second transistor to an off bias, causing the first transistor to carry current through the channel of the first transistor and the second transistor to block a second voltage.