Silicon Evanescent Devices for Optical Networks and Buffers

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of the requirements for the degree Doctor of Philosophy
in
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by

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Hyundai Park
This thesis is dedicated to my mom, dad, and my lovely wife, Erika

... for their love and support.
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ABSTRACT

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by

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The main driver today of the silicon photonics is the quest for silicon-based optoelectronic integrated circuits which can be manufactured in state-of-art high-volume silicon fabrication facilities. Additionally, it can open up vast and significant applications of photonics in optical interconnects in board-to-board, chip-to-chip, and intra-chip communications. Raman lasers and amplifiers, high speed modulators, and photodetectors have been successfully demonstrated and have widened the applications of silicon as an optoelectronic material. However, the indirect bandgap of silicon has been a major hurdle in achieving optical gain elements. Even though many different ways have been studied such as bandgap engineering, rare earth element doping and nano-patterned silicon, an electrically pumped silicon gain element has been an unsolved challenge.

One way to address the issue of having an electrically pumped optical gain element can be hybrid integration with III-V materials including die attachment of prefabricated III-V devices on silicon waveguide circuits, hetero-epitaxial growth of III-V gain layers on silicon substrates, and wafer bonding III-V gain layers on silicon.
This thesis reports on active photonic devices fabricated with a silicon passive silicon waveguide circuit using a low temperature oxygen plasma wafer bonding process, which is referred to as the silicon evanescent device platform. This integration platform is designed with the explicit objective of providing a scalable fabrication process for high volume manufacturing, and efficient light coupling between the active devices and the passive devices.

This thesis will initially detail first demonstrations of the silicon evanescent lasers, amplifiers, and photodetectors built on the silicon evanescent device platform. Next, two different integrated photonic devices, preamplified photoreceivers and optical buffers will be presented to show the feasibility of photonic integration on the silicon evanescent device platform.
# TABLE OF CONTENTS

I. Introduction...............................................................................................................1  
  1.1. Recent Progress in Silicon Photonics..................................................3  
  1.2. Hybrid Integration...............................................................................5  
  1.3. Scope of This Thesis .........................................................................12  
  1.4. Summary ...........................................................................................15  

II. Silicon Evanescent Device Platform .....................................................................20  
  2.1. General Device Structure ..................................................................20  
  2.2. Hybrid Waveguide Design................................................................21  
  2.3. Device Fabrication ............................................................................29  
  2.4. Proof of Concept ...............................................................................37  
  2.5. Summary ...........................................................................................46  

III. Electrically Pumped Silicon Evanescent Amplifiers and Lasers .........................50  
  3.1. Device Structure................................................................................50  
  3.2. Febry-Perot Silicon Evanescent Laser ..............................................52  
  3.3. Silicon Evanescent Amplifier ...........................................................66  
  3.4. Summary ...........................................................................................74  

IV. Silicon Evanescent Photodetectors ......................................................................78  
  4.1. First generation Device .....................................................................79  
  4.2. Second generation Device.................................................................86  
  4.3. Summary ...........................................................................................91
V. Integrated Silicon Evanescent Preamplifier and Photodetector .................. 93
   5.1. Device Design ................................................................. 94
   5.2. Device Characteristics .................................................... 109
   5.3. Summary ................................................................. 123

VI. Integrated Optical Buffers ................................................................. 126
   6.1. Device Layout ................................................................. 127
   6.2. Passive Components ....................................................... 129
   6.3. Device Fabrication ........................................................... 143
   6.4. Device Characteristics ..................................................... 147
   6.5. Packet Switching Experiment ............................................. 150
   6.6. Device Performance Analysis ............................................ 154
   6.7. Summary ....................................................................... 158

VII. Conclusions ............................................................................. 164
   7.1. Thesis Summary ............................................................. 164
   7.2. Future Work ................................................................. 166

Appendix .................................................................................... 173
Chapter 1 Introduction

Since the development of the first integrated circuit in 1959 [1], silicon has been the principal semiconductor material driving the digital electronics industry. Over time, innovations in silicon processing technology have resulted in low cost electronic devices with higher speeds and smaller sizes. In fact, as of February, 2008, a 65 nm technology node has been introduced into production lines. Furthermore, a technology node less than 45 nm has already been demonstrated and is expected to be deployed within the next few years (See Fig.1.1). In addition to extremely accurate processing resolution, large volume manufacturability leading to high device yield is another key aspect of Silicon technology. Currently, the typical size of silicon wafers is 200 millimeters. However, in the near future 450 millimeter silicon wafers will be employed in production lines [2].
**Figure 1.1.** Technology node development for silicon electronics industry. A typical wafer size for each period of time is also illustrated.

The main driver today of the silicon photonics is the quest for silicon-based optoelectronic integrated circuits which can be manufactured in state-of-art high-volume silicon fabrication facilities. Additionally, it facilitates the implementation of photonic integration with electronic control and driver circuits on a single substrate. This form of photonic-electronic integration has several advantages: 1) it can improve the performance of integrated devices by placing electronics in close proximity to photonic elements. 2) It can lower manufacturing cost by eliminating unnecessary packaging cost. 3) Potentially, it can open up vast and significant applications of photonics in optical interconnects in board-to-board, chip-to-chip, and intra-chip communications to increase the communication speed between different electronic building blocks where copper wires currently impose limitations both in terms of speed and power consumption.
This chapter will start by highlighting the basic material properties of silicon and review the recent progress of silicon photonics. This will be followed by a discussion of the motivation and scope of this thesis work.

1.1 **Recent Progress in Silicon Photonics**

Figure 1.2 shows the basic properties of Silicon [3, 4]. Silicon is transparent at the 1.5 µm and 1.3 µm telecommunication wavelengths as shown in Fig 1.2(a), while it is absorptive at wavelengths shorter than 1.1 µm. Figure 1.2(b) shows the band structure of silicon. The minimum energy point of the conduction band is located at a X valley and as such is not lined up with the maximum energy of the valence band. Because of this indirect bandgap of silicon, its light generation efficiency is very low since phonon assisted non-radiative recombination dominates over radiative recombination. Radiative recombination usually occurs between two energy levels with a negligible momentum difference in the momentum-energy space.

![Figure 1.2. Basic properties of silicon (a) Absorption spectrum. The data is taken from Ref. 3. (b) Schematics of calculated band structure of crystalline silicon from Ref. 4 (not to scale).](image-url)
Because of the aforementioned material limitations of silicon, most of the research in the silicon photonics, thus far, has focused on developing photonic devices based on passive waveguide technology such as low loss waveguides, filters, and modulators.

Recently, high speed silicon modulators have been reported using free carrier plasma dispersion in Mach-Zehnder interferometer structures [10, 11], photonic crystals [12] and ring resonator structures [13]. Strained silicon has been shown to break the inversion symmetry of silicon allowing silicon to exhibit linear electro-optic refractive index modulation [14]. Recently, an electro-absorption modulator based on the quantum confined stark effect in strained silicon germanium has been demonstrated [15].

Light detection is another major research topic in silicon photonics. Strained germanium and silicon germanium push the absorption out to 1.55 µm wavelength and are attractive since they are compatible with CMOS processing technologies [16, 17]. Integration of a photodetector with an electronic receiver circuit is critical for lower capacitance and higher sensitivity [18].

As mentioned previously, the indirect bandgap of silicon has been a major hurdle in achieving optical gain elements. To overcome this problem, many different ways have been studied such as bandgap engineering, rare earth element doping and nonlinear Raman interaction. Amongst those studies, optical Raman gain from the nonlinearity of silicon crystal yielded Raman lasers and amplifiers [19, 20, 21] and optical gain from nanopatterned silicon has been observed [22]. However, those devices have to be
pumped by external laser sources. Moreover, a typical device length of the Raman laser is ~8 cm which is order of magnitude longer than a typical length of III-V lasers.

1.2 HYBRID INTEGRATION

Even though there have been a lot of studies and reports about the optical gain in silicon, an electrically pumped silicon gain element has been an unsolved challenge. One way to address the issue of having an electrically pumped optical gain element can be hybrid integration with III-V materials. This includes 1) die attachment of prefabricated III-V devices on silicon waveguide circuits, 2) hetero-epitaxial growth of III-V gain layers on Silicon substrates, and 3) wafer bonding III-V gain layers on silicon substrates.

1.2.1 Die Attachment Method

The die attachment method [23] is to take prefabricated lasers and couple them to silicon waveguides as illustrated in Fig. 1.3. Since both the III-V laser waveguide and the silicon passive waveguide are already defined, aligning those two waveguides determines the coupling loss and reflection at the interface. Typical alignment accuracy is ~1 ~0.1 µm depending on the alignment scheme. A coupling loss of 4~5 dB between an amplifier and a passive waveguide is reported [24]. A multi-channel transmitter integrated with CMOS driving electronics has been demonstrated using this technique [25]. However, due to the tight alignment tolerances of the optical modes and the need to align each laser individually, this method has limited scalability, and it is difficult to envision die attaching more than a few lasers to each chip without prohibitive costs.
Furthermore, the reflections at the chip interfaces limit the gain and spectral flatness that can be achieved.

![Figure 1.3. Die attachment method (in-plane coupling scheme).](image)

### 1.2.2 Hetero Epitaxial Growth

The hetero epitaxial growth technique enables the creation of monolithically grown III-V gain layers on silicon substrates. However, the large lattice mismatch between III-V materials and silicon (8% between InP and Si, 4% between GaAs and Si) frequently requires a thick buffer layer prior to growing quantum wells or quantum dot layers [26] albeit a buffer-less growth technique has been reported recently [27]. The demonstrations include InGaAs quantum dot lasers [26] and InGaSb quantum well lasers [27] fabricated on a silicon substrate as shown in Fig.1.4. These demonstrations have widened the possibility of building monolithically integrated on-chip laser sources on the silicon photonics platform. However, an efficient coupling scheme from the III-V lasers to the silicon waveguide needs to be developed since the lasing optical mode lies in the III-V layers.
1.2.3 Wafer Bonding Technique

The wafer bonding technique is another way to transfer III-V epitaxial layers to silicon substrate. The work presented in this thesis falls into this approach. In general, the wafer bonding technique has been widely used to combine the advantages of different material systems with a large lattice mismatch. It has been reported that wafer bonding generates misfit dislocations from the lattice mismatch only in the bonded interface without adding threading dislocations in transferred epitaxial layers [28]. Figure 1.5 illustrates the wafer bonding technique.
Figure 1.6 categorizes several wafer bonding techniques and summarizes important demonstrations. High brightness LEDs are one application of direct wafer bonding. AlGaInP light emitting layers are first grown on a lattice matched GaAs substrate and then transferred to a GaP substrate. GaP substrates are transparent at emission wavelengths of AlGaInP and result in improved luminous efficiency [29]. VCSELs operating at 1.5 µm have been reported by bonding high reflectivity GaAs based DBR mirrors to InP based gain layers in order to circumvent the poor quality of InP based DBR mirrors [30]. Wafer bonding of silicon with III-V compound semiconductors has produced various photonic devices as well. For instance, wafer bonding between InGaAs layer and Silicon has yielded APDs with high gain bandwidth products [31]. Additionally, III-V lasers fabricated on Silicon substrates have demonstrated the feasibility of optoelectronic integration on a Silicon substrate [32].
Figure 1.6. Categories of wafer bonding techniques.
The examples mentioned above fall into the category of direct wafer bonding; implying that two materials are bonded covalently without an interfacial layer. Typically this direct bonding process requires a high annealing temperature in the range of 600 ~ 700 °C, to form strong covalent bonds. In the case of direct bonding of silicon and InP, the thermal expansion coefficient mismatch between silicon (2.6 x 10^{-6} K^{-1}) and InP (4.8 x 10^{-6} K^{-1}) can induce thermal stress that accumulates resulting in cracking or significant bowing. The largest reported size of a direct wafer bonded sample between silicon and epitaxial layers grown on an InP substrate is ~3x3 cm^2 [33], and even this requires substrate thinning and sophisticated surface preparation procedures prior to a high temperature anneal.

Therefore, a low temperature annealing step is preferable when bonding two material systems that have a large thermal expansion coefficient mismatch. An interfacial layer such as an oxide or benzocyclobutene (BCB) is widely employed to enable low temperature wafer bonding. An oxide layer has a highly hydrophilic surface which facilitates the formation of strong covalent bonds even at low temperatures in the range of ~250 °C~ 400 °C. From a commercial standpoint, the most important application of oxide meditated wafer bonding is to manufacture silicon-on-insulator (SOI) wafers. The top silicon layer of a SOI wafer is created by polishing or exfoliating a top silicon substrate after bonding two silicon substrates with oxide layers grown on surfaces. Oxide meditated wafer bonding of silicon and III-V compound semiconductors have demonstrated III-V microdisk lasers on a silicon substrate [35].
Figure 1.6 also shows a wafer bonding technique using oxygen plasma treatment [36]. This bonding process falls into an intermediary category somewhere between direct wafer bonding and oxide wafer bonding. The surfaces of the two materials are treated with low power oxygen plasma. This oxygen plasma creates a very thin layer of oxide on the surfaces, whose properties are different from the native oxide. The oxide layer created by the plasma has more dangling bonds and a smoother surface leading to the formation of very strong covalent bonds even at a low anneal temperatures in the range of 250 ~300 °C. The work presented in this thesis uses the oxygen plasma wafer bonding process. The details of the bonding mechanism and process flow will be discussed in Chapter 2.

Since a very thin amorphous layer of different materials’ oxide is created at the bonded interface (~10 nm), the bonded interface is insulative. Alternatively, it has been reported that B₂H₆ plasma treatment leaves a conductive bonding interface highly doped with Boron (B) after low temperature anneal [37].

Wafer bonding using an adhesive layer is also being investigated. The adhesive layer is spun on the sample surface, and is cured after two substrates are brought in contact. Since the adhesive layer planarizes the surface, this bonding is less sensitive to surface roughness and defects compared to other approaches. III-V lasers [38] and photodetectors [39] on silicon have been demonstrated using this technique. However, since the adhesive layer has a thickness of ~0.1 ~ 1 µm with a refractive index of ~1.5, efficient light coupling from III-V devices to passive silicon waveguides needs to be developed.
1.3 **SCOPE OF THIS THESIS**

This thesis reports on active photonic devices fabricated with a silicon passive silicon waveguide circuit, using an oxygen plasma wafer bonding process. We refer to this integration platform as the *silicon evanescent device platform*. This integration platform is designed with the explicit objective of providing: 1) a scalable fabrication process for high volume manufacturing, and 2) efficient light coupling between the active devices and the passive devices.

Initial development of this new device platform was carried out collaboratively with another graduate student, Alex Fang. After the first demonstration of the electrically pumped FP lasers, the direction of this research has been divided into two different paths: 1) advanced silicon evanescent devices (this work) and 2) advanced silicon evanescent lasers (Ref. 40).

This thesis will initially detail first demonstrations of the silicon evanescent lasers, amplifiers, and photodetectors built on the silicon evanescent device platform. Next, two different integrated photonic devices, preamplified photoreceivers and optical buffers will be presented to show the feasibility of photonic integration on the silicon evanescent device platform.

Figure 1.7 shows the basic structure of the silicon evanescent devices. Silicon waveguides are first fabricated and then III-V layers are bonded forming a hybrid waveguide structure. The optical mode in this waveguide is confined by both the silicon waveguide and the III-V layers. By designing the silicon waveguide dimensions correctly, the optical mode can be mostly confined in the silicon waveguide with a small
portion of the mode coupled to the III-V layers. Through the mode overlap with the III-V layers, the optical mode can be amplified or absorbed efficiently while simultaneously maintaining efficient mode coupling to a silicon passive waveguide. This is due to the fact that the III-V optical mode is already very close to the mode of the silicon passive silicon waveguide. The oxygen plasma wafer bonding process is chosen to build this device platform because it allows a low temperature anneal which doesn’t destroy the silicon circuits fabricated prior to the bonding process and also preserves the quality of III-V layers by minimizing thermal stress.

![Diagram](image)

**Figure 1.7.** General structure of silicon evanescent devices.

Figure 1.8 shows the flow of this thesis. Chapter 2 discusses the general concept, the design, and fabrication of devices. The basic mechanism of the low temperature oxygen plasma wafer bonding process is overviewed. The first optically pumped silicon evanescent lasers as a proof of concept is presented at the end of the chapter.

Chapter 3 and 4 presents the first demonstrations of electrically driven silicon evanescent discrete devices. The first electrically pumped lasers and amplifiers are
presented in Chapter 3 including discussions about the thermal characteristics of the
devices. Chapter 4 presents the first photodetectors built on the same device structure as
the lasers and amplifiers.

Chapter 5 presents integrated preamplified receivers. The design issues of the
interface between the hybrid waveguide and silicon passive waveguide are explored.
Next, the high speed detector design is discussed followed by the characteristics of the
fabricated device.

Chapter 6 deals with integrated optical buffers. Theory for the passive silicon
waveguide loss is investigated and compared with the measurements results from the
fabricated silicon waveguides. After characterizations of individual components
implementing the integrated optical buffer, the integrated optical buffer operating at 40
Gb/s is demonstrated. The device model is developed to understand the limitations of
the current performance and several ways to improve the device performance are
discussed.

Finally, chapter 7 concludes this dissertation and discusses several directions for
future work.

1.4 SUMMARY

This chapter gives a brief overview of current research trends in the field of
silicon photonics. Recent research in silicon photonics has been motivated by well
developed silicon processing technology but silicon based active photonic devices such
as lasers and amplifiers are an unsolved problem because of the indirect bandgap of
silicon. In this chapter we introduce the silicon evanescent device platform as a viable solution to building active photonic devices on silicon. In the research literature, various hybrid integration techniques have been proposed but each approach has issues associated with either scalability or efficient light coupling from the active devices to the passive silicon waveguides. The work presented in this thesis is motivated by a desire to build a device platform based on silicon that is scalable and allows for efficient light coupling from active devices to the passive silicon waveguides. As will be shown in the later chapters, this device platform can be a solution to build highly functional photonic integrated circuits on silicon for applications such as optical interconnects and data communications.

![Figure 1.8. Outline of this thesis.](image)
1.5 References


Chapter 2  Silicon Evanescent Device Platform

This chapter describes the general structure of the hybrid silicon evanescent device platform, the theoretical concepts, and the fabrication issues that form the basis for the work in this dissertation. First, the hybrid waveguide structure and its general design concepts are discussed. Next, the general fabrication procedure of the hybrid device structure including the low temperature wafer bonding process and III-V back-end process is outlined. Finally, the first results from optically pumped hybrid silicon evanescent lasers are presented as a proof of concept of this hybrid integration platform.

2.1 General Device Structure

Figure 2.1 shows the general cross sectional device structure of hybrid silicon evanescent devices. The hybrid waveguide structure is comprised of III-V layers bonded to a silicon waveguide fabricated on a SOI wafer. The mesa structure formed on the III-V region enables current flow through the multiple quantum well region. In general the III-V layers consist of a p-type contact layer, a p-type cladding, a p-type separate confinement heterostructure (SCH) layer, an undoped multiple quantum well layer (MQW), a n-type contact layer, and a n-type superlattice (SL).
Amplifiers and lasers have a wide III-V mesa (12 ~14 µm) for better heat conduction and mechanical strength as shown in Fig. 2.1(a) while a narrow III-V mesa (2 ~4 µm) is chosen for detectors and modulators for high speed operation with a reduced capacitance as shown in Fig. 2.1(b). The optical mode in this hybrid waveguide lies both in the silicon waveguide and the multiple quantum well layers. Consequently, the hybrid waveguide structure has two important waveguide design parameters: 1) silicon confinement factor and 2) quantum well confinement factor. The quantum well confinement factor is a critical design parameter in order to achieve enough optical gain and absorption while the silicon confinement factor is an important parameter determining coupling efficiency when the device is integrated with silicon passive devices. The two confinement factors of the hybrid waveguide can be manipulated by changing the silicon waveguide dimensions.

**Figure 2.1.** Cross sectional structure of hybrid silicon-evanescent devices with (a) a wide III-V mesa for amplifiers and lasers (b) a narrow III-V mesa for detectors.

### 2.2 HYBRID WAVEGUIDE DESIGN

Table 2.1 summarizes the III-V epitaxial layer structure initially grown on an InP substrate. The MQW region consists of eight 7 nm thick 1.7 µm quaternary...
(1.7Q)Al_{0.055}Ga_{0.292}In_{0.653}As quantum wells under compressive strain (0.85 %) and 10 nm thick 1.3Q Al_{0.089}Ga_{0.461}In_{0.45}As barriers under tensile strain (-0.55 %). The photoluminescence peak of the quantum wells is designed to be 1545 nm. The quantum wells are compressively strained to split the heavy hole and the light hole valence bands and to reduce the density-of-states in the valence band leading to a reduction of transparency carrier density. Barriers have tensile stress to balance the net strain close to zero [1].

**Table 2.1. III-V epitaxial layer structure.**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Doping (cm^{-2})</th>
<th>Thickness(nm)</th>
<th>n @ 1550nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>p contact</td>
<td>In_{0.53}Ga_{0.47}As</td>
<td>p type, 1x10^{19}</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Cladding</td>
<td>InP</td>
<td>p type, 1x10^{18}</td>
<td>1500</td>
<td>3.1681</td>
</tr>
<tr>
<td>SCH</td>
<td>Al_{0.131}Ga_{0.34}In_{0.528}As</td>
<td>p type, 1x10^{17}</td>
<td>250</td>
<td>3.4564</td>
</tr>
<tr>
<td>MQWs</td>
<td>Al_{0.089}Ga_{0.461}In_{0.45}As (9x)</td>
<td>undoped</td>
<td>10</td>
<td>3.5309</td>
</tr>
<tr>
<td></td>
<td>Al_{0.055}Ga_{0.292}In_{0.653}As (8x)</td>
<td>undoped</td>
<td>7</td>
<td>3.5387</td>
</tr>
<tr>
<td>n contact</td>
<td>InP</td>
<td>n type, 1x10^{18}</td>
<td>110</td>
<td>3.1681</td>
</tr>
<tr>
<td>SL</td>
<td>In_{0.83}Ga_{0.15}As_{0.327}P (2x)</td>
<td>n type, 1x10^{18}</td>
<td>7.5</td>
<td>3.2818</td>
</tr>
<tr>
<td></td>
<td>InP (2x)</td>
<td>n type, 1x10^{18}</td>
<td>7.5</td>
<td>3.1681</td>
</tr>
<tr>
<td>bonding</td>
<td>InP</td>
<td>n type, 1x10^{18}</td>
<td>10</td>
<td>3.1681</td>
</tr>
</tbody>
</table>

An unstrained 1.3Q Al_{0.131}Ga_{0.34}In_{0.528}As SCH layer is placed above the MQW layer. A two period InP/1.1Q In_{0.85}Ga_{0.15}As_{0.327}P superlattice (SL) is employed below the 110 nm thick InP spacer layer. The SL region has 7.5 nm thick alternating layers of InP/InGaAsP to inhibit the propagation of defects from the bonded interface to the QW region [2]. Finally a 10 nm thick InP spacer is used as a bonding interface to silicon. The refractive index of each layer is calculated from the dielectric constants for strained layers [3]. Material parameters of the quaternary
layers (AlGaInAs, and InGaAsP) are calculated by interpolation using Vegard’s law with binary material parameters of InAs, AlAs, GaAs and GaP [4].

Figure 2.2 shows the index profile in the vertical direction of the hybrid waveguide consisting of a silicon waveguide and III-V layers. The refractive indices of the MQW and SL regions are weight-averages taking into account the thickness of each layer to reduce the computation time [5]. As can be seen in the mode profile superimposed in the figure, the typical silicon confinement factor ($\Gamma_{Si}$) in this work is in the range of 70 ~ 80 % while the quantum well confinement factor ($\Gamma_{QW}$) is in the range of 2 ~ 4 %.

Figure 2.2. Index profile of the hybrid waveguide in the vertical direction with a typical fundamental mode profile.

The optical mode overlap with each region is dependent on the refractive index and thickness of the III-V layers as well as the silicon waveguide dimensions.
The confinement factors with different III-V layer thickness and silicon waveguide dimensions are calculated using the Beamprop™ mode solver, and the results are shown in Fig. 2.3.

**Figure 2.3.** Calculated confinement factors of the fundamental TE mode with different silicon waveguide heights (a) as a function of silicon waveguide width, SCH thickness=0.25 μm, n type layer thickness=0.15 μm, active region=0.146 μm (8 QWs) (b) as a function of active region thickness, SCH thickness=0.25 μm, n type layer thickness=0.15 μm, silicon waveguide width=2.0 μm (c) as a function of SCH thickness, n type layer=0.15 μm, active region=0.146 μm (8 QWs), silicon waveguide width=2.0 μm (d) as a function of n type layer thickness, SCH thickness=0.25 μm, active region=0.146 μm (8 QWs), silicon waveguide width=2.0 μm. (The typical waveguide design used in this work is indicated as arrows in the figure.)
In general, with a fixed set of III-V layers, the silicon confinement factor increases as the height or width of the silicon waveguide increases while the quantum well confinement factor decreases as shown in Fig. 2.3(a). The confinement factor variation with different III-V layer thicknesses is shown in Fig. 2.3(b), (c) and (d). The SCH layer and active region have a higher refractive index than silicon, hence, increasing their thickness results in the optical mode being pushed into the III-V region (Fig. 2.(b) and (c)). Consequently, the quantum well confinement factor increases. It is important to note that the n-type layers (InP and SL), which are placed between high index III-V layers and a silicon waveguide, have a lower refractive index. As a result, thick n type layers decouple the III-V layers from the silicon waveguide. As shown in Fig. 2.3(d), for 0.7 µm or 0.9 µm silicon waveguide height, the silicon confinement factor increases with thicker n type layers because the fundamental TE mode becomes close to a passive silicon waveguide mode. However, it decreases for a 0.5 µm silicon waveguide height because the fundamental TE mode becomes similar to an optical mode solely guided by III-V layers.

Figure 2.4 shows the two dimensional mode profiles with different silicon waveguide widths and III-V layers as specified in Table 2.1. The left mode profile (a 1 µm wide silicon waveguide) is similar to the center quantum well design with a higher quantum well confinement factor while the right mode profile (a 2 µm wide
silicon waveguide) is similar to an offset quantum well design. Understanding the parameters that control the mode profile is important for designing devices for a wide range of applications. For example, a lower quantum well confinement factor is preferable for better saturation characteristics in amplifiers and photodetectors while a larger confinement factor can provide higher optical gain and absorption in lasers, amplifiers and photodetectors. Moreover, multi-stage amplifiers and detectors can be realized by tapering the silicon waveguide width to achieve high gain or absorption with high saturation power [6].

![Figure 2.4](image)

**Figure 2.4.** Calculated two dimensional mode profiles with different silicon waveguide widths of (a) 1.0 µm, (b) 1.25 µm and (c) 2.0 µm. The silicon waveguide height and the slab height is fixed at 0.7 µm and 0.1 µm respectively.

In addition to the optical mode profile, the electronic band structure of the III-V layers is also important in order to supply electrons and holes into the active region with minimal leakage. Holes injected from the top of the III-V mesa, flow through the p type cladding and SCH layer and recombine with electrons which flow laterally through the n type InP and SL layers. The doping concentration of each layer is designed to keep additional free carrier loss from each layer to less than 1
cm\(^1\) while ensuring the electrical resistance is low enough to minimize the series resistance of the PIN diode. Table 2.2 summarizes the material parameters used in the simulations. These include the mobility of majority carriers, bandgap energy, conduction band offset and valence band offset. The n type bottom layer is chosen to be InP since the high electron mobility of InP enables the flow of current laterally through the thin layer without a significant voltage drop. The thickness of the n type InP layer also affects the efficiency of the optical gain and absorption since, in general, a thicker InP layer results in decreasing the quantum well confinement factor because of its lower index (3.17). Consequently, there is a trade-off between the electrical resistance and the quantum well confinement factor. For this work, the total thickness of n layers is chosen to be 150 nm.

Table 2.2. Material parameters of the III-V layers used in the simulations. The band gaps and the band offsets are provided by Landmark, Inc. Other values are taken from Ref. [7, 8, 9, 10]. Note that the heavy hole effective masses of the wells and the barriers are assumed to be the same as InGaAsP materials with the same bandgap energies.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>(E_g) (eV)</th>
<th>(\Delta E_c) (eV)</th>
<th>(\Delta E_v) (eV)</th>
<th>(\mu) (cm(^2)/Vs)</th>
<th>(m_c)</th>
<th>(m_{hh})</th>
</tr>
</thead>
<tbody>
<tr>
<td>p contact</td>
<td>InGaAs</td>
<td>1.35</td>
<td>0</td>
<td>0</td>
<td>p, 100</td>
<td>0.077</td>
<td>0.61</td>
</tr>
<tr>
<td>Cladding</td>
<td>InP</td>
<td>0.9539</td>
<td>0.1111</td>
<td>0.2851</td>
<td>p, 50</td>
<td>0.061</td>
<td>0.42</td>
</tr>
<tr>
<td>SCH</td>
<td>AlGaInAs</td>
<td>0.9539</td>
<td>0.1274</td>
<td>0.2689</td>
<td>50</td>
<td>0.061</td>
<td>0.42</td>
</tr>
<tr>
<td>MQWs</td>
<td>AlGaInAs (9x)</td>
<td>0.7411</td>
<td>0.2352</td>
<td>0.3737</td>
<td>50</td>
<td>0.057</td>
<td>0.37</td>
</tr>
<tr>
<td></td>
<td>AlGaInAs (8x)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n contact</td>
<td>InP</td>
<td>1.35</td>
<td>0</td>
<td>0</td>
<td>n, 2100</td>
<td>0.077</td>
<td>0.61</td>
</tr>
<tr>
<td>SL</td>
<td>InGaAsP (2x)</td>
<td>1.274</td>
<td>0.1060</td>
<td>0.1170</td>
<td>n, 2100</td>
<td>0.065</td>
<td>0.46</td>
</tr>
<tr>
<td></td>
<td>InP (2x)</td>
<td>1.35</td>
<td>0</td>
<td>0</td>
<td>n, 2000</td>
<td>0.077</td>
<td>0.61</td>
</tr>
<tr>
<td>bonding</td>
<td>InP</td>
<td>1.35</td>
<td>0</td>
<td>0</td>
<td>n, 2100</td>
<td>0.077</td>
<td>0.61</td>
</tr>
</tbody>
</table>

Figure 2.5(a) shows the calculated profile of the current density (A/cm\(^2\)) at a forward bias of 2 V using a two dimensional drift-diffusion simulator, Silvaco\(^{TM}\)
based on the finite element method. The detailed dimensions are embedded in the same figure. The arrows and contours represent the direction and magnitude of the current density. Band diagram and carrier densities at the same forward bias voltage in the vertical direction are shown in Fig. 2.5(b). The figure shows that a carrier density of $\sim 5 \times 10^{18}$ cm$^{-3}$ can be supplied with a variation of $< 20\%$ through the eight wells. Figure 2.5(c) shows the lateral carrier distribution in the x direction. As shown in the figure, the optical mode in the active region is confined to the 4 µm wide region and this ensures that the optical gain is evenly distributed in the region where the optical mode overlaps. The optical mode in the active region is calculated with the silicon waveguide dimensions used for the simulations in Fig. 2.4(c). The current channel width can be further optimized to achieve maximum overlap between carrier distribution and the optical mode. The estimated series resistance of this structure is $\sim 2778$ ohms-µm (i.e. $\sim 2.778$ ohms for a 1000 µm long device) as shown in Fig. 2.5(d).
Figure 2.5. (a) Calculated profile of the current density at 2 V. Upper part of cladding is omitted in this figure for better illustrations. (arrows) direction (contours) magnitude (b) Band diagrams (top) and carrier densities (bottom) in the vertical direction (c) Carrier densities in the lateral direction (d) IV characteristics of a 1 mm long device. The temperature is assumed to be 300 K.

2.3 DEVICE FABRICATION

2.3.1 Oxygen plasma assisted wafer bonding process

The transfer of the III-V epitaxial layer structure to a SOI substrate is a key step in the fabrication of this hybrid platform and has direct impact on the device performance, yield and reliability. Due to the mismatch between the thermal expansion coefficient of silicon and InP ($\alpha_{\text{Si}} = 2.6 \times 10^{-6} / \text{K}$, $\alpha_{\text{InP}} = 4.8 \times 10^{-6} / \text{K}$), a
high temperature anneal (typically > 400 °C), can easily cause cracks or deformation of the III-V layers. Figure 2.6(a) shows a Nomarski microscope surface image of III-V epitaxial layers bonded to a SOI substrate through direct wafer bonding at 600 °C. Surface deformation can clearly be seen in this picture which can lead to degradation of material quality as well as affecting the scalability of the process due to the accumulation of stress over larger sample sizes. In order to address this issue, an oxygen plasma surface treatment process is incorporated to enable a low temperature anneal [11]. An anneal temperature of 300 °C is chosen to minimize thermal mismatch stress while still being able to convert the weak Van der Waals bonds formed by the room temperature bonding to strong covalent Si-O-In and Si-O-P bonds. Figure 2.6(b) shows smooth surface morphology of InP epitaxial layers after this low temperature wafer bonding process. It is noteworthy that the residual thermal mismatch stress still exists even after the low temperature anneal and can affect the device reliability. Therefore, the gradient of the thermal mismatch stress in the bonded structure and its effects on the device performance such as photoluminescence (PL) peak change need to be investigated further.
**Figure 2.6.** Nomarski microscope surface images of the transferred III-V layers at bonding temperatures of (a) 600 °C (b) 300 °C.

**Figure 2.7.** Process flow of the low temperature oxygen plasma assisted wafer bonding process.
Figure 2.7 is the process flow of the oxygen plasma assisted low temperature wafer bonding. After thorough sample cleaning to ensure the surfaces are particle free, the native oxide on SOI and InP are removed in standard buffered HF solution and NH₄OH, respectively, resulting in clean, hydrophobic surfaces. The samples then undergo an oxygen plasma surface treatment to grow an ultra-thin layer [11]. The Si-O-Si bonds of the oxide (SOI side) are found to be more strained than conventional oxides formed with a standard RCA-1 cleaning process or other hydrophilic wet-chemical treatment processes, and have a higher readiness to break and form new bonds. The subsequent deionized water dip further terminates the oxide surface with polar hydroxyl groups OH⁻ forming bridging bonds between the mating surfaces resulting in spontaneous bonding at room temperature. To strengthen the bond, the bonded sample is annealed at a pressure of 1.5 MPa and a temperature of 300 °C, for typically 12~18 hours.

The chemical reactions occurring during the annealing can be divided into two steps as shown in Eq. 1 and 2 [12].

\[
\text{Si-OH + OH-M} \rightarrow \text{Si-O-In (or P)} + \text{H}_2\text{O} \quad \text{Eq. 2.1}
\]

\[
\text{Si} + \text{H}_2\text{O} \rightarrow \text{SiO}_2 + \text{H}_2 \quad \text{Eq. 2.2}
\]

Along with Si-O-In and Si-O-P group, the first step generates H₂O which in turn oxidizes the silicon surface producing SiO₂. As mentioned in Ref. 11, the bonded interface may consist of the different oxide group of Si-O-In, Si-O-P and
SiO$_2$. However, further investigations on the interfacial layer using transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) need to be carried out to study its thickness and compositions.

The hydrogen generated as a byproduct should be diffused out of the interface efficiently. The hydrogen diffusion process is typically slow and this requires significantly longer anneal time than the conventional direct bonding processes (typical anneal time of ~1 hour). In order to expedite the hydrogen diffusion, etched trenches on the silicon wafer as bonding channels are incorporated. Without bonding channels, it is found that the hydrogen can be trapped at the interface and forms micro bubbles resulting in lower device yield. Additionally, the hydrocarbon from a non-perfect surface cleaning procedure can be a bubble source congregating hydrogen and generating hydrocarbon gas such as CH$_4$ [13]. In this work, the silicon waveguide trenches are utilized as bonding channels and ozone cleaning is incorporated as a final sample cleaning step to minimize the hydrocarbon contaminations. Figure 2.8 clearly shows the effect of bonding channels on the formation of micro bubbles. The bubble density is ~30,000 mm$^{-2}$ (Fig. 2.8(a)) and ~1200 mm$^{-2}$ (Fig. 2.8(b)) without and with bonding channels on the silicon, respectively. Moreover, as shown in Fig. 2.8(b), the bubbles are generated only in the region with coarser channel spacing (~50 µm) not in the region with a denser channel spacing (~13 µm).
2.3.2 Silicon waveguide and III-V backend processing

This section will describe the general procedure of the silicon waveguide formation on a SOI wafer and III-V back-end processing after the wafer bonding process. The silicon waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate using Cl₂/Ar/HBr-based plasma reactive ion etching. The thickness of the buried oxide (BOX) is 1 µm~2 µm for this work. The III-V epitaxial layer is then transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding which is described in the previous section. After removal of the InP substrate using HCl: H₂O (3:1), mesa structures on III-V layers are formed by dry etching the p type layers using a CH₄/H₂/Ar-based plasma reactive ion etch. Two different hard masks are used for the III-V mesa etching process in this work. Silicon nitride hard mask is used for fabricating the first generation lasers, amplifiers and photodetectors (Chapter 3 and
4) while Pd/Ti/Pd/Au metal layers are used for the second generation amplifiers, photodetectors and optical buffers (Chapter 5 and 6). The metal hard mask enables a self-aligned process between the p contact metal and p III-V mesa leading to efficient current injection in laterally tapered III-V mesas. Subsequent wet-etching of the quantum well layers to the n type layers is performed using H₃PO₄:H₂O₂:H₂O (1:5:15). Ni/AuGe/Ni/Au alloy contacts are deposited onto the exposed n type InP layer. Pd/Ti/Pd/Au p contacts (Ti/Au in the self aligned process) are then deposited on the center of the mesas. For lasers and amplifiers, protons (H⁺) are implanted on the two sides of the p type mesa to create a 4 µm wide current channel and to prevent lateral current spreading, ensuring a large overlap between the carriers and the optical mode. Ti/Au probe pads are then deposited on top of the mesa. Then, if necessary, the sample is diced into several bars and each bar is polished. Two different types of the III-V back-end processing are illustrated in Fig. 2.9(a) and (b).
Figure 2.9. Fabrication procedures (a) Silicon nitride hard mask process (b) Self aligned process. Some of the process details are not shown here and are described in the process follower in Appendix 1.
2.4 **Proof of Concept: Optically Pumped Hybrid Silicon Evanescent Lasers**

In order to prove the concept of the hybrid waveguide architecture, the first fabricated devices were optically pumped hybrid silicon evanescent lasers. The III-V layers for the optically pumped lasers are homogenous through the entire device without going through any III-V processing steps and have a slightly different epitaxial structure from the structure specified in Table 2.1 to enable the optical pumping. The III-V epitaxial layers have a thicker top SCH layer (0.5 µm) and additional bottom SCH layer (0.05 µm) to increase the absorption efficiency of the pump light. Also five quantum wells are used and all the layers are undoped except for the n type 10 nm thick InP bonding interface layer. Figure 2.10(a) shows the structure of the device.

![Figure 2.10](image)

**Figure 2.10.** (a) Device structure of the optically pumped hybrid laser (b) a SEM image of one of the fabricated device.

After the bonding process and subsequent InP substrate removal, the sample is diced into several bars and then the facets of each bar are polished to form the laser cavity. The polished facets are coated with a broadband dielectric high reflection
(HR) coating consisting of three periods of SiO₂/Ta₂O₅ with a reflectivity of approximately 80 %. A scanning electron microscope (SEM) image of one of the fabricated device prior to applying HR coating is shown in Fig. 2.10(b).

2.4.1 First generation devices-Pulsed operation

The first generation devices are fabricated with a silicon waveguide height, width and slab height of 0.97 µm, 1.3 µm, and 0.19 µm respectively. The resulting hybrid structure supports a fundamental TE mode with a silicon confinement factor of 42.8 % and a quantum well confinement factor of 3.6 % for five quantum wells. The final device length after dicing and polishing is 600 µm. The BOX layer thickness is 0.5 µm.

The devices are optically pumped perpendicular to the laser by a 980 nm diode laser. The light from the pump laser is focused by a cylindrical lens illuminating a 10 µm by 916 µm rectangular spot incident on the device through the top InP cladding layer (See Fig.2.11). The pump laser is operated pulsed to increase the pump power. The coupled pump power to the device was determined by factoring out the reflected pump power (~40 %) and calculating the overlap of the pump beam with the laser mode. The laser output is collected with a fiber from the waveguide and subsequently characterized using a spectrum analyzer and photodetector. The fiber coupling efficiency is experimentally measured to be -5dB. The transverse electric (TE) and transverse magnetic (TM) near-field images of the output mode are
recorded on an IR camera through a polarizing beam splitter and an 80x lens at the opposite waveguide facet.

**Figure 2.11.** Block diagram of the test setup for optically pumped silicon evanescent lasers.

Figure 2.12 shows the pulsed output power collected by a lensed fiber through a single facet as a function of average pump power and temperature. The threshold increases from 30 to 50 mW between 12 °C and 20 °C and the structure exhibits a temperature coefficient (T₀) of 18 K. This low T₀ is largely due to the lack of carrier confinement structure in the 0.5 µm thick absorber layer. The maximum output power of 1.4 mW is limited by the available maximum power of the pump laser. The single output differential quantum efficiency is approximately 3.2 % at 12 °C, and the total efficiency taking into account the light from both facets and the coupling losses of 5 dB is approximately 20 %. The lasing mode is predominantly TE.

It is important to note that lasing only occurs in the optical mode defined by the silicon waveguide region. In other words, slab modes in the III-V region do not
support lasing. This can be seen from the inset of Fig. 2.12, which compares the light output for pumping in the two regions. This can also be seen by translating the pump beam across the rib waveguide. The optical output power drops with a FWHM of 6 µm wider than the width of the rib, as expected from the finite pump beam width of 10 µm.

![Figure 2.12. Single-sided fiber-coupled pulsed output power of the first generation device as a function of pump power for several temperatures.](image)

**2.4.2 Second generation devices-CW operation**

The second generation devices are fabricated with several changes to achieve continuous wave operation. First, the silicon waveguide dimensions are modified with a lower height to increase the quantum well confinement factor. Second, the fabrication process including the silicon waveguide formation and the wafer bonding is optimized to achieve a low loss waveguide and a high device yield. Additionally,
the thickness of the BOX layer is increased to 1 µm in order to minimize the radiation loss through the substrate. Finally, a 1250 nm fiber laser with a maximum output power of 2 W is used to pump the devices, since the previous L-L measurements were limited by the available output power of a 980 nm pump laser. The spot size of this laser is 12 µm by 917 µm. The final device length after dicing and polishing is 800 µm. The fabricated device dimensions of the silicon waveguides are a height of 0.7 µm and a slab height of 0.1 µm. Each bar contains several widths of the silicon waveguides from 1 µm to 5 µm.

Figure 2.13 shows the continuous wave (CW) output power as a function of pump power and temperature from two different lasers with waveguide widths of 4 µm and 1 µm. In Fig. 2.13(a), a 4 µm wide device is operating with a threshold pump power of 23 mW with a fiber-coupled maximum output power of 4.5 mW and a slope efficiency of 3 % at 20 ºC. The total maximum output power taking into account the light from both facets and the coupling losses of 5 dB is approximately 28 mW and the corresponding slope efficiency is 16 %. The threshold increases from 23 to 105 mW between 20 ºC and 60 ºC as shown in the inset of Fig.2.13(a) and the structure exhibits a temperature coefficient \( T_0 \) of 27 K. The kinks in the LL curves are due to multimode lasing with a wide waveguide dimension. It is observed that higher order modes are superimposed onto the fundamental mode in region II of the LL curve while only a fundamental mode is lasing in region I. Figure 2.13(b) shows
LL curves of a 1 µm wide device with a threshold of 120 mW and a slope efficiency of 0.5 % at 20 ºC. Since this waveguide width is narrower, the fundamental mode lases without other higher order modes up to 0.6 mW. This device demonstrates a maximum fiber-coupled output power of 0.9 mW. The total maximum output power including the output from both facets and coupling losses is approximately 5 mW with a slope efficiency of 2.8 %. The lasers with other waveguide widths also operate continuous wave at room temperature and have threshold powers between 23 mW and 120 mW.
Figure 2.13. LL curves (a) 4 µm wide, 800 µm long device (b) 1 µm wide, 800 µm long device.
Figure 2.14. Lasing spectra for a 4 µm wide, 800 µm long device. The y-axis is in log scale.

Figure 2.14 shows the lasing spectrum of a 4 µm wide device with two different pump powers all operating at 25 °C. The optical spectrum consists of the expected FP response for the 800 µm long cavity.

Overall device yield and threshold variation are shown in Fig. 2.15. Sixty devices (ten devices at each of the six widths) were characterized. 47 of the sixty devices lase with a threshold power for each waveguide width varying less than ±9 %. The yield of the four wider widths is 98 %, but the yield is lower for the narrower stripe widths due to damage during polishing. In Fig. 2.16, the measured optical modes imaged by the IR camera are shown for different waveguide widths. The simulated mode profiles are also shown in the same figure. The transition of the optical mode from the III-V region to the silicon region can be seen as the waveguide width increases. The calculated silicon and quantum well confinement
factors are also summarized for each waveguide width at the bottom of the figure. The experimentally observed optical modes qualitatively match the calculated mode profiles.

![Figure 2.15](image)

**Figure 2.15.** Device yield and threshold variation. Number at each width represents the number of lasing devices out of ten fabricated devices.

![Figure 2.16](image)

**Figure 2.16.** Simulated (top) and measured (bottom) optical mode profiles of the optically pumped hybrid lasers with different waveguide widths. The waveguide height is 0.76 µm with a slab height of 0.1 µm. The calculated silicon and the quantum well confinement factors are specified at the bottom.
2.5 **SUMMARY**

This chapter described the general concepts of the hybrid silicon evanescent device platform and explored issues related to device fabrication. The hybrid waveguide structure consists of a silicon waveguide bonded to III-V layers. The optical mode in this waveguide structure lies both in the silicon and III-V regions and optical gain/absorption can be provided from the III-V MQW region by injecting carriers through this region. The basic waveguide design concept has been discussed. The silicon waveguide dimensions can manipulate the confinement factors of the silicon and the MQW regions, and in general a taller or wider silicon waveguide has more mode overlap in the silicon region. This characteristic can be utilized to achieve high gain and high saturation in multistage amplifiers or detectors by tapering the silicon waveguide width. Tapering adjusts the quantum well confinement factor along the length of the device and hence, better controls absorption and saturation characteristics as the photon density in the hybrid waveguide changes.

The low temperature oxygen plasma assisted wafer bonding process has been described in this chapter as well. The oxygen plasma surface treatment enables bonding of two different material systems at a low annealing temperature to preserve the material quality. The chemical reaction during the annealing step has been studied and the introduction of bonding channels and an ozone cleaning process are found to improve the quality of the bonded layers as well as the device yield.
Finally, the optically pumped hybrid lasers have been demonstrated as a proof of concept for this new device platform. The fabricated lasers operate continuous wave at room temperature and have thresholds in the range of 23 mW \textasciitilde 120 mW depending on the waveguide dimensions. The lasing mode profiles also follow the trend of simulated mode profiles. This demonstration indicates the quality of the III-V material is well preserved after the low temperature wafer bonding process, and thus highlights the ability of this hybrid architecture to build active photonic devices on the silicon photonics platform.
2.6 REFERENCES


Chapter 3  Electrically Pumped Silicon Evanescent Amplifiers and Lasers

This chapter presents the first electrically pumped silicon evanescent lasers and amplifiers operating at the 1.5 µm wavelength range. The first part of this chapter covers the first demonstration of an electrically pumped silicon evanescent laser operating continuous wave (CW) with a threshold of 65 mA at 15 °C and a maximum operating temperature of 40 °C. The second part of this chapter presents a silicon evanescent amplifier with a maximum on-chip gain and 3 dB output saturation power of 13 dB and, 11 dBm, respectively. High speed data amplification is investigated at various data rates and the power penalty due to ASE noise and the pattern effects is measured to be in the range of 0.5 ~ 1 dB. In addition thermal characteristic of the device are also analyzed to achieve further improvements for next generation devices.

3.1 Device Structure

Figure 3.1 shows the cross sectional structure of the first hybrid silicon evanescent lasers and amplifiers. The width of III-V mesa is 75 µm while the current channel at the center of the III-V mesa is 4 µm. The silicon strip waveguide height is 0.76 µm. A 2 µm thick BOX layer is used for a bottom cladding of the silicon waveguide. The lasers and amplifiers have different facet configurations. The laser facets are normal
to the waveguide direction to form mirrors with a ~32% reflection while the amplifier facets are 7° tilted to the waveguide direction and anti-reflection (AR) coated to suppress the feedback from the reflected light (See Fig 3.1(b). Figure 3.2 shows a scanning electron microscope (SEM) image of the hybrid waveguide for lasers and amplifiers. The final length of the laser and amplifier is 860 µm and 1.36 mm respectively.

The devices are mounted on a temperature controlled stage and are driven by applying current through the top p contact. Lensed fibers are used to couple the light in and out of the devices with an estimated coupling loss of 5 dB. Coupling loss is estimated by factoring out waveguide loss from an insertion loss measurement. First, the insertion loss (~19 dB from a 1.36 mm long amplifier) is measured from the amplifier at long wavelengths. Second, the waveguide loss is estimated to be ~9 dB from a modal loss of 15 cm⁻¹ measured from the laser using Hakki-Paoli method [1]. This coupling loss is used to characterize device performance through this chapter.

**Figure 3.1.** (a) cross-sectional structure of the 1st demonstrated laser and amplifier (b) top view of the laser (c) top view of the amplifier.
3.2 Fabry-Perot Silicon Evanescent Laser

3.2.1 Laser Performance

The facets of the devices are normal to the waveguide and made by dicing and polishing the ends of the hybrid waveguide. This forms a laser cavity with a ~32 % mirror reflectivity. The silicon waveguide width is 2.5 μm.

The device first is tested under pulsed current injection by applying 0.5 μs long square-wave current pulses with a 4 % duty cycle. The output power is measured from one facet through a fiber coupling for various stage temperatures ranging from 15 to 80 °C as shown in Fig. 3.3 (a). The pulsed threshold is 52 mA and its fiber coupled differential efficiency is 3.1 % at 15 °C. The maximum lasing temperature is 75 °C. Taking into account the 5 dB coupling loss and considering light output from the both facets, a total differential efficiency under pulsed operation can be estimated at ~19.7 %.

The L-I curves as a function of temperature for CW operation are shown in Fig. 3.3 (b). The curves show the typical output power roll-off at higher current because of self heating effect. The CW threshold is 65 mA and a maximum fiber coupled single sided CW output power is 1.8 mW at 15 °C with a corresponding differential efficiency of 2.1 %. A total CW differential efficiency and a maximum CW output power is estimated.
at 13.3 % and 11.4 mW, respectively considering the fiber coupling loss and the double sided output power. The injection efficiency for the pulsed operation is estimated to be 61 % [2]. Using this value, the pulsed differential efficiency is theoretically calculated to be 28.3 %. The discrepancy between the measured pulsed differential efficiency and the theoretical estimation can be attributed to the uncertainty in the coupling loss.

![LI curves of the hybrid laser](image)

**Figure 3.3.** LI curves of the hybrid laser (a) pulsed operation (b) CW operation.

The threshold current variation with different stage temperatures for pulsed and CW operation is shown in Fig. 3.4. The pulsed threshold current increases from 52 to
212 mA with a maximum lasing temperature of 75 °C. Under pulsed operation the characteristic temperature coefficient ($T_o$) is estimated to be 45 K which is comparable to III-V lasers on InP operating in 1.5 µm wavelength regime [3]. The CW threshold current increases from 65 to 135 mA between 15 °C and 40 °C resulting in a CW characteristic temperature coefficient ($T_o$) of 39 K. It is lower than that of the pulsed operation because it includes the effect from the thermal impedance of the laser structure.

![Figure 3.4. Threshold current variation as a function of stage temperatures.](image)

![Figure 3.5. IV characteristics.](image)
The IV curve is shown in Fig. 3.5. The laser has a threshold voltage of 2 V and a series resistance of 7.5 ohms in the range of 2 ~5 V. Most of the series resistance is contributed from the thin n layer. The dotted line in the figure represents the simulated IV curve using Silvaco™. The series resistance is calculated to be 7.2 ohms. Even though the simulation and the experiment yield a similar series resistance, there is a discrepancy between the IV curves because of the slow turn-on between 1 and 2 V in the measured IV curve.

The device relies on ~32 % reflectivity from a polished facet and a reduction in threshold current can be achieved by optimizing the cavity structure. The threshold current is typically determined by volume, resonance characteristics, gain and loss of the cavity. Figure 3.6 shows estimated threshold current with a different reflectivity and a cavity length. The threshold current is calculated from a total modal loss of a cavity and an approximated logarithmic formula between a current density and a material gain. Equation 3.1 describes the relationship between a threshold current density \( J_{th} \) and a total modal loss. The \( g_0, J_0, \eta_i, \Gamma_{QW}, \alpha_i \) and \( \alpha_m \) is gain coefficient, transparent current density at the active region, injection efficiency, quantum well confinement factor, modal waveguide loss, and mirror loss respectively [3]. From Eq. 3.1, the threshold current with different reflectivity and cavity length is derived as described in Eq. 3.2. \( L \) and \( W \) in the equation are the cavity length and the width of the active region.
\[
\Gamma_{QW} g(J_{th}) = \Gamma_{QW} g_0 \log\left(\frac{\eta_i J_{th}}{J_{tr}}\right)
\]

\[
= \alpha_i + \alpha_m \\
= \alpha_i + \frac{1}{L} \log\left(\frac{1}{R}\right) \\
\text{Eq.3.1}
\]

\[
I_{th}(L, R) = \frac{W L J_w}{\eta_i} \exp\left(\frac{1}{g_0 \Gamma_{QW}} \left(\alpha_i + \frac{1}{L} \log\left(\frac{1}{R}\right)\right)\right) \\
\text{Eq.3.2}
\]

As stated before, a modal waveguide loss \((\alpha_i)\) of 15 cm\(^{-1}\) was measured using the Hakki-Paoli method in the long wavelength regime. \(g_0\) and the transparent input current density \((J_w/\eta_i)\) is estimated to be 972 cm\(^{-1}\) and 777 A/cm\(^2\) by measuring the single pass gain from the amplifier which will be described in detail in Chapter 3.3. Note that \(J_{tr}\) is defined as a transparent current density at the active region. Finally a quantum well confinement factor \((\Gamma_{QW})\) of 3.4 \% is calculated using Beamprop\textsuperscript{TM} mode solver. Both threshold currents for pulsed and CW operation are plotted at a given cavity length. The CW threshold current shows a better agreement with the calculations since the gain coefficient and the transparent current density are measured under CW current injection. In general, the threshold current is lower with higher reflectivity as shown in the figure and a highly resonant cavity structure can be realized by the deposition of high reflection coatings onto the waveguide facets, Bragg gratings or ring resonant cavity structures.
Additional improvements in lasing threshold and differential efficiency could be made by improving the injection efficiency of the device. The proton implant profile is designed to be effective through at least the upper half of the SCH in the p-type mesa, but has not been experimentally optimized. This implant profile could be optimized in order to reduce the current spreading in the SCH to minimize the portion of the current which flows to outside of the lasing region (active region) as shown in Fig. 3.7.
Figure 3.8 shows the measured lasing spectra of the laser driven at three different current levels of 75, 200 and 350 mA. The spectrum was measured with an HP 70952A optical spectrum analyzer with a resolution bandwidth of 0.08 nm. The lasing wavelength is around 1577 nm at 75 mA and is shifted to longer wavelengths at higher current levels due to device heating. The rate of lasing peak shift is \( \sim 0.22 \ \text{nm/mA} \). The spectrum consists of the Fabry-Perot response with a free spectral range of 0.38 nm corresponding to a modal group index of 3.68.

![Fig. 3.8 CW lasing spectra with different current levels.](image)

Other device dimensions were also fabricated for waveguide widths from 1-3.5µm. The yield is reasonable with 26 of the 36 lasers on this chip lasing all with similar performance when tested individually. The output powers and current thresholds were all on the order of \( \sim 1 \ \text{mW} \) and \( \sim 75 \ \text{mA} \) respectively. The current yield is dominated by waveguide chipping and bond delamination during polishing of the bonded waveguide facets and is more prevalent in the narrower waveguides. In addition, this
step makes the quality control of the polished facets very difficult resulting in a large variation in coupling loss. Utilizing monolithic laser feedback schemes, such as ring resonator cavities or gratings in the silicon region will remove the device performance dependency on facet polishing, which will also enable the reliable characterization of the device performance such as the injection efficiency and the waveguide loss.

3.2.2 Thermal performance analysis

Commercial optical devices for telecommunications typically require a maximum operating temperature of greater than 60 °C. In order to meet this requirement and provide sufficient device performance at various operating conditions this section investigates the thermal characteristics of the device to improve the maximum operating temperature.

Laser turn-off occurs when the active region doesn’t provide enough optical gain to overcome the net modal loss of the laser cavity. The optical gain from the active region drops as the temperature increases because of the increased carrier leakage out of the active region and non-radiative recombination [3]. When the active region temperature is too high to keep the optical gain at threshold, the laser will shut off. Under the pulsed operation, the maximum operating temperature is the same as the active region temperature at laser turn-off ($T_{\text{off}}$). However, if there is self heating associated with electrical power consumption in the device, i.e. under CW operation, the active region temperature increases as electrical current is injected. This causes output power roll-off after the lasing threshold and eventually turns off the laser. In addition, the maximum CW operating temperature is lower than the maximum pulsed
operating temperature since the active region temperature is always higher than the ambient temperature.

The amount of the temperature increase due to the electrical power consumption is determined by the thermal impedance of the device. The thermal impedance of the device can be extracted from the electrical power consumptions at the laser turn-off at various stage temperatures \( T_{\text{stage}} \) [3]. The relationship between \( T_{\text{off}} \) and \( T_{\text{stage}} \) can be written as Eq. 3.3 assuming self heating is primarily caused by the electrical power dissipation of the diode.

\[
T_{\text{off}} = T_{\text{stage}} + \Delta T_{\text{self-heating}} \\
= T_{\text{stage}} + P_{d,\text{off}} Z_T
\]

Therefore,

\[
P_{d,\text{off}} = -\frac{1}{Z_T} (T_{\text{stage}} - T_{\text{off}}) \quad \text{Eq. 3.3}
\]

\( P_{d,\text{off}} \) is electrical power dissipation at the laser turn-off and \( Z_T \) is a thermal impedance of the laser structure. Since \( T_{\text{off}} \) and \( Z_T \) are constant with a given cavity structure, \( P_{d,\text{off}} \) varies linearly with \( T_{\text{stage}} \).

Electrical power dissipation at the laser threshold also can be written as Eq. 3.4.

\[
P_{d,\text{th}} = I_{\text{th}} V_{\text{th}} \\
\approx \frac{I_0^2}{R_s} \exp\left(\frac{2T_{\text{stage}}}{T_0}\right) + V_{\text{ON}} I_0 \exp\left(\frac{T_{\text{stage}}}{T_0}\right) \quad \text{Eq. 3.4}
\]

Equation 3.4 assumes that the threshold current increases exponentially with the stage temperature, \( I_{\text{th}} = I_0 \exp(T_{\text{stage}}/T_0) \), and the threshold voltage of the diode is linear with the threshold current, \( I_{\text{th}} = R_d (V_{\text{th}} - V_{\text{ON}}) \).
At a given stage temperature, if the electrical power consumption for the laser threshold is larger than the electrical power consumption at the laser turn-off \((P_{d,\text{th}} > P_{d,\text{off}})\), the device can’t reach to the lasing threshold because the optical gain will walk off from the threshold gain as the driving current increases. Figure 3.9 shows \(P_{d,\text{off}}\) and \(P_{d,\text{th}}\) of the current device which are extracted from the measured LI and IV curves. The thermal impedance \((Z_T)\) and the active region temperature at the laser turn-off \((T_{\text{off}})\) is estimated to be 40 °C/W and 80 °C respectively by linear fitting the measured \(P_{d,\text{off}}\) with Eq. 3.3. This agrees with the measured maximum pulsed operating temperature shown in Fig.3.3 (b).

![Figure 3.9](image)

**Figure 3.9.** Electrical power consumptions at the threshold and the laser turn-off. Dotted lines are plotted by the data fitting using Eq. 3.3 and Eq. 3.4.

In order to achieve a high operating temperature, it is important to design the device such that the generated heat is extracted out of the active region efficiently as well as the minimizing electrical power consumption in the device. The thermal
impedance of the current device dimensions is analyzed. Figure 3.10 shows the
temperature profile calculated by solving the heat equation using finite element method
with FEMLAB™. Thermal conductivity of each layer used in the simulations is
summarized in Table 3.1. It is assumed that the temperature of the 4 µm wide region at
the center of the III-V layers generates heat. Heat flux \(Q_{\text{heat}}\) is calculated by setting the
temperature of the boundary of the center of the III-V region \(T_{\text{active}}\) and the bottom of
the silicon substrate \(T_{\text{stage}}\) to be 77 °C and 27 °C respectively. The thermal impedance
of a given structure is calculated using Eq. 3.5

\[
Z_T = \frac{T_{\text{active}} - T_{\text{stage}}}{Q_{\text{heat}}} 
\]  

Eq. 3.5

The calculated thermal impedance of the current laser structure is 47 °C/W which agrees
reasonably with a measured impedance of 40 °C/W.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity (Wm⁻¹K⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V layers</td>
<td>68</td>
</tr>
<tr>
<td>Silicon</td>
<td>163</td>
</tr>
<tr>
<td>SiO₂</td>
<td>1.38</td>
</tr>
<tr>
<td>Gold</td>
<td>310</td>
</tr>
</tbody>
</table>

Table 3.1. Thermal conductivity used in the simulations.

Figure 3.10. Temperature profile of the laser structure. The active region
temperature and the bottom of the silicon substrate are set to be 77 °C and 27 °C
respectively. Most of the substrate is omitted in this figure for better illustration.
The thermal impedance of the current device is primarily limited by the 2 μm thick BOX layer. Figure 3.11 shows the calculated thermal impedance as a function of a thickness of the BOX layer (Fig.3.11 (a)) and III-V mesa width (Fig.3.11(b)). The reduction of the BOX thickness will reduce the thermal impedance, as shown in the figure, but cannot be reduced indefinitely since that layer is used as the lower cladding of the optical waveguide. Thinner BOX layer thicknesses yield higher propagation loss due to mode leakage into the substrate. The leakage loss as a function of a BOX layer thickness is calculated using Beamprop™ as shown in the secondary y-axis of Fig. 3.11(a). With a given waveguide height of 0.7 μm, the BOX layer thickness should be more than 0.3 μm to keep the leakage loss less than 0.1 dB/cm.
Figure 3.11. (a) Calculated thermal impedance in left y-axis and optical loss in right y-axis as a function of BOX thickness. (b) Calculated thermal impedance in left y-axis and series resistance in right y-axis as a function of III-V mesa width.

Further improvement can be achieved by minimizing the electrical power consumption of the device. The series resistance of the device is mostly contributed by the thin n type layer. Figure 3.11(b) shows the calculated thermal impedance variation with different III-V mesa widths while its secondary y-axis shows the calculated series resistance. The gap between the end of the III-V mesa and n contact, and the current
channel width at the center of the III-V mesa is kept to be 2 µm, and 4 µm respectively. As shown in the figure, there is a sharp drop in the thermal impedance near a mesa width of 30 µm. When the mesa width is narrower than 30 µm, the edges of the III-V mesa don’t overlap with the silicon at both sides. As a result, heat flow relies only on the center path through the 2 µm wide silicon waveguide resulting in higher thermal impedance as shown in Fig. 3.12(a).

**Figure 3.12.** (a) Temperature profile in a narrow mesa (b) temperature profile with a thermal shunt.

The thermal impedance of narrow mesas can be lowered with several changes in the device design. First, the air gap width can be narrowed to ~3 µm at each side. This air gap needs to be chosen carefully to ensure that optical mode is not coupled to the silicon region at the both sides. Second, the thermal shunt structure utilizing probe metal can extract heat from the active region to the silicon substrate through the additional
metal pads deposited on the III-V mesa. Its general structure is shown in Fig. 3.12(b). At the right side of the mesa, the top silicon layer and BOX layer are etched away and the metal pad is deposited creating additional path of heat flow from the top of the mesa to the silicon substrate. Figure 3.12(b) shows the effectiveness of the thermal shunt. The thermal impedance is calculated to be 51 °C/W which is 2.5 times reduction compared to the structure shown in Fig. 3.12(a). Additional reduction in the thermal impedance can be achieved by optimizing the device dimensions and metal spacing.
3.3 **Silicon Evanescent Amplifier**

Optical amplifiers are key components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. However, they have only been realized in silicon through optical pumping using the Raman effect [5]. As an alternative approach, a die of III-V based amplifiers can be attached to a silicon passive waveguide circuit, but their gain and noise figure are limited by reflections from interfaces and coupling loss to the silicon waveguide. The silicon evanescent device platform can solve this problem since the optical mode of the hybrid waveguide can be tailored to be similar to the silicon passive waveguide mode leading to efficient mode coupling with very low reflection. In this section, the first silicon evanescent amplifier is presented, and its dynamic amplification characteristics are investigated.

3.3.1 **Amplifier performance**

The facets of the amplifier are 7° angled and AR coated to prevent reflection and enable single pass gain measurements. The silicon waveguide width of the amplifier is 2 µm. The device gain is measured by launching and collecting the signal through lensed-fibers at both the input and output facets. The input polarization is controlled by a polarization controller. The angle between the fiber and the normal to the facet is ~25° to maximize the coupling of output light from the 7° angled waveguide.
Figure 3.13. (a) Measured amplifier gain as a function of current (b) estimated net modal gain and material gain as a function of input current density. Note that the x-axis represents input current density, not current density at the active region.

Figure 3.13(a) shows the measured TE small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using a 5 dB coupling loss. The maximum fiber-to-fiber TE gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. Figure 3.13(b) represents the estimated net modal gain, \( \Gamma_{\text{QW}-\alpha} \). The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current.
density at the device input, \( g = g_0 \log(\eta_i J/J_{tr}) \), where \( g_0 \) is 972 cm\(^{-1}\) and \( J_{tr}/\eta_i \) is 777 A/cm\(^2\). With the estimated injection efficiency of 61 \%, the transparent current density at the active region is \( \sim 466 \) A/cm\(^2\). The fitting uses the gain data at the lower current density regime where the device heating effect is not significant. However, more accurate material gain with a current density can be measured under pulsed operation. The waveguide loss \((\alpha_i)\) of 15 cm\(^{-1}\) is used and \( \Gamma_{QW} \) is assumed to be 3.4 \%. At lower current densities, the gain increases logarithmically, while at higher current densities it saturates due to device heating.

Figure 3.14 shows the gain spectra with different bias currents. The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA for TE polarization. The measured TM gain is typically lower than TE gain because of the compressively strained quantum wells. For example, TM gain is around 1 dB when TE gain is 10 dB.

![Figure 3.14. Gain spectra with different current levels.](image-url)
Figure 3.15(a) shows gain saturation characteristics of the device. Output power on the x axis is rescaled from the measured value considering 5 dB coupling loss. The 3 dB output saturation power from the chip is measured to be 11 dBm. The 3 dB output saturation power, $P_{0,SAT}$, can be theoretically written as Eq. 3.6 [6],

$$P_{0,SAT} = \frac{G_0 \log 2}{G_0 - 2} \cdot \frac{wd}{\Gamma} \cdot \frac{h\nu}{(dg/dN)\tau}$$  \hspace{1cm} \text{Eq.3.6}

where $G_0$ is the unsaturated chip gain, $w$ is the optical mode width at the quantum well region, $d$ is the total thickness of the active material, $h\nu$ is the photon energy, $dg/dN$ is the differential gain, and $\tau$ is the carrier lifetime. Figure 3.15(b) shows the calculated $P_{0,SAT}$ with different quantum well confinement factors ($\Gamma_{QW}$) and optical mode widths ($w$) at a unsaturated chip gain ($G_0$) of 13 dB. The measured value agrees with theoretical calculations computed with a mode width ($1/e$) of 2 µm. The fundamental mode supported in this hybrid waveguide structure is similar to the one in the offset quantum well structure and its typical quantum well confinement factor is in the range of 2 ~3 % resulting in higher output saturation powers than the centered quantum well amplifiers with a typical quantum well confinement factor of 5 ~15 %. Further improvement of the saturated output power may be obtained by using the tapered or flared waveguide structure demonstrated with III-V amplifiers [7] by manipulating the silicon waveguide width without changing the III-V region. For example, the beginning of the amplification, a hybrid waveguide with a narrower silicon waveguide width (Fig. 2.4(a)) is used and the silicon waveguide width is tapered out to reduce the quantum well
confinement factor (Fig. 2.4(c)) as the photon density increases for better saturation characteristics.

![Figure 3.15](image)

**Figure 3.15.** (a) Measured gain saturation (b) 3 dB saturation output power as a function of quantum well confinement factor with different mode size.

The noise figure \( NF \) is measured from the spontaneous emission density at the signal wavelength using Eq. 3.7 [8].

\[
NF = 10 \log \left( \frac{2 \rho_{\text{ASE}}}{G_o h \nu} + \frac{1}{G_o} \right) \tag{3.7}
\]

The first term in the logarithm formula represents signal-spontaneous beat noise and the second term represents shot noise. It should be noted that \( \rho_{\text{ASE}} \) is the ASE density at the signal wavelength with the same polarization state as the signal. Since the quantum wells are compressively strained, it is assumed that the most of the ASE noise is TE polarized [9] and this assumption gives more conservative estimation of the NF.

The measured NF varies between 16.4 dB and 12.7 dB depending on the current level as shown in Fig. 3.16(a). The internal NF of the device can be between 11.4 dB and 7.7 dB considering 5 dB coupling loss. The dotted line in the figure is calculated noise...
figure using Eq. 3.8 [6] from the measured gain characteristics assuming that spontaneous emission is dominant over other non-radiative recombination. The NF decreases at higher current levels because of a larger spontaneous emission factor, $N_a/(N_a-N_{tr})$. The discrepancy between the theory and the measurements can be attributed from the TM portion of the ASE noise as well as the uncertainty of the coupling loss measurement (typically +/- 0.5 dB). In addition, there are some difficulties in measuring the ASE density over the small frequency interval of interest which is associated with the finite resolution bandwidth of the spectrum analyzer (0.1 nm) [10].

$$NF = 10 \log_{10} \left( \frac{2N_a}{N_a - N_{tr}} \cdot \frac{\Gamma_{QW} g(N_a)}{\Gamma_{QW} g(N_a - \alpha_i)} \right)$$

$$= 10 \log_{10} \left( \frac{2J}{J - J_{tr}} / \eta_i \cdot \frac{\Gamma_{QW} g(J)}{\Gamma_{QW} g(J - \alpha_i)} \right)$$

Eq. 3.8

Figure 3.16. (a) Measure the noise figure of the amplifier (b) amplified spectra (inset) ripples of ASE spectrum from a residual reflectivity.

Figure 3.16(b) shows the amplified spectra with amplified spontaneous emission (ASE) noise spectra with different current levels. The residual reflectivity from a 7 °
angled and AR coated facet is estimated to be $5 \times 10^{-4}$ by measuring a spectral ripple of 0.2 dB at 13 dB chip gain as shown in the inset of Fig. 3.16(b).

3.3.2 High speed data amplification

Eye closure due to carrier dynamics in semiconductor optical amplifiers is a major issue in the design of SOAs. Injecting a short, high power optical pulse into the semiconductor amplifier will cause gain saturation instantaneously [11]. The slow gain recovery process associated with carrier injection requires several hundred picoseconds to restore the unsaturated gain. In the case of pseudo random bit sequences (PRBS), the amplified output can be strongly degraded by pattern effects. Figure 3.17 shows measured 10 Gb/s NRZ eye diagrams with three different input powers. The degradation of the quality (Q) factor of the signal can be observed with input power above -4 dBm.

![Eye Diagrams](image)

**Figure 3.17.** 10 Gb/s NRZ amplified eye diagrams after amplification (a) -7 dBm input power (b) 2 dBm input power (c) 5 dBm input power.

To investigate the performance of the fabricated amplifier, bit error rate (BER) measurements are employed at 3 different data rates, 2.5 Gb/s NRZ, 10 Gb/s NRZ and 40 Gb/s RZ. For 10 Gb/s and 40 Gb/s, PRBS of $2^{31} - 1$ was used to carry out the BER test. A shorter sequence of $2^{10} - 1$ was chosen for 2.5 Gb/s because of low frequency cut
off in the measurement system. The input power is kept at -16 dBm to keep the device unsaturated. A variable optical attenuator (VOA) is inserted between the output of the amplifier and the receiver (Rx) to adjust the received power. Power penalty of the amplifier is extracted by comparing the BER performances of the Tx-amplifier-Rx link with the back-to-back transmitter (Tx). As shown in Fig. 3.18 a low power penalty of 0.5 dB for all three data rates is achieved. This penalty comes in majority from the ASE noise of the amplifier, which is not related to the data rate or the pulse duration. To compare the distortion due to the pattern effect, another BER curve with a higher input power of 2 dBm is plotted in Fig. 3.19 An additional power penalty of 0.5 dB is required when pattern effect starts to reduce the Q factor of the signal.

![Figure 3.18](image)

**Figure 3.18.** High speed data amplification at NRZ 2.5 Gb/s and RZ 40 Gb/s. (a) eye diagrams with and without amplification (b) BER curves for 2.5 Gb/s and 40 Gb/s amplification.
3.4 SUMMARY

This chapter presented the first hybrid laser and amplifier. The laser operates CW at room temperature with 65 mA threshold, ~1.8 mW single sided fiber coupled output power and overall differential quantum efficiency of 13.3%. The maximum operating temperature is 40 °C and is good for a first demonstration, and has potential for improvement by improving heat extraction and minimizing parasitic heat generation. Thermal analysis shows that the thermal impedance of the device can be improved with thinner BOX layers. Moreover, the heat generation can be reduced by reducing the series resistance of the device. In addition high resonant cavity designs such as integrated Bragg reflectors or ring structures can reduce the threshold current, further extending the maximum operating temperature.
The amplifier has a maximum chip gain of 13 dB and a spectral bandwidth of 62 nm. The internal noise figure of the device is 8 dB at a high current density which is close to the typical noise figure of conventional III-V amplifiers. The 3 dB saturation output power is 11 dBm which is expected from the dimensions of the fabricated devices. The device structure yields 2 ~ 4 % quantum well confinement factors and this low confinement structure is inherently beneficial for the linear amplifications. The hybrid waveguide structure can be designed to be similar to a centered quantum well structure by manipulating the silicon waveguide dimensions and this is better for applications requiring high gain such as boost amplifiers. High speed amplification capability is also presented and the power penalty from the ASE noise is ~0.5 dB regardless the data rates. The pattern effect degrades the signal quality at high input power, and the device exhibits ~1 dB power penalty from this effect at 2 dBm input power with 10 Gb/s NRZ modulation.

Even though this demonstration is the first step to build active silicon photonic integrated devices, it should be mentioned that the performance from the first demonstrated devices trails the state of art III-V lasers and amplifiers. However, a lot of improvement can be achieved by modifying the device dimensions and employing advanced silicon waveguide structures such as tapers, ring resonators, and gratings.
3.5 REFERENCES


Chapter 4  Silicon Evanescent Photodetectors

This chapter presents silicon evanescent photodetectors. The photodetector consists of two sections: 1) a silicon passive waveguide at the input and 2) a hybrid waveguide to absorb the light coupled from the silicon input waveguide. The hybrid waveguide has the same cross sectional structure as the lasers and amplifiers. This is advantageous as it provides for easy integration with active devices that have the same epitaxial layer structure and fabrication procedures. The first fabricated hybrid photodetector has a fiber coupled responsivity of 0.32 A/W with an internal quantum efficiency of 90%. The device bandwidth is 0.5 GHz and is limited by the relatively large device dimensions and parasitic capacitances. A redesign followed by a second fabrication run was undertaken to achieve higher speed operation. The results from this run are also presented in this chapter and the devices show a bandwidth of 1 GHz limited by a low frequency roll-off from carrier diffusion. Finally, alternative device structures are described for next generation high speed devices based on the experience gained from the first couple of iterations.
4.1 **FIRST GENERATION DEVICE**

4.1.1 **Device Structure**

Figure 4.1(a) shows the cross sectional structure of the 1st hybrid silicon evanescent photodetector. The width of III-V mesa is 12 µm while the current channel in the center is 4 µm wide. The silicon rib waveguide is fabricated with a final height of 0.69 µm, width of 2 µm, and slab thickness of 0.19 µm. Figure 4(b) shows the top view of the device. The light from a fiber is first coupled to the silicon passive input waveguide and then the optical mode in the passive silicon waveguide is coupled to the hybrid waveguide. At the junction of the hybrid waveguide and the passive silicon waveguide, the III-V region is tilted by 7º to reduce the reflection at the waveguide transition. As light propagates through the hybrid waveguide, it is absorbed in the III-V region generating electron hole pairs. When the device is under reverse bias, the carriers are swept away. The silicon facet is diced with an angle of 7 ° and AR coated with a single layer of Ta₂O₅ (~5 % reflectivity) to minimize the reflection. The final III-V absorbing region length in the hybrid photodetector is 400 µm. A SEM image of the final fabricated hybrid photodetector and a close view of the junction at the device input are shown in Fig. 4.2(a) and (b) respectively. In Fig.4.2(b), the surface roughness at the interface is originated from the un-optimized hard mask etching process. The little dots on the silicon waveguide are most likely polymers generated during the III-V etching process. These can be removed by a better de-scum process. The silicon confinement factor is calculated to be 63 % with the fabricated device dimensions while the quantum well confinement is calculated to be 4 %.
Figure 4.1. (a) cross-sectional device structure (b) top view.

Figure 4.2. (a) SEM of the fabricated device (b) SEM of the junction between the input silicon waveguide and the hybrid photodetector.
4.1.2 Device Characteristics

The device is mounted on a temperature controlled stage set to 15 °C. The photodetector responsivity is measured by launching the light into the silicon waveguide through a lensed fiber and measuring the generated photocurrent with a Keithley 2400 source meter while placing the device under reverse bias. The angle between the fiber and the normal to the facet is ~25° to maximize the light coupling from the laser source to the 7° angled silicon waveguide facet. The coupling efficiency from the fiber to the input silicon waveguide is estimated to be -5.5 dB by measuring insertion loss of a passive silicon waveguide of the same dimensions. The input polarization is controlled by a polarization controller.

![Figure 4.3. Measured TE responsivity and internal quantum efficiency.](image)

**Table 4.1.** Calculated coupling efficiency from the fundamental mode of the silicon input waveguide to the four different modes of the detector waveguide with calculated III-V confinement factors. The white lines in the middle represent the quantum well layers.
Figure 4.3 shows the measured TE responsivity on the first y-axis with an input power of 0.2 mW. The measured TE responsivity at 1550 nm is 0.31 to 0.32 A/W, and is roughly constant over a range of bias conditions (0.5V to 3V). Figure 4.3(a) also shows the calculated quantum efficiency of the photodetector using the estimated 5.5 dB fiber coupling loss. At a reverse bias of 3V the quantum efficiency is ~ 90 % at 1550 nm. Even though the mode overlap between the silicon rib waveguide and the fundamental hybrid waveguide mode is 63 %, the quantum efficiency is higher than this because of higher order mode coupling. The 12 µm wide absorbing layer can collect other higher order modes excited from the input silicon waveguide mode. The coupling from the fundamental mode of the silicon waveguide to each mode of the hybrid waveguide is calculated using FIMMWAVE™ and the simulation shows ~95 % of the input mode is coupled to the hybrid waveguide modes. Table 1 summarizes the calculated coupling efficiency of four different modes of the detector waveguide. The calculation of quantum efficiency does not take into account the scattering loss. The reflection at the edge of the III-V region is calculated to be approximately $10^{-6}$ when the fundamental mode of the silicon waveguide is coupled to the hybrid waveguide. The reflection at the interface is small because the fundamental mode of the silicon waveguide doesn’t experience much of the discontinuity of the III-V layers when it is coupled to the hybrid waveguide. The TE material absorption coefficient is estimated to be $1594 \text{ cm}^{-1}$ at zero bias by measuring the output power from a silicon output waveguide and using the calculated quantum well confinement factors of the fundamental and higher order modes as summarized in Table 1. The TE spectral
response is shown in Fig. 4.4. The edge of the spectral response is redshifted with a higher reverse bias since the applied electric field increases the absorption at longer wavelength [1]. The TM responsivity is measured to be 0.23 A/W at a wavelength of 1550 nm, which is typically lower than TE responsivity because of the lower interaction of the compressively strained quantum wells with light holes.

![Figure 4.4. TE Spectral responses with different biases.](image1)

![Figure 4.5. Saturation characteristics with different biases.](image2)
Figure 4.5 shows the saturation characteristics of the device at an input wavelength of 1550 nm. The x-axis of the graph shows the coupled input power taking into account the 5.5 dB coupling loss. The laser source is amplified through an erbium doped fiber amplifier (EDFA) with a 50 mW maximum available power out of the lensed fiber resulting in a maximum power of 14 mW coupled into the device. At a lower bias, the output current generally saturates faster due to carrier screening effects [2]. The 1-dB saturation input power is 1.8 mW and 8.8 mW for 0 V and 1 V reverse bias, respectively. No output current saturation is observed beyond a reverse bias of 4 V for the available 14 mW of fiber coupled power.

![Image of I-V curve](image.png)

**Figure 4.6.** I-V curve without light input. (inset) dark current in linear scale.

The I-V curve of the device is shown in Fig. 4.6. The dark current is typically 50 nA to 200 nA with a bias range of -1V to -4 V, and breakdown occurs when the reverse bias exceeds 16 V. The diode ideality factor \(n\) under small forward bias (<0.5 V) is measured to be 2, indicating that the recombination current in the quantum well region is
dominant. The 11 ohm series resistance beyond diode turn-on (0.8 V) is due to the thin n-layer and the contact resistances.

The device capacitance was measured using a C-V meter with different reverse biases and the results are shown in Fig. 4.7(a). The capacitance is 7.5 pF under zero bias and decreases down to 5.3 pF as the reverse bias increases. This large capacitance is mainly due to the large III-V mesa size (12 µm x 400 µm). The capacitance of the III-V mesa is calculated to be 3.8 pF with zero bias ignoring the air fringe capacitance. Moreover, two p-probe pads contribute an additional capacitance of 2.95 pF from a 450 nm thick SiN layer ($\varepsilon_r=7.5$) sandwiched between the p-probe pad and the n-layers. Figure 4.7(b) shows measured capacitance with different device lengths. The capacitance is linear with device length since the mesa area and the number of p-probe pads also increase linearly.
Figure 4.7. Capacitance with different reverse bias for a 400 µm long device (b) Capacitance vs. device length at a reverse bias of 4 V.

The frequency response of the device was measured by a network component analyzer with a 50 Ω termination. The bandwidth of the device is 470 MHz at a reverse bias of 4 V as shown in Fig. 4.8. The measured bandwidth agrees with a RC limited bandwidth of 482 MHz calculated from the measured series resistance and capacitance of the device. The frequency response is currently RC limited by the large capacitance from the III-V mesa and the p-probe pads. The capacitance of the mesa can be reduced by reducing the width and length of the III-V mesa. The mesa capacitance can also be reduced by modifying the proton implant profile such that it extends through the top InGaAs p contact layer of the mesa [3]. Moreover, the p-pad capacitance can be
minimized by changing the 450 nm thick SiN insulation layer to a several micron thick benzocyclobutene (BCB, $\varepsilon_r=2.6$) layer.

![Frequency response with two different bias conditions with a 12 µm wide and 400 µm long III-V mesa. The dotted line is a calculated RC limited bandwidth.](image)

**Figure 4.8.** Frequency response with two different bias conditions with a 12 µm wide and 400 µm long III-V mesa. The dotted line is a calculated RC limited bandwidth.

### 4.2 SECOND GENERATION DEVICE

#### 4.2.1 Device Structure

As discussed in the previous section, the first generation devices have 0.5 GHz RC limited bandwidth due to the large device dimensions and the parasitic capacitance from the pad design. Three major changes are made to achieve a higher bandwidth. First, the implantation profile is adjusted to insulate the top contact layer of both sides of the III-V mesa to apply electrical field only at the center of the mesa. This reduces the width of the undoped quantum well layer which contributes to the capacitance. Second, the device length is chosen to be 100 µm with an estimated quantum efficiency of ~50 %. Finally, ~5 µm thick BCB layer is used as a pad layer underneath the p probe and the
overlapping area between the p probe pad and the n contact metal is reduced to minimize the parasitic pad capacitance. The modified cross sectional structure and top view of the second generation devices is shown in Fig.4.9(a) and (b) respectively. The silicon rib waveguide is fabricated with a final height of 0.69 µm, width of 1 µm, and slab thickness of 0.19 µm. Those waveguide dimensions yield a silicon confinement factor and a quantum well confinement factor of 30 % and 8 % respectively for the fundamental mode. When the fundamental mode of the silicon waveguide is coupled to the hybrid waveguide, higher order mode excitation will be more than the previous device because of the reduced silicon confinement factor of the fundamental mode in the hybrid waveguide. Even though this higher order coupling increases the quantum efficiency, this is detrimental for high speed operation as it causes carrier diffusion which will be discussed later in this chapter.

![Cross-sectional device structure and top view of the 2nd generation device.](image)

**Figure 4.9.** (a) cross-sectional device structure (b) top view of the 2nd generation device.

### 4.2.2 High Speed Performance

The devices are tested with the same procedure as the first generation devices. The device has an internal quantum efficiency of ~ 50 % and exhibits a similar spectral
response to the previous device. More specific data on the quantum efficiency and spectral response with various device lengths will be shown in Chapter 5.

Figure 4.10. Bandwidth of the 2nd generation device (dotted line) Estimated bandwidth from the circuit model ($R_L=50 \, \Omega$).

Figure 4.10 shows the measured device bandwidth for a 100 µm long device. The 3dB bandwidth is ~0.5 GHz because of the initial roll-off at low frequency regime. To investigate the origin of this low frequency roll-off, the impedance of the device is measured using a network analyzer. As shown in Fig. 4.11(a), the real and imaginary parts of the impedance don’t match with a simple RC circuit model. Fig. 4.11(b) shows a circuit model including additional capacitance ($C_p$) and resistance ($R_p$) parallel to the junction capacitance ($C_j$) to account for the effect of the implantation profile. Since proton implanted at each implantation energy is distributed with Gaussian profile in the vertical direction, the bottom of the SCH layer is populated with lower hydrogen density. This bottom SCH layer results in additional resistance and capacitance because some of
the current can flow through the implanted region as well as electrical field can be applied to the undoped quantum well layer. The series resistance in the model is divided into upper and lower parts shown as $R_{s1}$ and $R_{s2}$ respectively. The impedance ($Z_0$) of this circuit can be written as Eq. 4.1.

$$Z_0 = R_{s2} + \left( \frac{1}{R_{s1} + \frac{1}{j\omega C_j}} + \frac{1}{R_p + \frac{1}{j\omega C_p}} \right)^{-1} \quad \text{Eq. 4.1}$$

Reasonable fitting with measured data yields values of 0.80 pF and 370 Ω for $C_p$ and $R_p$, respectively. Other circuit parameters are summarized in the figure. Frequency response of this model is derived in Eq. 4.2.

$$\left| \frac{V_{\text{out}}}{I_p} \right|^2 = \left| \frac{R_L}{j\omega(R_L + R_{s1} + R_{s2})C_j + 1 + j\omega(R_L + R_{s2})C_p \left( \frac{j\omega R_{s2}C_j + 1}{j\omega R_p C_p + 1} \right) + 1} \right|^2 \quad \text{Eq. 4.2}$$

The dotted line in Fig. 4.10 is the calculated frequency response using Eq.4.2 with the parameters in Fig. 4.11. Even though this circuit model adds 1 dB roll-off near 1 GHz, the calculated frequency response still doesn’t account for additional 2 dB roll-off of the measured response. Additional roll-off can be attributed to the diffusion of carriers generated from both sides of the quantum wells where higher order modes are generating carriers. In this region, carriers should diffuse to the center of the mesa in order to get drifted as illustrated in Fig. 4.12. This diffusion process typically occurs on a time scale of a few hundred nanoseconds resulting in the roll-off at low frequency.
Figure 4.11. (a) Real and imaginary part of the impedance, (dotted) fitting with the circuit model (b) Circuit model for the device. The values at the bottom are used for the fitting.

Figure 4.12. Carrier diffusion due to higher order modes. One of the higher order modes is superimposed with the figure for better illustration. (not to scale)

Figure 4.13 shows two alternative structures to achieve higher bandwidth. The total width of the III-V mesa can be narrowed to 2 μm ~ 4 μm without implantation as shown in Fig. 4.13(a). This structure has a thin n layer overhanging on the air gap region and a supporting layer such as a thick polymer layer should be provided for mechanical strength. The second structure shown in Fig. 4.13(b) uses proton implantation all the way down to the quantum wells to ensure implantation of the entire SCH layer as well as to force the generated carriers in the sides of the mesa to recombine through the recombination traps created by the protons [4]. This approach has sufficient mechanical
strength but the internal quantum efficiency will be lower because the carriers can be lost through recombination without contributing to photocurrent.

Figure 4.13. Proposed structures for high speed operation (a) Narrow mesa structure (b) Wide mesa structure with deeper implantation. (not to scale)

4.3 SUMMARY

This chapter presented the hybrid photodetectors utilizing the same hybrid waveguide structure and fabrication procedures as the lasers and amplifiers. The first generation devices showed a fiber coupled responsivity of 0.32 A/W with an internal quantum efficiency of 90% over the 1.5 μm wavelength. The device bandwidth is 0.5 GHz limited by the large device dimensions and the parasitic capacitance. The second generation device is designed for a high speed operation by reducing the device length and using BCB for a pad layer. However the device speed is limited by the imperfect implantation profile and carrier diffusion. Two alternative structures for higher bandwidth are also proposed in this chapter. This device is useful as a power monitor with a laser or a pre-amplified receiver with a silicon evanescent amplifier without adding any additional fabrication steps or modifications to the III-V epitaxial structure.
4.4 REFERENCES


Chapter 5  Integrated Silicon Evanescent Preamplifier and Photodetector

This chapter presents the integration of a silicon evanescent preamplifier and a photodetector. To integrate the devices on the same silicon waveguide, the interface between the silicon waveguide and the hybrid waveguide needs to be properly designed. The abrupt and angled termination of the III-V layers used earlier for the first generation of detectors is found to insufficient when it is used in amplifiers. A III-V taper structure is designed and fabricated for amplifiers to couple the silicon waveguide mode to the hybrid waveguide mode and vise versa with high coupling efficiency and low reflection. A high speed detector design is also investigated based on the measured characteristics of the first generation detectors. The self aligned process is developed to enable pumping of the narrow III-V mesa structure present in both the taper and the detector. The integrated device exhibited a total responsivity of 5.7 A/W and a receiver sensitivity improvement of 8.5 dB at 2.5 Gb/s data rate. Several possible reasons limiting the current bandwidth and future directions to improve device speed are discussed at the end of this chapter.
5.1 DEVICE DESIGN

5.1.1 Device Structure

Figure 5.1 shows the device layout of the integrated hybrid silicon evanescent preamplifier and photodetector. There are two major changes in device design. First, at the transition between the passive silicon waveguide and the hybrid waveguide of the amplifier, the width of the III-V mesa is tapered to increase coupling efficiency and minimize reflection at the junction. The width of III-V mesa is 14 µm while the current channel in the center is 4 µm wide. Second, the III-V mesa width of the detector is narrowed down to 3 µm at the p cladding layer and 2 µm at the p-type SCH and the quantum well layers to reduce the capacitance of the device. The silicon rib waveguide is fabricated with a final height of 0.69 µm, width of 2 µm, and slab thickness of 0.19 µm resulting in a silicon confinement factor and a quantum well confinement factor of 63 % and 4 % respectively.

![Device layout](image)

**Figure 5.1. Device layout**

5.1.2 Hybrid Amplifier Interface Design

Even small reflection at the ends of the amplifier can cause significant gain ripple and even lasing due to the increased resonance from the optical gain. Figure 5.2 shows the gain ripple calculated with three different optical gains. To suppress the gain ripple
to less than 0.1 dB, reflectivity at the interface should be kept less than $4 \times 10^{-4}$ at a gain of 10 dB. Therefore, it is important to design the junction between the passive waveguide and the amplifier to minimize the reflection and also to increase the coupling efficiency of a propagating optical mode at the junction of the passive waveguide and the amplifier.

This section will investigate two different junction designs as shown in Figure 5.3. The first approach is to terminate the hybrid waveguide by tilting the interface angle between the air and III-V layers as shown in Fig. 5.3(a). The tilted interface can deflect the reflected beam leading to reduce the coupling to the input waveguide. This approach can be easily fabricated without a significant requirement of accurate alignment between the III-V junction and the silicon waveguide. Second approach shown in Fig. 5.3(b) has a tapered III-V structure so that the optical mode is adiabatically transformed from one mode to the other mode. This approach can theoretically achieve a 100% transmission,

![Figure 5.2. Gain ripple due to the facet reflectivity with different gain levels.](image)

This section will investigate two different junction designs as shown in Figure 5.3. The first approach is to terminate the hybrid waveguide by tilting the interface angle between the air and III-V layers as shown in Fig. 5.3(a). The tilted interface can deflect the reflected beam leading to reduce the coupling to the input waveguide. This approach can be easily fabricated without a significant requirement of accurate alignment between the III-V junction and the silicon waveguide. Second approach shown in Fig. 5.3(b) has a tapered III-V structure so that the optical mode is adiabatically transformed from one mode to the other mode. This approach can theoretically achieve a 100% transmission,
but the performance is dependent on the fabrication tolerance such as alignment accuracy and side wall roughness of a dry etched III-V taper.

Figure 5.3. Two different interface designs for amplifiers (a) Abrupt junction (b) Tapered junction.

5.1.2.1 Abrupt Junction

The abrupt junction with a tilted interface is first investigated because it is relatively easier to fabricate. Figure 5.4 shows the measured ASE spectra out of the amplifier with a 7° angled interface width different current levels. The amplifier length is 2000 µm. The ASE spectra exhibit a lot of ripples as well as a slow envelope with a period of ~8 nm indicating that there is a cavity formed by two reflective interfaces. At higher current levels, this device even starts lasing because of a long active region.

Figure 5.4. ASE spectra from a 2 mm long amplifier with different current levels.
To extract the reflectivity of the interface, the FP responses in the spectra are analyzed. Gain-reflectivity product ($b$) is extracted from the ASE spectra, using the Fourier transform analysis technique [1]. Details for the numerical manipulation of this technique can be found in Ref. 2. The gain-reflectivity product is defined in Eq. 5.1. Since there are two unknown terms (Reflectivity and modal gain) in the equation, usually multiple gain-reflectivity products need to be measured with different device lengths at the same current density to extract the two parameters. The terms used in this analysis are defined in Fig. 5.5 (a).

$$ b = R_{\text{eff}}(\lambda)e^{i\tau(\lambda)L} \quad \text{Eq. 5.1} $$

In the case of this device, $R_{\text{eff}}$ is a function of wavelength since there are two reflected beams from the silicon waveguide and the amplifier interface respectively and the phase difference between those beams is wavelength dependant. If it is assumed that the reflection of the silicon passive waveguide mode is negligible ($R_1' = 0$) with 100% coupling efficiency at the amplifier interface ($T_1$ and $T_1' = 1$), then the maximum and the
minimum $R_{\text{eff}}$ occur in the condition of in-phase and out-of-phase as written in Eq. 5.2 and 5.3.

$$R_{\text{eff, max}}(\lambda) = (\sqrt{R_1} + \sqrt{R_2})^2$$  \hspace{1cm} \text{Eq. 5.2}$$

$$R_{\text{eff, max}}(\lambda) = (\sqrt{R_1} - \sqrt{R_2})^2$$  \hspace{1cm} \text{Eq. 5.3}$$

**Figure 5.6.** (a) Gain-reflectivity product of a 2 mm long amplifier (b) Gain-reflectivity products from a peak and valley with three different device lengths. Dotted lines are fitting curves using Eq. 5.1.

Figure 5.6(a) shows the gain-reflectivity product (b) from the ASE spectrum of a 2000 µm long device at 200 mA (2500 A/cm$^2$). The gain-reflectivity product has a slowly varying envelope because of the coupled cavity effect. Figure 5.6(b) shows the peak (in phase) and the valley (out of phase) of the gain-reflectivity products near 1575 nm from devices with different lengths of 800 µm, 1200 µm and 2000 µm at a current density of 2500 A/cm$^2$. Assuming gain per unit length is the same for those devices, the effective reflectivity and the net modal gain can be extracted by fitting the data to Eq. 5.1. From the peak gain-reflectivity products, the maximum effective reflectivity ($R_{\text{eff, max}}$) and the net modal gain are estimated to be 0.016 and 10.7 cm$^{-1}$ while the minimum
effective reflectivity ($R_{\text{eff, min}}$) and the net modal gain are estimated to be 0.0037 and 9.1 cm$^{-1}$ from the valleys near 1575 nm. The reflectivity of each interface ($R_1$ and $R_2$) can be calculated using Eq. 5.2 and 3.

The calculation yields two reflectivity values of 3.1x$10^{-3}$ and 2.4x$10^{-4}$. Empirically, reflectivity from an AR coated, 7° angled silicon waveguide is $\sim$10$^{-3}$ $\sim$ 5x10$^{-4}$. Therefore, 3.0x$10^{-3}$ is a reasonable value for junction reflectivity. This analysis also explains lasing of a 2000 µm long device. Even though each interface has a reflectivity of an order of 10$^{-3}$, the coupled cavity enhances the effective reflectivity up to 0.014 when two reflected signals are in-phase. The mirror loss with a reflectivity of 0.014 is 20.7 cm$^{-1}$ for a 2000 µm long device which can be reached by the modal gain from the active region (See Fig. 3.12(b) in Chapter 3).

![Image](image_url)

**Figure 5.7.** (a)Transmission at the junction with different junction angles (b) Reflection at the junction with different junction angles (c) simulated beam propagation. Input is the fundamental mode of the hybrid waveguide from the left side.
Figure 5.7 shows the reflection and the transmission as a function of interface angle between the silicon passive waveguide and the hybrid waveguide calculated by Fimmwave™. As shown in Fig 5.7(a), the transmission between the fundamental modes follows the silicon confinement factor (~63%). When the fundamental mode of the silicon passive waveguide is coupled to the hybrid waveguide modes, the higher order modes are also excited and they continue to be guided by the III-V mesa structure. However, when these higher order modes are coupled back to the silicon passive waveguide, they end up coupling to radiative modes through the air interface. As a result, this higher order mode coupling results in coupling loss which is detrimental for the amplifier. Fig. 5.7(b) shows the reflection characteristics with the angled interface. The reflection of the hybrid waveguide mode at the interface is orders of magnitude higher than that of the passive waveguide mode since the hybrid waveguide mode has some portion of the optical mode in the III-V layers and it experiences abrupt refractive index change at the interface between the air and the III-V layers. Figure 5.7(c) shows the simulated beam profile when the fundamental mode of the hybrid waveguide is launched from the left side. It is clearly seen that a standing wave is formed because of the reflected beam at the interface. The reflectivity of the fundamental mode of the hybrid waveguide with a 7° angled interface is calculated to be $2.2 \times 10^{-3}$. The discrepancy between the experimentally measured reflectivity and the theory can be attributed to several factors. First, the model used in the analysis assumes the input and output silicon waveguides have the same length, but some devices have a slightly
different input and output waveguide length resulting in a different in-phase and out-of-phase condition for each side. Second, the fabricated junction is not exactly at a 7° tilt (limited by the contact lithography process) and its shape is slightly bowed inwards, which also can cause some deviation from the theory. However this analysis is sufficient to show the limitation of the abrupt junction design and to understand the lasing behavior of the long amplifier.

5.1.2.2 Tapered Junction

Because of the poor performance of the tilted junction, adiabatic III-V tapers are investigated. Figure 5.8 shows the parameters which affect taper performance. The final width and length of the taper needs to be designed properly through beam propagation simulations. The width and the position of the taper tip will be determined by fabrication accuracy.

![Diagram of a taper and its design parameters](image)

**Figure 5.8.** Schematic of a taper and its design parameters.
To determine a final width for the taper, modal index and confinement factors of the fundamental mode of the hybrid waveguide are calculated as a function of the III-V mesa width. As shown in Fig. 5.9 (a) and (b), a III-V mesa wider than 4 µm doesn’t affect the optical mode laterally. Therefore, the final width of the taper ($W_0$) doesn’t have to be as wide as the III-V mesa of the amplifier ($W_A$, 14 µm). A width of 4 µm is chosen to be the final width ($W_0$) and then the mesa width is abruptly changed to a mesa width of 14 µm ($W_A$) in the simulations. The calculated transmission between the fundamental modes of the silicon waveguide and the hybrid waveguide as a function of taper length is shown in Fig. 5.10(a). Theoretically almost 100 % of efficiency is achievable between the fundamental modes with a taper length more than ~50 µm. Other higher order mode excitation is suppressed to less than 5 % as shown in the same figure. Reflection is also calculated and the results are shown in Fig. 5.10(b). The reflection with a III-V taper is greatly reduced ($< 10^{-5}$) which is roughly three orders of magnitude lower than the abrupt junction design. The simulations assume the taper tip
has zero width and is positioned at the center of the silicon waveguide. The simulated beam propagation profile in Fig. 5.10(c) clearly shows the effectiveness of the taper to couple one fundamental mode to the other mode without any significant radiation loss and reflection.

![Simulation results](image)

**Figure 5.10.** (a) Transmission at the junction with different taper lengths (b) Reflection at the junction with different taper lengths (c) simulated beam propagation through an 80 µm long taper. Input is the fundamental mode of the hybrid waveguide from the left side.

To account for fabrication tolerance, the coupling efficiency is also calculated with different tip widths and tip positions. The calculation shows that the coupling efficiency doesn’t decrease much up to a tip width of 0.3 µm and a tip position of 0.2 µm for a 70 µm long taper while a 50 µm long taper shows more dependency on the width and the position of the tip as shown in Fig. 5.11. An alignment accuracy of the stepper is
typically +/- 0.3 µm and the tip width becomes ~ 0.2 µm after the lithography. Therefore, the loss induced from the lithographical accuracy should not be significant. Additionally, the dry etched side wall of the III-V taper can also induce additional scattering loss which may dominate the actual taper loss.

In the final fabricated device, the taper design is chosen at the junction of the silicon waveguide and the hybrid waveguide. The width of the III-V mesa is tapered from 0 µm to 4 µm over a length of 70 µm while the width from 4 µm to 14 µm is tapered more abruptly over 5 µm. The performance of the fabricated taper will be discussed in Section 5.2.

![Graphs showing coupling efficiency with tip position variation and different tip width.](image)

**Figure 5.11.** (a) Coupling efficiency with tip position variation. (b) Coupling efficiency with different tip width.

### 5.1.3 High Speed Detector Design

#### 5.1.3.1 Lumped Detector Bandwidth

In the previous chapter, the bandwidth of the first generation detector is limited by the capacitance from the III-V mesa as well as the pad design. The total capacitance
of the device can be divided into two components; junction capacitance and pad capacitance. The junction capacitance is determined by the area and the thickness of the undoped quantum well layer while the pad capacitance is determined by the thickness of the pad layer and the overlapped area between the p probe pad and the n layer as written in Eq.5.4.

\[ C = C_j + C_p \]

\[ = \frac{\varepsilon_i}{t_i} WL + \frac{\varepsilon_{pad}}{t_{pad}} A_{pad} \]

Eq. 5.4

where \( \varepsilon_i, \varepsilon_{pad}, t_i, t_{pad}, A_{pad}, W \) and \( L \) are dielectric constant of the intrinsic layer (SCH and QWs), dielectric constant of the pad layer, intrinsic layer thickness, pad layer thickness, pad area, width of the quantum well layer and length of the quantum well layer respectively. The intrinsic layer includes the undoped quantum wells and the depleted portion of the SCH layer.

**Figure 5.12.** (a) Calculated band diagram at reverse bias voltage of 8 V. (b) Calculated depletion region thickness.
As shown in Fig 5.12(a), the current 250 nm thick SCH layer is not fully depleted up to a reverse bias of 8 V and the thickness of the depleted region increases as the reverse bias voltage increases. The calculated intrinsic layer thickness with different biases is shown in Fig. 5.12(b).

**Table 5.1. Material properties of the quantum well layer and insulation layers.**

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant ($\varepsilon_r$)</th>
<th>Refractive index (n) @1550 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic layer</td>
<td>12.4</td>
<td>1.57</td>
</tr>
<tr>
<td>SU-8 (3015)</td>
<td>3.28</td>
<td>1.57</td>
</tr>
<tr>
<td>BCB</td>
<td>2.6</td>
<td>1.543</td>
</tr>
<tr>
<td>Silicon Nitride</td>
<td>7.5</td>
<td>2.05</td>
</tr>
</tbody>
</table>

**Figure 5.13.** (a) Calculated junction capacitance as a function of device length with different widths of III-V mesa (b) Calculated pad capacitance (c) Calculated series resistance.
Figure 5.13(a) and (b) show the calculated junction and pad capacitance respectively using Eq. 5.3 at a reverse bias of 4 V. The pad layer is changed from a 450 nm thick SiN layer in the first generation detector to a ~5 µm thick SU-8 (3015) layer. Table 5.1 summarizes material properties used in the calculations as well as the properties of benzocyclobutene (BCB) and SiN for comparisons. SU-8 can be easily spun with a thickness of 5 ~ 6 µm and has lower dielectric constant than a SiN layer. For a circular pad with a diameter of 50 µm the resulting pad capacitance is smaller than 0.01 pF. Figure 5.13(c) shows the calculated series resistance which is scaled from the measured series resistance of a 400 µm long device. It is assumed that the resistance only varies with the device length not the width of the quantum well layer.

From the estimated capacitance and series resistance, the estimated RC limited bandwidth with a 50 Ω load is calculated and the results are shown in Fig. 5.14(a). In general, the bandwidth is higher with a shorter device length because of a smaller capacitance. However, there is a roll-over point because a high series resistance from a short device starts to limit the bandwidth. Even though a shorter device is necessary for a higher device bandwidth, a reduced length will decrease the quantum efficiency of the photodetector. Figure 5.14(b) shows the calculated quantum efficiency as a function of a device length. The measured material absorption of 1594 cm⁻¹ at 1550 nm under no bias is used for this calculation. It is assumed that only the fundamental mode of the hybrid waveguide is excited with a quantum well confinement factor of 4 %. Figure 5.15 shows a contour plot of the width of the quantum well layer in the plane of the quantum efficiency and the RC limited bandwidth.
Figure 5.14. (a) Calculated RC limited bandwidth for different III-V mesa widths as a function of device length (b) Calculated quantum efficiency as a function of device length. A 50 Ω termination is assumed.

Figure 5.15. Contour plot of constant device width in the quantum efficiency-RC limited bandwidth plane. A 50 Ω termination is assumed.

To overcome the trade-off between the bandwidth and the quantum efficiency of lumped detectors, traveling wave electrodes can be employed. By matching an electrical velocity with an optical propagation velocity, the device can operate without being
limited by RC response. Consequently, the device length can be increased for a high quantum efficiency [3].

5.1.3.2 Detector Interface Design

Since the mesa width of the detector is narrower than the amplifier mesa width, the mode coupling at the interface between the silicon passive waveguide and the hybrid detector waveguide is different and needs to be investigated as well. The III-V taper can be used in the detector waveguide, but this additional taper length will add extra device capacitance. The abrupt junction can be more suitable for detectors, since the excited higher order modes can contribute to photocurrent. Additionally, the diffusion process is suppressed by narrowing down the mesa width. The III-V mesa width at the quantum well layer and the SCH layer is 2 µm while the InP cladding is 3 µm wide. As shown in Fig. 5.16, more than 94% of the fundamental mode of the silicon waveguide is coupled to the hybrid waveguide including the fundamental mode and the higher order modes in the hybrid waveguide.

![Mode coupling at the detector interface](image)

**Figure 5.16.** Mode coupling at the detector interface (7° tilted abrupt junction).
5.2 Device Characteristics

5.2.1 Device Fabrication

The amplifier has a very sharp and narrow taper tip where electrical current needs to be injected. Therefore, metal deposition after etching the III-V mesa is not desirable because the alignment error from the lithography can leave some region without metal contacts. Additionally, misalignment may cause the metal to fall off from the mesa resulting in possibly shorting the device. In order to pump the taper region efficiently without shorting the device, the self-aligned process is used for device fabrication. After the bonding process is completed and the InP substrate is removed, the P metal stacks are deposited. A gold layer is kept to be thin (100 nm) in order to enable this layer to be wet etched without a significant undercut. After depositing a SiN hardmask, the metal layers are etched. First, the gold layer is wet etched and then the Pd/Ti/Pd layers are dry etched by a mixture of Cl₂ and Ar. Since this dry etch process also etches the III-V layers, the etch process is closely monitored by a laser to stop at the right point. After the metal etching is finished, the device undergoes the standard III-V layer etching and metal deposition process. Figure 5.17(a) shows the etched InP substrate with the self aligned process. The edge of the gold layer is rounded because of the undercut from the wet etch but the other metal layers still hold the shape of the original mask. Figure 5.17(b) shows the etched taper structure using this process. It can be seen that the the taper tip approaches the limit of the stepper resolution (~0.2 μm). The self aligned process also enables the fabrication of a narrow mesa structure for the detectors. A 3 μm wide mesa is etched using the self-aligned process and quantum well
layers are further narrowed by using a selective wet etching process. The final width of the quantum well layer is ~2 μm. A SEM image of the detector cross section is shown in Fig. 5.17(c). As shown in the figure, SU-8 layer is used both as a pad layer as well as a mechanical support for the thin n layers.

![SEM images of the detector cross section](image)

**Figure 5.17.** SEM images of (a) a dry etched III-V mesa using self aligned process. (b) a III-V taper. (c) cross section of a detector.

Scanning electron micrograph (SEM) images of the final fabricated amplifier and photodetector are shown in Fig. 5.18(a) and close-up views of the two different device junctions are shown in Fig. 5.18(b) and 5.18(c), respectively. In the taper region, the width of the III-V mesa is tapered from 0 μm to 4 μm over a length of 70 μm and the width from 4 μm to 14 μm is tapered more abruptly over 5 μm since III-V mesas wider than 4 μm do not laterally affect the optical mode as mentioned in the previous section. The detector p and n pads are designed to be 100 μm apart from center to center to use
a standard GSG RF probe for high speed testing. The silicon input and output waveguide facets are AR coated with a single layer of Ta₂O₅ (~5 % reflectivity).

![SEM images](image)

**Figure 5.18.** SEM images of (a) eight fabricated devices (b) III-V taper of the amplifier (c) 3 µm wide III-V mesa of the detector. Images were taken before the p-probe metal deposition.

### 5.2.2 Detector Performance

The quantum efficiency of the photodetector is measured first by launching the light to input 2 (See Fig. 5.1) and measuring the generated photocurrent with a Keithley 2400 source meter. Figure 5.19(a) shows the measured internal quantum efficiency for TE polarization at 1550 nm and 1575 nm as a function of detector reverse bias voltage for a 100 µm long device. A coupling loss of 5 dB is used to estimate the input power from a lensed fiber. The coupling loss is measured from an insertion loss of a silicon passive waveguide with the same dimensions as the input and output silicon waveguide.
of the device. The internal quantum efficiency is in the range of 50% to 55% with bias voltages between -2 to -4 V. The TE spectral response is shown in Fig. 5.19(b). The edge of the spectral response red-shifts with increased reverse bias, while the absorption at the shorter wavelengths slightly decreases due to the quantum confined stark effect. Figure 5.20 shows the measured quantum efficiency at 1550 nm with varying device lengths. Detectors with three different lengths are fabricated and two different junction designs are employed for each length. The III-V taper is 20 µm long for the detectors to minimize additional capacitance. As shown in the figure, the tapered junction shows slightly better or similar internal quantum efficiency. This small difference can be attributed to the possibility that the actual loss from the fabricated tapers is comparable to the radiation loss at the abrupt junction.

![Graphs showing quantum efficiency and spectral response](image)

**Figure 5.19.** (a) Quantum efficiency as a function of reverse bias at 1550 nm and 1575 nm (b) Spectral response for TE polarization.
Figure 5.20. Measured internal quantum efficiency with various device lengths and junction designs at 1550 nm. The dotted line is calculated quantum efficiency with a material absorption of 1594 cm$^{-1}$ and a quantum well confinement factor of 4%.

The dark currents for three different device lengths are shown in Fig. 5.21. Dark current decreases as the device becomes shorter and varies from 62 nA to 422 nA for a 100 μm long device with a reverse bias voltage of 1V to 4V. The measured dark current is higher than typical dark currents of III-V photodetectors. This can be attributed to the conductivity of native Indium oxide. Native oxide removal prior to spin coating a SU-8 layer can help to decrease the dark current. Device capacitance is measured with different bias voltages by the network analyzer and the results are shown in Fig. 5.22(a). For a 100 μm long device, the measured capacitance is 0.16 pF with a reverse bias voltage of 4V, and in general the measured capacitances show good agreement with the calculated capacitances in Fig. 5.13(a). In the same figure, the series resistances are also plotted in the secondary y-axis showing that they scaled with a device length. Figure 5.22(b) shows the calculated RC limited bandwidth with the measured capacitance, the
series resistance and a 50 Ω termination. The devices have an estimated RC limited bandwidth higher than 10 GHz. This agrees with the calculations shown in Fig. 5.14.

![Graph showing dark current as a function of device length with bias voltages.](image)

**Figure 5.21.** Dark current as a function of device length with bias voltages.

![Graphs showing measured capacitance and series resistance at a reverse bias voltage of 4 V and estimated RC limited bandwidth calculated from the capacitance and the series resistance with a 50 Ω termination.](image)

**Figure 5.22.** (a) Measured capacitance and series resistance at a reverse bias voltage of 4 V (b) Estimated RC limited bandwidth calculated from the capacitance and the series resistance with a 50 Ω termination.

### 5.2.3 Amplifier Performance

The chip gain of the amplifier for a 1240 μm (1100 μm + two tapers) is measured by launching the signal to Input 1 (See Fig. 5.23(a)). The coupled input power
to the amplifier is calibrated using a coupling loss of 5 dB. By measuring the photocurrent out of the detector, the amplifier chip gain is calculated using Eq. 5.5

\[
G = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_p}{P_{\text{in}}R} \quad \text{Eq.5.5}
\]

where \( R \) is the measured responsivity of the detector shown in 5.19 (a).

Figure 5.23(a) shows the measured chip gain at 1550 nm and 1575 nm. Figure 5.23(b) shows the net modal gain as a function of a current density. The quantum well confinement factor (\( \Gamma_{\text{QW}} \)) and the waveguide loss (\( \alpha_i \)) are assumed to be 4% and 15 cm\(^{-1}\) respectively. The fitting the data to the logarithm function yields a gain coefficient (\( g_0 \)) and a transparent input current density (\( J_{\text{tr}}/\eta_i \)) of 702 cm\(^{-1}\) and 1120 A/cm\(^2\) at 1575 nm respectively. At 1550 nm, the gain coefficient and the transparent input current density are 1190 cm\(^{-1}\) and 1815 A/cm\(^2\). Even though the gain coefficient is higher at 1550 nm, the maximum chip gain occurs at a longer wavelength because its transparent current density is higher and the thermal effect becomes significant beyond this current density. The transparent current density of the current device is higher than
the 1st amplifier described in Chapter 3 because the depth of the proton implantation profile is shallower than that of the 1st amplifier. With the same implantation energy, its projection depth in the current device is shallower because of a 100 nm thick gold layer. The gain peak occurs at 1570 nm and the 3 dB gain bandwidth is ~60 nm at 300 mA as shown in Fig. 5.24.

**Figure 5.24.** The amplifier gain spectrum with three different currents.

### 5.2.4 Taper Performance

Reflection of the fabricated tapers is analyzed by measuring the ASE spectrum from the amplifier. The ASE spectra from the amplifier are shown with three different currents in Fig. 5.25. The tapered junction reflectivity is estimated by measuring the ripples of the Fabry-Perot response of the amplifier ASE. Although the ASE spectrum shows no clear Fabry-Perot cavity response, the maximum ripple due to noise at 300 mA (a chip gain of 9.5 dB) is 0.1 dB which corresponds to a maximum reflectivity of $6 \times 10^{-4}$. 

118
To estimate the loss from the III-V taper, the responsivity of the amplifier under reverse bias is analyzed. The responsivity of the amplifier under reverse bias is measured to be $1.06 \sim 1.15$ A/W in the wavelength range of 1530 nm to 1580 nm. This corresponds to an internal quantum efficiency of $86 \sim 90\%$. Since the amplifier is long enough to absorb all of the light coupled to the hybrid waveguide in the short wavelength range, this indicates that the taper loss is $\sim0.6$ dB for this particular device as shown in Fig. 5.26 and it is typically $0.6 \sim 1.2$ dB. The fabricated taper length is 70
µm long and the additional loss measured through the taper can be attributed to side wall roughness and the blunt tip of the taper.

**5.2.5 Integrated device performance**

The overall responsivity of the integrated device is measured by launching the input signal to Input 1 and measuring the photocurrent out of the detector after pre-amplification. The chip gain of the amplifier is 9.5 dB and the reverse bias voltage of the detector is -4 V. The input wavelength is 1550 nm. The overall responsivity of the receiver before saturation is 5.7 A/W and the device is saturated by 0.5 dB at an output photocurrent of 25 mA as shown in Fig.5.27. The x-axis of the graph shows the coupled input power taking into account the 5 dB coupling loss. The dark current of the receiver due to the ASE noise from the amplifier is 25 µA at an amplifier current of 300 mA. An output photocurrent of 25 mA corresponds to an output power of ~16 dBm from the amplifier and this indicates that the 3 dB output saturation power of the amplifier is greater than 16 dBm. This is significantly higher than the 3 dB output saturation power of the previous device. This improvement originates from the saturation of the gain at high current density. Around a current level of 300 mA, the gain is almost saturated and less sensitive to the carrier density change in the active region. This reduces $dg/dN$ in Eq. 3.6. From the measured $dg/dJ$, $dg/dN$ is estimated to be $\sim 4.8 \times 10^{17}$ cm$^2$ at 300 mA if the injection efficiency is 60 %. This yields a 3 dB output saturation power of 18 dBm using Eq. 3.6.
Figure 5.27. Saturation characteristics of the receiver.

Figure 5.28. (a) Impulse response with different input powers at a reverse bias of 4 V (b) Fourier transform of the impulse response.

The impulse response of the detector is measured by launching 600 fs short pulses with a 20.1 MHz repetition rate from a mode-locked fiber laser to input 2 (See Fig.5.1). A 40 GHz RF probe connected to a 26 GHz bias-tee is used to collect the photo current. The signal is fed into a 50 GHz digital communications analyzer to sample the pulse. The response exhibits a rising time (10 - 90 %) of 18 ps. Figure 5.28(a) shows the impulse response measured with six different input pulse power levels. The
long tail of the response indicates that carrier transport, especially hole transport, limits the device bandwidth. The Fourier transform of the impulse response is shown in Fig. 5.28(b) and the 3 dB bandwidth is estimated to be ~3 GHz.

The current quantum wells have a valence band offset of ~105 meV between the well and the barrier, which causes hole trapping and electrical field screening. To investigate the dependence of the impulse response on the input power and the reverse bias voltage, the each measured impulse response is normalized by the total pulse energy. Figure 5.29(a) shows the impulse response with different pulse power at a reverse bias of 4 V. For both input pulse powers, the tail is still significant, but it is reduced at a lower input power. This can be attributed to the electrical field screening from the trapped carriers [4]. In Fig. 5.29 (b), two normalized impulse responses are plotted with different bias levels. Even though the tail reduces at a higher reverse bias value, it still limits the device speed. Further investigations on different quantum well design and/or different layer thickness needs to be pursued to improve the device speed.
Figure 5.30. (a) Eye diagrams of 2.5 Gb/s and 5 Gb/s PRBS input signal. (Top) with the amplifier (bottom) without the amplifier (b) Bit error rate curves measured with $2^{31}-1$ NRZ 2.5 Gb/s transmissions with different amplifier gains.

Figure 5.30(a) shows eye diagrams measured at non-return-to-zero (NRZ) 2.5 Gb/s and NRZ 5 Gb/s collected directly with a GSG probe and fed through 37 dB electrical amplification. The top two eye diagrams are measured after the signal is amplified (9.5 dB gain) through input 1 while the bottom two eye diagrams are directly detected without amplification by launching the signal to input 2 (See Fig. 5.1). The Q factors of the eye diagrams detected without the amplifier is slightly higher than the ones after the amplification at the same photo current level, e.g. 7.7 vs 8.4, because of the additional ASE noise. The eye diagrams are open for modulation up to 5 Gb/s NRZ.

The bit error rate (BER) was measured with a 2.5 Gb/s NRZ $2^{31}-1$ pseudorandom bit sequence (PRBS) with different amplifier gains and the results are shown in Fig. 5.30(b). The purple data points are baseline measurements without the
amplification by launching the signal to input 2. The BER data at an amplifier current of 100 mA shows worse receiver sensitivity than the receiver sensitivity without amplification (baseline) because the amplifier operates below the transparency. Once the amplifier is driven beyond transparency, the power penalty becomes negative as shown in the three BER curves on the left side. At the maximum gain of 9.5 dB, the power penalty is -8.5 dB compared to the baseline and the receiver sensitivity at a BER of $10^{-9}$ is -17.5 dBm. The 1 dB difference between the gain and the measured power penalty is due to the ASE noise. This is slightly higher than the power penalty of 0.5 dB from the previous measurements (Chapter 3) because of lack of a bandpass filter. Better sensitivities would be achievable with a good transimpedance amplifier and a proper electrical termination.

5.3 SUMMARY

This chapter presented the integration of preamplifiers with photodetectors. The overall device responsivity after pre-amplification is 5.7 A/W. The integrated preamplifier has a maximum gain of 9.5 dB and the detector has ~50 % internal quantum efficiency with a quantum well confinement factor of 4 %. The detector bandwidth is 3 GHz even though measured capacitance and resistance indicate a RC limited bandwidth of ~ 10 GHz. The impulse response shows that there is a long tail after the falling edge of the pulse which primarily limits the device bandwidth. This can be attributed to the current quantum well design wherein carriers are trapped before collection. BER measurements are done with 2.5 Gb/s NRZ data and the receive sensitivity is improved
by 8.5 dB (compared to the sensitivity without the pre-amplification). A III-V taper is incorporated at the junction between the silicon waveguide and the hybrid amplifier waveguide to minimize reflection and increase coupling efficiency. The fabricated taper shows an estimated loss of 0.6 dB and a reflection of less than $6 \times 10^{-4}$. To improve the device speed, several different designs of the quantum wells and layer thicknesses need to be investigated. Further, a traveling wave design can be employed to overcome RC limitations.
5.4 References


Chapter 6  Integrated Optical Buffer

Optical buffers are one of the important components to realize all optical packet switched network to address contention and congestion of optical packets. Various types of optical buffering technologies have been demonstrated including silicon coupled resonators [1], photonic crystals [2], fiber delay lines [3, 4]. The first two approaches can be categorized into feed-forward buffers based on slow light technology while the last two approaches are based on feed-back buffers consisting of a recirculating delay line and an optical switch. The feed-back buffers offer several advantages over other approaches in terms of compact integration and large delay [5] even though a fixed delay line length sets some restrictions of a minimum delay and a maximum packet length.

This chapter presents an integrated recirculating optical buffer consisting of a low loss silicon waveguide delay line and a silicon evanescent gate matrix switch. This chapter begins by device layout and design of low loss silicon delay lines as well as other passive components such as MMI splitters and waveguide crossings. Next, the performance of the integrated optical buffer is presented.

The demonstrated device is implemented with an 8 cm long delay line, silicon evanescent gate matrix switch and four silicon evanescent amplifiers. A 2x2 gate
matrix switch is chosen over interferometer based switches because it provides low
crosstalk and high extinction ratio which are important metrics for cascadability [6].
The demonstrated gate matrix switch has a DC crosstalk and a DC extinction ratio of
34 dB and 41 dB respectively. The switching time of ~3.4 ns is primarily limited by the
electrical reflections between the device and the driving electronic circuit. The
integrated optical buffer shows a packet delay of 1.1 ns controlled by the gate matrix
switch with a power penalty of 2.4 dB.

This demonstration illustrates the ability of the silicon evanescent device
platform to realize new type of photonic integrate devices by combining low loss
silicon passive components and the silicon evanescent devices.

6.1 DEVICE LAYOUT

Figure 6.1(a) shows a layout of the integrated optical buffer. This is a typical
recirculating optical buffer consisting of a silicon delay line and a gate matrix switch
with additional boost amplifiers. Once optical packets are routed into the delay line,
they are stored in the delay line for multiple recirculations. The gate matrix switch
controls how long the stored packets will stay in the recirculating loop. The buffering
time is multiple of the minimum delay determined by the length of the recirculating
loop. The 2x2 gate matrix switch consists of two MMI splitters and four switching
amplifiers. Input packets are split into two output ports and one of the split signals is
gated by the amplifiers to a desired output port as illustrated in Fig. 6.1(b). Since this is
based on broadcasting-and-selection method, there is an inherent loss of 6 dB from the
input splitters and the output combiners. However this loss can be compensated from
the optical gain of the switch amplifiers. The gate matrix switches are beneficial to high cross talk suppression and high extinction ratio from the high absorption by reverse-biasing the amplifiers. However, the amplifiers need to be designed properly to ensure the operation with a low power penalty due to the ASE noise.

**Figure 6.1.** Device layout (a) integrated buffer (b) gate matrix switch. The cross-over operation is illustrated as an example.
6.2 Passive Components

This section will present the design and evaluation of passive components implementing the optical buffers. The loss characteristics of very long delay lines are studied with several waveguide dimensions and different fabrication techniques. Other passive components such as MMI splitters and waveguide crossings are discussed as well.

6.2.2 Silicon delay line

The low loss waveguide is a critical component to achieve a long buffering time without significant signal degradations. Figure 6.2 shows the possible delay with different silicon waveguide lengths using Eq. 6.1.

\[ t_d = \frac{n_g L}{c} \]  

Eq. 6.1

where \( n_g, L \) and \( c \) are a group index, a waveguide length, and a speed of light (3\( \times 10^8 \) m/s) respectively. A group index of 3.68 is used for the calculation, which is estimated from the wavelength dependent transmission of the ring resonators with similar waveguide dimensions [7]. As shown in the figure, a delay of ~ 10 ns can be achieved with an 82 cm long silicon waveguide. A delay around 10 ns is interesting because more than 40% of the data packets in the internet traffic is 40 bytes~44 bytes [8] which corresponds to a packet length of 8 ns in 40 Gb/s transmission systems. A shorter delay around 1 ns (a waveguide length of 8 cm) is also attractive for the applications such as packet synchronizations [9]. In this work, two waveguide lengths of 114 cm and 7.6 cm are chosen to study the characteristics of waveguide loss.
Waveguide loss occurs when a waveguide mode is coupled to radiating modes (radiation loss) or is absorbed by a waveguide material (absorption loss). Since the absorption edge of silicon is near a wavelength of 1.1 µm, the absorption loss is negligible for transmissions at 1.5 µm wavelength regime. Hence, in many instances, the loss in the silicon waveguide is dominated by the radiation loss from the surface irregularities of the waveguide surfaces (scattering loss) and from the waveguide bends (bend loss) [10].

The scattering loss primarily depends on the side wall roughness created by the waveguide fabrication process. Roughness in the initial photoresist mask is transferred to the dielectric hard mask and sequentially transferred to the dry etched waveguide side walls. Additionally, a dry etching process induces more roughness on the etched surface. A number of different methods have been investigated to minimize sidewall
roughness including post exposure bake [11], side wall oxidation [12,13], and hydrogen annealing [14]. The theoretical treatment of the scattering loss has to consider the coupling between a guided mode to radiation modes at the irregular surface. The surface roughness is characterized by statistics using an autocorrelation function [15]. The autocorrelation function has two parameters to describe the surface roughness: 1) mean square deviation from a flat surface \( \sigma^2 \), 2) correlation length \( L_C \). Typically an exponential or a Gaussian function is used for an autocorrelation function.

For waveguide sidewalls defined lithographically, it is known that an exponential function describes their autocorrelation better [16]; hence, it is used in this work. According to the model developed by Payne and Lacey, the analytical expression of the scattering loss from rough side walls can be written as Eq. 6.2 using the exponential autocorrelation function [10].

\[
\alpha \ (cm^{-1}) = \frac{\sigma^2}{\sqrt{2k_0d^4n_i}} g(V)f(x, \gamma) \quad \text{Eq.6.2a}
\]

\[
g(V) = \frac{U^2V^2}{(1+W)} \quad \text{Eq.6.2b}
\]

\[
f(x, \gamma) = \frac{x\sqrt{(1+x^2)^2 + 2x^2\gamma^2} + 1-x^2}{\sqrt{(1+x^2)^2 + 2x^2\gamma^2}} \quad \text{Eq.6.2c}
\]

\( U, V, W, x, \) and \( \gamma \) are the normalized waveguide parameters or dimensionless combinations with the correlation length, the waveguide width and the surface roughness as defined by Eq. 6.3.

\[
U = d\sqrt{n_1^2k_0 - \beta^2}, \quad V = k_0d\sqrt{n_1^2 - n_2^2}, \quad W = d\sqrt{\beta^2 - n_2^2k_0} \quad \text{Eq. 6.3a}
\]
\[ x = W \frac{L_C}{d}, \quad \gamma = \frac{n_2 V}{n_1 W \sqrt{\Delta}}, \quad \text{where} \quad \Delta = \frac{n_1^2 - n_2^2}{2n_1^2} \]

Eq. 6.3b

where \( \sigma, k_0, 2d, n_1, n_2, \) and \( \beta \) are a standard deviation of the surface roughness, a free space wave number, a width of the waveguide, effective core index, effective slab index, and a propagation constant of a rib waveguide. Since this model is based on a two dimensional slab waveguide, the effective index model is used as shown in Fig. 6.3(a). In Eq. 6.2a, the first term, \( g(V) \), represents the optical mode overlap to the surface roughness and purely determined by the waveguide dimensions while the second term, \( f(x, \gamma) \), describes the relation between the correlation length and the beating length of the guided mode and the radiation mode. More detailed descriptions for the mathematical derivation of the equations can be found in Ref. 10 and its references.

Figure 6.3(b) shows the calculated scattering loss as a function of a waveguide width with different slap heights (etching depths) of 0.3 \( \mu \text{m} \) and 0.4 \( \mu \text{m} \). In the calculation the waveguide height is fixed at 0.7 \( \mu \text{m} \). The standard deviation of the surface roughness \( (\sigma^2) \) and the correlation length \( (L_C) \) is assumed to be 2 nm and 1 \( \mu \text{m} \) respectively. As shown in the figure, waveguides with a deeper etch have higher scattering loss from more overlap on the side wall. In addition it is interesting that the scattering loss is maximized near 0.2 \( \mu \text{m} \) wide waveguides and it decreases again as the waveguide width is reduced. This can be explained by the deconfinement of the optical modes with a modal index being very close to a cladding index [17]. It might be also worth pointing out that, in addition to the side wall roughness, the roughness at the
interfaces between different layers such as a waveguide clad and a core can contribute to the waveguide scattering loss.

Another major term of the waveguide loss is bend loss. In order to maximize the level of integration on a single chip, compact and low loss silicon waveguide bends are required. Low loss waveguide bends with 1 µm radius of curvature have been demonstrated with strip waveguides which have a large index contrast in the horizontal
plane [18]. The refractive index difference of a rib waveguide is relatively small in the horizontal plane, and thus the bend radius for a rib waveguide needs to be much larger than that of a strip waveguide. However, rib waveguides are preferable for the application of very long silicon delay lines because small strip waveguides have larger overlap of the optical mode in waveguide side walls resulting in higher scattering loss. Integration of a 100 cm long silicon delay line on a ~ 1 cm x 1 cm chip requires the number of 90° bends in the range of 50~100. To minimize the accumulated loss from many waveguide bends, the radius of the curvature needs to be determined carefully. The beam propagation method using Beamprop™ is employed to predict bend loss with different bend radii. Figure 6.4 shows radiation loss from 90° bends calculated as a function of a curvature radius for TE polarization. The y axis of the figure represents the accumulated bend loss from one hundred 90° bends. The silicon waveguide dimensions are summarized in the figure. The accumulated bend loss becomes less than 1 dB for a bend radius larger than 150 µm. This calculation only considers coupling to the TE slab modes. However, there is additional loss from the radiation loss through the TM slab mode coupling as well as scattering at the side walls [19]. Considering those additional terms contributing the bend loss, a bend radius 500 µm is chosen for the layout of the actual recirculating loop to stay on a conservative side.
To study the effect of waveguide dimensions and various fabrication techniques (side wall oxidation, post exposure bake and etching chemistry) on the waveguide loss, five samples are prepared with different fabrication conditions and waveguide dimensions as summarized in Table 6.1. The waveguide loss is characterized by the insertion loss measurement. The loss measurement from these long waveguides enables a small difference in a waveguide loss to be distinguished by reducing the uncertainty induced by the coupling loss variation. For example, a measurement resolution can be less than 0.01 dB/cm for a coupling loss variation of 1 dB. The input/output waveguides are 7° tilted to the normal direction of the facet and AR-coated to minimize the reflections. Additionally, their waveguide width is tapered to 2 µm to keep the coupling loss the same. The waveguide height is fixed at 0.7 µm in order to incorporate the same design of the silicon evanescent amplifiers described in the previous chapters. The minimum 90° bend radius is 500 µm. The sample sizes with
a 114 cm long loop and a 7.6 cm long loop are 1 cm x 1.5 cm and 0.3 cm x 0.3 cm respectively. To integrate multiple silicon delay lines on a limited space, four loops are interleaved as shown in Fig. 6.5.

Table 6.1. Waveguide dimensions and fabrication conditions used for the waveguide loss characterization.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Waveguide height (µm)</th>
<th>Slab height (µm)</th>
<th>Width (µm)</th>
<th>Length (cm)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.7</td>
<td>0.4</td>
<td>1.4, 1.6, 1.8, 2.0</td>
<td>114</td>
<td>Cl₂/Ar/HBr dry etch</td>
</tr>
<tr>
<td>2</td>
<td>0.7</td>
<td>0.4</td>
<td>1.4, 1.6, 1.8, 2.0</td>
<td>114</td>
<td>Cl₂/Ar/HBr dry etch, smoothing oxidation</td>
</tr>
<tr>
<td>3</td>
<td>0.7</td>
<td>0.4</td>
<td>1.4, 1.6, 1.8, 2.0</td>
<td>114</td>
<td>Cl₂/Ar/HBr dry etch, post exposure bake</td>
</tr>
<tr>
<td>4</td>
<td>0.7</td>
<td>0.3</td>
<td>1.4, 1.6, 1.8, 2.0</td>
<td>114</td>
<td>Cl₂/Ar/HBr dry etch</td>
</tr>
<tr>
<td>5</td>
<td>0.7</td>
<td>0.4</td>
<td>2.0</td>
<td>7.6</td>
<td>Cl₂ dry etch</td>
</tr>
</tbody>
</table>

Figure 6.5. SEM images of the fabricated 114 cm long silicon waveguides. 4 loops are interleaved.

The measured total loop loss is summarized in Table 6.2. The total loop loss is estimated by subtracting a coupling loss of 5 dB from the measured insertion loss. Figure 6.6 shows the measured waveguide loss as a function of waveguide width. The dotted lines plot an estimated scattering loss with different standard deviations of surface roughness. At each waveguide width, a maximum scattering loss is calculated in the range of the correlation length between 0.1 µm and 20 µm using Eq.6.2. The samples with smoothing oxidation process or the post exposure process show slightly
better waveguide losses of 0.3 ~ 0.35 dB/cm. The side wall roughness of Sample 5 (etched by pure Cl\(_2\)) has a standard deviation of surface roughness of 10 nm ~ 15 nm, and the measured waveguide loss agrees reasonably with the estimated maximum scattering loss. However, the waveguide losses of Sample 1, 2, 3 and 4 don’t agree with the estimated maximum scattering loss with a measured standard deviation of surface roughness of ~2 nm. This indicates that the losses of those samples are dominated by other sources such as the Si/BOX interface or some residual absorption. This is supported by the fact that Sample 2 (smoothing oxidation) shows only slight improvements in the waveguide loss even though it has been reported that the smoothing oxidation can reduce the roughness greatly down to ~0.3 nm [12]. It is shown that Sample 4 with a slab height of 0.3 µm exhibits higher loss (or similar) than Sample 1 with a slab height of 0.4 µm. This indicates that the waveguide loss is dominated by the scattering loss, not the bending loss. Two different dry etching processes are also investigated. The sample etched by pure Cl\(_2\) (Sample 5) has a higher waveguide loss (~0.9 dB/cm) than the samples etched by a mixture of Cl\(_2\)/Ar/HBr (Sample 1~4), primarily due to the rougher side walls from the unoptimized etching conditions.
Figure 6.6. Measured waveguide loss with different waveguide dimensions and processing conditions. Dotted lines are the calculated scattering loss with a slab height of 0.4 µm with a variation of standard deviation of surface roughness.

Table 6.2. Measured total waveguide loss. A coupling loss of 5 dB is assumed.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Width (µm)</th>
<th>1.4</th>
<th>1.6</th>
<th>1.8</th>
<th>2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>55.12 dB</td>
<td>55.12 dB</td>
<td>53.54 dB</td>
<td>42.32 dB</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>53.64 dB</td>
<td>51.66 dB</td>
<td>42.85 dB</td>
<td>35.94 dB</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>51.36 dB</td>
<td>51.66 dB</td>
<td>46.65 dB</td>
<td>41.03 dB</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>56.75 dB</td>
<td>55.86 dB</td>
<td>49.88 dB</td>
<td>47.05 dB</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>7 dB</td>
</tr>
</tbody>
</table>

6.2.3 Multimode Interference (MMI) splitter

Design of MMI couplers are based on the self imaging principle. Multiple optical modes excited in a multimode waveguide periodically reproduce an input mode profile as a single or multiple images as they are propagating through the waveguide [20]. This property is utilized to build power splitters or combiners. Typical MMI based devices have a wider multimode waveguide supporting a large number of guided modes interfaced with narrower input and output access waveguides. Figure 6.7 shows the operation of a 1x2 MMI splitter simulated by Beamprop™. It is shown that the
excited modes generate multiple images along the multimode waveguide as they are propagating (3 fold images at 60 µm and 2 fold images at 73 µm).

![Simulated beam propagation in a MMI splitter.](image)

**Figure 6.7.** Simulated beam propagation in a MMI splitter.

In order to achieve a desired split ratio with a low loss, the length of the multimode waveguide needs to be terminated at a proper imaging position which is determined by the propagation constants of the optical modes. Figure 6.8(a) shows the calculated transmission to output waveguides as a function of a multimode waveguide length of a 1x2 MMI splitter. The y axis represents the deviation from the ideal -3 dB transmission when the input power is unity. A width, a height and a slab height of the access waveguides are 2 µm, 0.7 µm, and 0.4 µm respectively. The basic loss mechanisms of MMI splitter are the diffraction loss of the input field at the multimode waveguide and the coupling loss between the multimode waveguide and the output waveguides [21]. As shown in the figure, the minimum loss of a 73 µm long splitter
with a width of 8 µm is estimated to be ~0.2 dB. Figure 6.8(a) also contains the calculated transmission of MMI splitters with widths of 7.5 µm, and 8.5 µm in order to estimate loss variation caused by the process bias (difference between the device dimensions on the mask and on the sample). A +/- 0.5 µm variations in length and width of the multimode waveguide can increase the loss up to 1.6 dB. The wavelength dependency of the transmission is shown in Fig. 6.8(b). A minimum loss around 0.2 dB can be achieved at a wavelength of 1570 nm and the spectral band width with a loss increase of 0.1 dB is 120 nm. In addition to the diffraction and the coupling loss, the inherent waveguide losses such as the scattering loss and the absorption loss exist in the device as well. Therefore with given design constraints, it is important to make the device length as short as possible. Figure 6.9 shows an SEM image of the MMI splitter fabricated for the gate matrix switch. The device dimensions are summarized in the same figure.

![Figure 6.8.](image.png)

**Figure 6.8.** Calculated 2x1 MMI splitter characteristics (a) loss variation as a function of a MMI length with different waveguide widths (b) loss variation as a function of a wavelength.
Figure 6.9. SEM images of the fabricated MMI splitters. (right) passive waveguides for the gate matrix switch including two MMI splitters. (left) close view of one of the splitters. The dimensions of the access waveguides are a width, a height and a slab height of 2 µm, 0.7 µm, and 0.4 µm.

6.2.3 Waveguide crossing

Electronic integrated circuits have many interconnect layers stacked vertically leading to flexible routing and high density integration. On the contrary, current photonic integrated circuits are mostly constricted to a single layer. Therefore, waveguide routings without many waveguide crossings would be difficult or impossible in complex photonic integrated circuits. Waveguide crossings between silicon waveguides require stringent design because their tightly confined optical modes experience more diffraction when they encounter intersecting waveguides. Various structures such as parabolic tapers [22] and multimode couplers [23] have yielded better loss and crosstalk performance for the silicon waveguides with dimensions in submicron range. However typical waveguide dimensions used in this work is larger than those silicon nano-wires and simulations suggests that direct crossings might be enough to provide sufficient performance with low loss and crosstalk.
The simulations are carried out for TE polarization using a 2 dimensional finite difference time domain method (FDTD). The effective index model is used to map the 3 dimensional rib waveguide index profile to 2 dimensional space to save computational time. Figure 6.10(a) shows the transmission across a waveguide crossing as a function of the angle between the two intersecting waveguides. The estimated loss is less than 0.2 dB with an angle between 50° and 80°. An angle of 60° ~ 80° is used in the device layout and a right angle crossing is avoided since the cross talk is increased due to the abrupt mismatch that the input field experiences [24]. Figure 6.10(b) shows a SEM image of the fabricated waveguide crossing with an angle of 60°.

![Figure 6.10](image)

**Figure 6.10.** (a) Simulated transmission as a function of an intersecting angle of two waveguides. (b) A SEM image of the fabricated waveguide crossing with an angle of 60°. The dimensions of the waveguides are a width, a height and a slab height of 2 µm, 0.7 µm, and 0.4 µm.
6.3 **DEVICE FABRICATION**

This section will go over several issues related to the fabrication of the optical buffers. The selective bonding process is outlined, by which the III-V material is bonded selectively in the region where the silicon evanescent amplifiers are fabricated. The modified III-V back end process, to fabricate the amplifiers with protecting the exposed silicon delay line region, is also presented.

### 6.3.2 Necessity of selective bonding

The surface change of the silicon waveguide by the bonding process is studied with atomic force microscopy (AFM) measurements. The half of a silicon waveguide sample is first bonded with III-V layers and then the bonded III-V layers are subsequently removed by the selective wet etching steps. AFM measurements are carried out to compare the surface roughness of the re-exposed silicon with another half of the silicon surface where the III-V layers are not intentionally bonded. Figure 6.11 shows 3 dimensional plots of the measured surface roughness. It is apparent that the silicon surface originally bonded with the III-V layers has a rougher surface. The standard deviation of this region is measured to be 0.356 nm (Fig. 6.11(b)), while the standard deviation of the other region is 0.254 nm (Fig. 6.11(a)).

The increased surface roughness can result in additional waveguide loss as it is described in Eq. 6.2. This incremental loss might be negligible if the total length of the waveguide is short. However, it could be significant for a very long waveguide. For example, a waveguide loss change of 0.1 dB/ cm can add 10 dB more loss for a 100 cm long waveguide. In order to avoid this possible problem and protect the silicon delay...
line during the III-V back end process, the bonding process is slightly modified such that the III-V layers are bonded only the amplifier and gate matrix switch region. Meanwhile, the silicon delay line region is covered and protected by a thick SiO₂ during the III-V process. The modified process flow is described in the next section.

![Figure 6.11](image-url)

**Figure 6.11.** (a) Surface roughness of the un-bonded silicon region (b) Surface roughness of the region bonded with III-V layers (III-V layers are subsequently removed.).

### 6.3.3 Modified process flow

Figure 6.12 shows the process flow of the optical buffers. After silicon waveguides are dry etched, a 0.5 μm thick SiO₂ layer is deposited on the silicon sample without removing a SiO₂ hard mask layer. Then, the silicon waveguide region for the amplifiers and the switch is exposed by wet-etching the SiO₂ layer by buffered HF. After cleaning procedure, a III-V sample is roughly aligned by tweezers and bonded on the opened silicon region. The SiO₂ on the delay line region serves as a protection layer from the scratches and any possible contaminations which can be caused by the bonding process.
Figure 6.12. Modified process flow for the delay line region protection.

Figure 6.13. (a) A microscope image of the silicon sample used for the optical buffer (b) III-V layer dry etched by the MHA process for amplifiers.
Figure 6.13(a) shows a microscope image of the silicon sample consisting of the delay line (spiral shape on the top right) and additional passive waveguides for the gate matrix switch. A 1.5 mm gap between the delay line region and the switch region is intentionally employed to have an enough tolerance when the III-V sample is aligned by tweezers. After anneal and InP substrate removal, the III-V layer for the amplifier and the switch is lithographically defined by the MHA dry etch process as shown in Fig. 6.13(b). Additional 0.5 µm thick SiO₂ layer is deposited for the protection of the silicon waveguides in the switch region. Then the SiO₂ layer on the III-V region is dry etched by CHF₃. Finally the amplifiers are fabricated using the self aligned process.

**Figure 6.14.** A SEM image of the cross section of the silicon waveguide after III-V processing is finished.
Figure 6.15. (a) SEM image of 8 integrated amplifiers (b) Microscope image of the fabricated device mounted on an AlN carrier.

The silicon waveguide in the delay line region is protected by ~1 µm thick SiO$_2$ layer. After all of the III-V processing is finished, ~0.7 µm thick SiO$_2$ layer still covers the silicon waveguides as shown in Fig. 6.14. This layer is also used as a waveguide cladding. Figure 6.15(a) shows SEM images of the fabricated amplifiers in the optical buffer. Four buffers are integrated with interleaved four delay lines with a waveguide width, a height and a slab height of 2 µm, 0.7 µm and 0.4 µm respectively. The fabricated device is mounted on an aluminum nitride (AlN) carrier and the electrical pads of the device are wire-bonded to the carrier for device probing using a probe card. An image of the mounted device is shown in Fig.6.15(b).

6.4 DEVICE CHARACTERISTICS

The loss of a 7.6 cm long delay line is first characterized using a simple single delay line structure, which is illustrated in Fig. 6.16(a). The delay line loss is measured using mode locked laser pulses. The input pulse from the mode locked laser is split into two pulses by a 1x2 MMI splitter. One pulse (reference pulse) goes through the straight waveguide while the other propagates though the delay line. Two pulses are then combined again at the output at a different timing. By looking at the peak powers and their time positions, the loss and the time delay of the delay line can be simultaneously measured. The delay line loss is measured to be 7 dB before the bonding and III-V processing. However, even though the delay line is well protected by a SiO$_2$ layer, the loss is increased up to 15 dB after the fabrication of the amplifiers as shown in Fig.
6.16(b). The measurements assumed that the two amplifiers are identical. The actual loop loss can be greater than the measured loss of 15 dB if the reference pulse saturates the amplifier. The reason for this loss increase has not been clearly specified yet, and it needs to be investigated further.

Figure 6.16. (a) Structure layout of the single delay unit. (b) Measured delay and loss of the delay line.

The gain of the amplifier is characterized by measuring photocurrents from an adjacent reverse-biased amplifier. The input and output amplifiers are 1200 µm long while the switch amplifiers are 800 µm long. Figure 6.17(a) shows the measured amplifier gain as a function of a current. The maximum gain of the input/output and switch amplifier is 8 dB and 6 dB respectively. The ideal 3 dB loss of the MMI splitter
is used to estimate the chip gain of the amplifiers. The available gain from these amplifiers are enough to compensate the delay line loss (15 dB), and at a high bias level, the device shows lasing operation when the gate matrix is configured for through-mode as shown in Fig. 6.17(b).

![Figure 6.17. (a) Measured chip gain of the amplifiers. (b) Lasing at a higher bias.](image)

The crosstalk and DC extinction ratio of the gate matrix switch is measured to be -34 dB and 30 dB respectively. The dynamic switching characteristics are shown in Fig. 6.18. The switch amplifier is driven with an input voltage being controlled by an arbitrary pattern generator. CW laser light at 1560 nm is launched to the device and the output from the switch is analyzed by a digital component analyzer (DCA). The control voltage level swings from 0 V to 1.6 V, which corresponds to a current swing of 0 mA to 180 mA. As shown in Fig. 6.18(a), the rising edge of the switch output has multiple steps caused by electrical reflections between the cable and the device due to the impedance mismatch. Figure 6.18(b) shows the rise time and fall time as a function of an optical input power. The rise time varies from 3.8 ns to 3.4 ns while the fall time varies from 1.3 ns to 1.2 ns with an input power variation of -9 to -1 dBm. In general,
the switching time is dependent on the electrical circuit response and the carrier lifetime of the amplifier. The electrical circuit response is primarily determined by the device impedance. The carrier lifetime varies with the carrier density in the active region and becomes shorter at a higher carrier density. Even though the rise time of the current device limited by the electrical circuit response, generally the fall time is shorter than the rise time because of the aforementioned carrier lifetime dependence on the carrier density. During switching-off, the switch turns off faster at the beginning due to the higher current density and becomes slower as the carrier density decreases. However the fall time is mostly determined by the first fast switching period because the most of the light is absorbed already at lower carrier density resulting in negligible contributions to the fall time [1].

![Figure 6.18.](a) Waveform at the output of the switch. (b) Rise time and fall time as a function of the input power of the switch.

6.5 Packet Switching Experiment

The integrated device performance is evaluated with a RZ PRBS 40 Gb/s data stream. Figure 6.19 shows the test setup used for the measurements. A data packet at a
Figure 6.19. Schematic diagram of the testing setup.

Figure 6.20 shows data packets ($2^5 - 1$) with two different switch configurations (through and cross-over). The figure shows a packet delay of 1.1 ns after one recirculation through the 9 cm long delay line (Fig. 6.20(b)). The additional insertion loss after one recirculation is 2.6 dB because the signal wavelength (1560 nm), which is chosen for EDFA amplifications, is deviated from the gain peak of the on-chip amplifiers (1572 nm). The plots on the right side of Fig.6.20 show the close view of the
received packets. The packet after one recirculation has slightly more power fluctuations due to the ASE noise from three additional on-chip amplifications.

![Image](image.png)

**Figure 6.20.** (a) Data packets without recirculation (b) Delayed data packet after one recirculation.

To quantify the effect of the multiple amplifications, BER measurements with $2^{31}-1$ PRBS data streams are carried out. Figure 6.21(a) shows the measured BER as a function of a power at the receiver with different input power levels to the device. In general, BER of the delayed signal is higher than non-delayed signal as shown in the figure. Figure 6.21(b) shows the power penalty at a BER of $10^{-9}$ as a function of the input power. The power penalty without the delay is less than 1 dB with an input power variation of -16 to -4 dBm. However, the power penalty with one recirculation increases up to 4.3 dB because of additional ASE noise and shows a bathtub curve minimized at an input power around -10 dBm. At a low input power, the power penalty is dominated by the ASE noise while at a high input power the power penalty increases.
again because of the saturation of the amplifiers. The input dynamic range for less than a 3 dB power penalty is 8.5 dB for one recirculation.

The current device can’t be characterized under dynamic switching of the gate amplifiers because the minimum delay of the device is shorter than the switching time, which is primarily limited by the driving electronics. Typically a few nano-second long guard bands are employed to prevent data payloads from being distorted by a finite switching time. However, the rise time of the current switch of ~3.4 ns is longer than the packet delay of 1.1 ns. Additionally, only 44 bits can fit in the current delay line length (9 cm), which is too short to incorporate both the guard band and payload. Therefore, implementation with a longer delay line is needed for buffering the data packets for multiple recirculations.
Figure 6.21. (a) Measured BER as a function of the received power with different input powers to the device. (b) Power penalty at a BER of $10^{-9}$.

6.6 DEVICE PERFORMANCE ANALYSIS

In order to understand the current device performance, a simple device model, shown in Fig. 6.22, is analyzed. The model is based on a cascaded amplifier link consisting of lossy passive components and amplifiers. The definition of each term is
given in Table. 6.3. In this model, only the effect of the ASE noise is considered to simplify the problem.

Table 6.3. Definitions of the parameters used in the device model.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_i$</td>
<td>Gain of the input amplifier</td>
</tr>
<tr>
<td>$G_{sw}$</td>
<td>Gain of the switch amplifier</td>
</tr>
<tr>
<td>$G_d$</td>
<td>Gain of the amplifier in the loop</td>
</tr>
<tr>
<td>$L_{mmi}$</td>
<td>MMI transmission (-3dB)</td>
</tr>
<tr>
<td>$L_d$</td>
<td>Loop loss</td>
</tr>
<tr>
<td>$F$</td>
<td>Noise figure of the amplifier (assumed to be 7 dB)</td>
</tr>
</tbody>
</table>

The signal transmission in the device can be divided into three stages: 1) input stage, 2) recirculating stage, and 3) output stage. The effect of transmission through each stage is represented by an effective noise factor and a net gain, which can be calculated using a simple model of a cascaded chain of passive elements and amplifiers [25]. The detailed mathematical derivation is omitted here, and the resulted net noise figure of each stage is shown in Fig. 6.22. From the noise factor and the net gain of each stage, the effective noise factor of the entire device can be derived as a function of a number of recirculation ($N$), which is written as Eq.6.4.

$$F_{\text{net}}^{\text{net}} = F_{\text{IN}} + \frac{F_{\text{OUT}}}{G_{\text{IN}}}, \text{ for } 0 \text{ recirculation.} \quad \text{Eq.6.4a}$$
\[ F_{N=1}^{\text{net}} = F_{IN} + \frac{F_{\text{LOOP}}}{G_{IN}} \sum_{k=1}^{N} \frac{1}{G_{\text{LOOP}}^{k-1}} + \frac{F_{OUT}}{G_{IN} G_{\text{LOOP}}^N}, \] for \( N \) recirculations. Eq.6.4b

Since the device needs to be biased below the lasing threshold, there is another constraint that the net gain of the recirculating stage \((G_{\text{LOOP}})\) should be less than unity. Applying this condition to Eq.6.4b, the minimum noise factor after \( N \) recirculations occurs when \( G_{\text{LOOP}} \) is unity and is written as Eq. 6.5.

\[ F_{N=1}^{\text{net}} = F_{IN} + \frac{F_{\text{LOOP}}}{G_{IN}} N + \frac{F_{OUT}}{G_{IN}}, \] for \( G_{\text{LOOP}} = 1 \). Eq.6.5

Equation 6.5 suggests several ways to minimize the signal degradation from the ASE noise accumulation. First, the noise factor increases linearly as the number of the recirculations increases with a rate of \( F_{\text{LOOP}}/G_{IN} \) which is de-emphasized noise factor by the input amplifier gain at the recirculating stage. Therefore the input amplifier gain \((G_{IN})\) needs to be high enough to suppress the effect of the noise accumulation from the multiple recirculations. Next, the noise factor of the recirculating stage \((F_{\text{LOOP}})\) needs to be minimized for the same reason. As shown in the equation in Fig.6.22, \( F_{\text{LOOP}} \) is primarily determined by a product of the loop loss and the gain of the loop amplifier \((G_dL_d)\), which implies that signal power entering the loop needs to be preamplified with a higher gain.

The power penalty can be estimated by calculating receiver sensitivity for each recirculation. To simplify the calculation, it is assumed that ASE noise has dominant effects on the receiver sensitivity over other factors such as modulation format and timing jitter. Equation 6.6 is used for this calculation and the power penalty is defined.
as receiver sensitivity degradation at a BER of $10^{-9}$. A -27 dBm receiver sensitivity, which is estimated from the back-to-back BER measurements, is used as a reference. This equation also approximates that the shot and thermal noise is negligible compared to the beating noise of the ASE against itself and the signal [26].

$$P_{rec} = h v F_N^{net} \Delta f \left( Q^2 + Q \left( \frac{\Delta v_{opt}}{\Delta f} \right)^{1/2} \right)$$  \hspace{1cm} \text{Eq.6.6}

, where $h$, $v$, $\Delta f$, $\Delta v$, and $Q$ are Plank’s constant, optical frequency, electrical bandwidth of the receiver, optical bandwidth of the bandpass filter, and quality factor, respectively.

Figure 6.23 shows the calculated power penalty as a function of a number of recirculation with a different loss of the delay line and gain of the input amplifier. A quality factor ($Q$) of 6 is used which corresponds to a BER of $10^{-9}$. The optical and electrical bandwidth are assumed to be 2 nm (246 GHz) and 40 GHz respectively.

As shown in the figure, the input amplifier gain and loop loss are crucial factors affecting the quality of the signal after many recirculations. With a lower loop loss and higher input amplifier gain, the effect of the noise accumulation can be suppressed further. It is predicted that 9~10 recirculations with a power penalty of 2 dB can be achieved if a loop loss and an input amplifier gain can be 15 dB and 10 dB, respectively. However it is inevitable to have a more loss from a longer delay line. A delay of 10 ns corresponds to a ~80 cm long silicon waveguide resulting in a typical loss of 20 ~30 dB even with a sub-dB/cm waveguide loss. Therefore, adding one or two more amplifiers inside the delay line will lead to better performance in this case. However, signal degradation from the pattern effects needs to be considered and weighted with the
benefits from additional amplifications. In addition, device layout has to be laid out carefully in order to suppress the thermal run-away effect due to the integration of many optical amplifiers.

![Figure 6.23](image)

**Figure 6.23.** Calculated power penalty as a function of a number of recirculation with a different loss of the delay line and gain of the input amplifier.

### 6.7 SUMMARY

This chapter presented the first demonstration of integrated optical buffers. The device structure incorporates the silicon delay line with the gate matrix switch. The silicon delay lines are designed to minimize the bend loss, yet they are still compact enough to enable the entire device to be laid out within \( \sim 1 \times 2 \text{ cm}^2 \) space. The waveguide loss with various fabrication techniques such as the side wall smoothing and the post exposure bake is investigated. A minimum waveguide loss achieved in this work is \( \sim 0.3 \text{ dB/cm} \) and it is likely to be limited by the additional roughness of the interface of silicon and BOX layers, not by the side wall roughness. Other passive
components such as MMI splitters and waveguide crossings are designed and fabricated.

The gate matrix switch is chosen over other types of optical switches because of a low cross talk of -30 to -40 dB. The rise time of the fabricated switch is ~ 3.4 ns primarily limited by the electrical reflections between the amplifier and the RF cable. Careful device packaging can improve the switching speed by eliminating a long cable between the device and the electronic circuit.

The fabricated device demonstrates one recirculation with a 1.1 ns packet delay. The minimum power penalty with one recirculation is 2.5 dB with an input dynamic range of 9 dB. Even though two amplifiers in the delay line can compensate the delay line loss, delayed packets after multiple recirculations couldn’t be evaluated because of the longer switching time than the packet delay.

This demonstration highlights the ability of the silicon evanescent device platform for combining low loss silicon passive components with silicon evanescent active devices. Further improvements on the waveguide loss and the amplifier gain should improve the device performance, leading to longer buffering time, and will provide enough functionality as integrated optical buffers for all optical packet switched networks. In addition, this structure can be directly extended to integrated optical synchronizers with several gate amplifiers.
6.8 Reference


Chapter 7 Conclusions

The objective of this thesis was to develop a hybrid integration platform to build photonic active devices with silicon-based optoelectronic circuits. Major accomplishments of the presented work include: 1) development of hybrid waveguide architecture consisting of a silicon waveguide and III-V quantum well layers, 2) demonstration of optically pumped silicon evanescent lasers as a proof of hybrid waveguide concept, 3) demonstrations of electrically driven photonic active devices: silicon evanescent FP lasers, silicon evanescent amplifiers, and silicon evanescent waveguide photodetectors, and 4) demonstrations of integrated devices for future optical networks and data communications: preamplified photoreceivers and optical buffers.

7.1 Thesis Summary

The devices presented in this work are based on the hybrid waveguide structure consisting of III-V gain layers and a silicon passive waveguide. Through the mode overlap to the III-V gain region, the optical mode in the hybrid waveguide experiences optical gain or absorption leading to building efficient electrically driven photonic active devices on the silicon photonics platform. The amount of mode overlap in III-V gain
layers and silicon waveguide layer can be engineered by manipulating silicon waveguide dimensions as well as the thickness and refractive index of each III-V layer.

A low temperature oxygen plasma assisted wafer bonding process was incorporated for device fabrication. A low temperature anneal step was important to minimize the material degradation from the large thermal mismatch between silicon and InP as well as to achieve a good scalability for wafer level bonding process. The basic mechanism of strong oxide bond formation during the annealing step was studied and it was found out that hydrogen gas, which is a byproduct from the annealing process, has to be driven out of the bonded interface efficiently to avoid the formations of gas bubbles. Bonding channels and ozone cleaning steps have been employed to facilitate the hydrogen diffusion process.

The optically pumped silicon evanescent lasers were demonstrated first to prove the hybrid waveguide concept. The lasing optical modes followed the expected trend as the silicon waveguide dimensions were changed. The electrically driven discrete devices were then demonstrated by changing the III-V layer structure to enable electrical current injection through the III-V layers. In addition, the III-V back-end processing was developed to create a diode structure on III-V layers. The demonstrated device performance is summarized in Table 7.1.

<table>
<thead>
<tr>
<th></th>
<th>FP laser</th>
<th>Amplifier</th>
<th>Photodetector</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold:</td>
<td>65 mA</td>
<td>Chip gain: 13 dB</td>
<td>R (fiber coupled): 0.315 AW</td>
</tr>
<tr>
<td>P_{max}, n_{id}</td>
<td></td>
<td>P_{sat}: 11 dBm</td>
<td>Internal QE: 90 %</td>
</tr>
<tr>
<td>(single sided, fiber</td>
<td>1.8 mW, 1.6 %</td>
<td>0.5 dB power penalty for 40</td>
<td>Dark current: 50 nA ~ 200 nA</td>
</tr>
<tr>
<td>coupled)</td>
<td></td>
<td>Gb/s data amplification</td>
<td>BW: 0.5 GHz</td>
</tr>
<tr>
<td>Max. operating T:</td>
<td>40 °C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Two different integrated devices were demonstrated: preamplified photoreceivers and optical buffers. The preamplifier photoreceiver consists of a silicon evanescent amplifier, a waveguide photodetector and silicon passive input/output waveguides. The interface design between the silicon passive waveguide and the hybrid amplifier waveguide is important because any small reflections at the interface can cause a spectral gain ripple. Mode coupling at the interface with different junction designs was explored and, as a result, III-V taper structure at the amplifier interface was chosen over abrupt and angled termination of III-V layers for high coupling efficiency with a reflection lower than $10^{-4}$. The photodetectors were re-designed based on learning from the first demonstrated device. The device dimensions were optimized aiming at high speed operation. The demonstrated device had a total responsivity of 5.7 A/W with a bandwidth of 3 GHz. The bandwidth of the device was limited by the carrier transport not by the RC response. Further investigations on various epitaxial structures including different quantum well designs will improve the device bandwidth.

Integrated optical buffer were investigated using the silicon evanescent device platform. For recirculating buffers, low loss delay line is very crucial to re-circulate data packets for many times without significant signal degradation. The silicon evanescent device platform has advantages over the InP based device platform in a sense that a typical silicon waveguide loss is in a range of 0.1 ~1 dB/cm which is an order of magnitude less than that of the III-V based waveguides. The demonstrated buffer in this work had a 9 cm long silicon delay line corresponding to a time delay of 1.1 ns. The minimum power penalty from one recirculation was 2.5 dB. The device model
accounting for the effect of ASE noise was proposed. The simulation showed that pre-amplification before the packets go into the delay line is important in order to reduce the signal degradation from the ASE noise accumulation. Even though this demonstration shows the feasibility of the concept of the integrated optical buffers, further work on improving the amplifier gain and the waveguide loss needs to be followed to achieve performances required by actual optical packet routers.

The silicon evanescent device platform provides unique advantages over other hybrid integration techniques in terms of integration capability with silicon passive devices (high coupling efficiency, and low reflection) and manufacturability to fabricate many devices with a single bonding step. Future work, including studies on device performance and reliability, will expedite the developments of silicon-based optoelectronic circuits integrated with on-chip silicon evanescent photonic active devices overcoming the indirect bandgap characteristic of silicon.

### 7.2 Future Work

**7.2.1 Performance improvements of discrete devices**

The performance of the individual device first needs to be improved in many ways to meet the requirements of various applications in the communication systems. First, the thermal performance should be improved to achieve a higher operating temperature and a higher amplifier gain. The BOX layer thickness is the major factor to affect the thermal impedance of the device. For the waveguide dimensions used in this work (0.7 µm height and 2 µm width), the simulation suggested that a BOX layer
thickness between 0.5 µm and 1.0 µm provides enough optical guiding without a significant optical mode leakage through the substrate. In addition, the thermal shunt structure with etching the BOX layer (See Fig. 3.11(a)) will be useful to reduce the thermal impedance of the device. Second, higher confinement in the gain region will provide a higher gain or absorption with a given device length. The typical quantum well confinement factor of this work is 4% from the offset quantum well structure. However, the higher quantum well confinement factor around ~ 10% will lead to a lower laser threshold, higher amplifier gain, and higher photodetector quantum efficiency. A silicon waveguide width of 0.5 µm with the same III-V layer structure used in this work yields the quantum well confinement factor of 8% to 10%. Even though the silicon confinement is reduced in a narrower waveguide, the efficient mode coupling between the hybrid and the silicon passive waveguide can be still achieved by incorporating the III-V taper structure presented in Chapter 5. In addition, a multistage amplifier or photodetector with varying confinement factors along the device needs to be investigated to achieve both the high gain/absorption and high saturation characteristics as will be described in the next section.

7.2.2 Multi stage amplifiers and detectors

The offset quantum well structure that was used in this work provides lower quantum well confinement leading to better saturation characteristic than the centered quantum well structure. However, the optical gain or absorption from a device with a lower quantum well confinement is lower. The demonstrated optical gain in this work didn’t exceed 15 dB, which is relatively lower compare to a typical gain from the III-V
amplifiers. This is partially related to the thermal characteristics of the demonstrated device, but also related to the quantum well confinement factor. In order to achieve both of a high gain (or a high quantum efficiency for a photodetector) and a high saturation power, multi stage device structure can be utilized (See Fig. 7.1) [1]. The basic concept of this structure is that, by changing the waveguide dimensions in the device, the mode overlap with the active region is managed to be lower when the photon density is higher while it is kept higher when the photon density is lower.

This can be achieved by changing the silicon waveguide width while keeping the same III-V layer structure in the silicon evanescent platform. Narrower silicon waveguide is employed for a high gain or absorption stage. Meanwhile, silicon waveguide width is tapered out for high saturation power stage as shown in Fig. 7.1.

![Multistage amplifier and photodetector](image)

**Figure 7.1.** Multistage amplifier and photodetector.

### 7.2.3 Multi channel preamplified receivers

Integrated multichannel receivers consisting of multiple photodetectors and wavelength de-multiplexers are useful for wavelength division multiplexing (WDM)
systems. Monolithically integrated 40 channel preamplified receivers have been demonstrated on InP based integration platform [2].

Silicon-based wavelength multiplexer can have better wavelength accuracy in each channel facilitated by the accuracy of silicon fabrication technique. In addition to wavelength accuracy, multichannel silicon-based receivers integrated with silicon evanescent amplifiers and photodetectors can benefit from preamplification for improved receiver sensitivity (See Fig.7.2). Furthermore, as CMOS receivers with Ge photodetectors have been demonstrated already [3], receiver electronics can be integrated in the vicinity of photodetectors with silicon evanescent devices following a general process flow describe below.

**Figure 7.2.** Multichannel receiver with a silicon demultiplexer.

Silicon wavelength multiplexers including CMOS electronics is fabricated first, Then III-V layers can be bonded only on the photodetector and amplifier region followed by the III-V back end processing. This will be very similar to the one described
in Chapter 6. The maximum temperature of the III-V back side process is around 400 °C, which is unlikely to destroy CMOS electronics.

### 7.2.4 Optical buffers and synchronizers

In this work, a 114 cm long delay line (14 ns) were fabricated and exhibited a propagation loss of 35 dB (See Fig. 7.3) as mentioned in Chapter 6. Optical buffer with this long delay line were also fabricated. However, the loop loss increased almost infinitely after wafer bonding and III-V processing, which made it impossible to measure the delayed output packets. Even though this problem also exists in the device presented in Chapter 6, the delayed packet was measurable since the loop length is a lot shorter. Therefore the reason of the waveguide loss increase should be explored to implement optical buffers with a longer delay.

![Figure 7.3. Measured pulse delay and loss from a 114 cm long recirculating loop.](image)

Another potential application of this device structure is optical synchronizers. An optical synchronizer is a variable optical delay unit used to line up optical packets arriving asynchronously at an optical router in the time domain. Since there has been no
continuously tunable delay demonstrated in the optical domain thus far, multiple small delay units such as fiber delay lines have been used for optical synchronization [4]. Short silicon delay lines can replace fiber based delay lines leading to compact integration. Figure 7.4 shows a synchronizer implemented by silicon delay lines with different lengths and silicon evanescent amplifier gates. The path of the optical packet is controlled by the amplifier gates which eventually determine the delay of the gated output signal. With two different lengths of delay lines, 4 different combinations of delay can be possible: e.g., 0, 1, 2, and 3 ns delay is possible with 1 ns and 2 ns delay lines.

**Figure 7.4.** Integrated optical synchronizer.
7.3 REFERENCES


Appendix A. Self-aligned Process Follower

Preamp process follower v 1.3 (revised 3/11/08), Hyundai Park (x4235)
Mask set: preamp2.1-2.3, Preamp_rev2.2_1, Preamp_rev2.3_mask1

Batch #: Start date: End date:

1. P mesa (self aligned)
a. Litho (stepper, schedule: ) : optional (PTLM)
   - Thin p metal deposition (Ebeam#3, schedule: )
     - Oxide removal: BHF:DI(1:10) for 30sec
     - Pd/Ti/Pd/Au (30/170/170/1000)
b. SiN deposition (PECVD, schedule: )
   - Two layers of 1500A SiN, Rinse the sample between depositions
   - Litho (stepper, schedule: )
     - SPR955-0.9 (spin at 3krpm for 30sec, bake at 95C for 1min)
     - Exposure: 1.1 sec, offset 0
     - Bake: 110 C, 60 sec
     - Develop: MF701 for 40sec
d. SiN etching (RIE #3, schedule: )
   - O2 chamber clean (O2, 20sccm, 50 mT, 500 V, 30 min)
   - CF4 etch: CF4/O2 (20sccm/1.8sccm), 10mT, 250V, ~11 min (250-500 A/min), laser monitor
   - PR burn: O2, 20sccm, 10mT, 250V, 5 min
   - PR strip in 1165 at 80C
e. Au wet etching
   - Au etchant: DI (1:3), ~1’ 45”, check samples after a minute
   - Descum
f. Metal dry etching (RIE #5, schedule: )
   - O2 chamber clean: 50sccm, 55mT, 300W, 10min
   - Metal etch: Cl2/Ar(44sccm/20sccm), 10mT, 100W, ~4min, laser monitor
   - Pump/Purge/Pump for 2min each cycle
g. Mesa etching (RIE #2, schedule: )
   - O2 chamber clean: 20sccm, 125mT, 500V, 30min
   - MHA precoat: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, 20min
   - MHA etch: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, ~20min, laser monitor
- O2 Descum: O2, 20sccm, 300V, 125 mT, 10min
2. QW etching
   a. Litho (stepper, schedule: )
   - SPR955-1.8 (spin at 3krpm for 30sec, bake at 95C for 90sec , ~1.8um)
   - Exposure: 1.7 sec, offset 0
   - Bake: 110 C, 90 sec
   - Develop: MF701 for 60sec
b. Wet etch
   - H3PO4:H2O2:DI (1:5:15) for ~2’ 10” after color change
   - No N2 dry, bring the sample in DI
   - Strip PR in 1165 at 80C
   - Hard bake at 110 for 10min
c. SiN hard mask etch using PEII for 4min
d. SiN support layer deposition (PECVD, schedule: )
   - two layers of 1000A (2000A total, Rinse the sample between depositions)
   - use a glass plate
3. N metal deposition
   a. Litho (stepper, schedule: )
   - SF11 (two layers, spin at 4krpm for 30sec, bake at 200C for 2 min, cooling for 1 min)
   - AZ5214 (spin at 6krpm for 30sec, bake at 95C for 1min)
   - Exposure: 0.55 sec, offset 0
   - Hard bake at 110C for 60sec
   - Flood exposure 1min
   - Develop: MF701 for 60sec
   - UV Exposure: 300sec
   - Develop: SAL101 for 70sec
   - UV Exposure: 300sec
   - Develop: SAL101 for 70sec
   - UV Exposure: 300sec
   - Develop: SAL101 for 60sec
b. SiN etch using PE-II, 3 min
c. Metal deposition (Ebeam #3, schedule: )
   - Oxide removal: BHF:DI(1:10) for 30sec
   - Ni/Ge/Au/Ni/Au (50/300/300/200/10000)
   - Liftoff in 1165 at 80C
4. Anneal: strip annealer at 320C for 30sec (for 2um thick BOX)
5. Thick amp p metal deposition
   a. Litho (stepper, schedule: )
   - SF11 (two layers, spin at 4krpm for 30sec, bake at 200C for 2 min, cooling for 1 min)
   - AZ5214 (spin at 6krpm for 30sec, bake at 95C for 1min)
   - Exposure: 0.4 sec, offset 0
   - Hard bake at 110C for 60sec
   - Flood exposure 1min
- Develop: MF701 for 90sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
- UV Exposure: 300sec
- Develop: SAL101 for 60sec

b. SiN etch using PE-II, 3 min

c. Metal deposition (Ebeam#3, schedule: 

- Oxide removal: BHF:DI (1:10) for 30sec
- Pd/Ti/Pd/Au (30/170/170/15000)
- Lift off in 1165 stripper at 80C

6. Implantation

a. Litho (stepper, schedule: 

- SF11 (3 layers, spin at 4krpm for 30sec, bake at 200C for 1min, 1min, 2 min)
- AZ5214 (spin at 6krpm for 30sec, bake at 95C for 1min)
- Exposure: 0.55 sec, offset 0
- Hard bake at 110C for 60sec
- Flood exposure 1min
- Develop: MF701 for 90sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
b. Send out for implantation

c. Strip the resist layer in 1165

7. N layer etch

a. SiN deposition (PECVD, schedule: 

- Single layer of 500A SiN
b. Litho (stepper, schedule: 

- SPR955A-1.8 (spin at 3krpm for 30sec, bake at 100C for 90 sec,~ 1.8um)
- Exposure: 1.7 sec, offset 0
- Bake: 110C, 90sec
- Develop: MF701 for 60sec
- O2 chamber clean: 20sccm, 125mT, 500V, 30min
- MHA precoat: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, 20min
- MHA etch: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, 10min
- O2 Descum: O2, 20sccm, 300V, 125 mT, 10min
- Strip the resist layer in 1165 at 80C

c. Mesa etching (RIE #2, schedule: 

176
- O2 chamber clean: 20sccm, 125mT, 500V, 30min
- MHA precoat: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, 20min
- MHA etch: CH4:H:Ar (4sccm:20sccm:10sccm), 75mT, 500V, 10min
- O2 Descum: O2, 20sccm, 300V, 125 mT, 10min
8. VIA open
a. SiN adhesion layer deposition (PECVD, schedule: )
   - single layer of 500A
b. SU8 Litho (stepper, schedule: )
   - Sample clean with ACE/ISO/DI
   - Dehydration bake at 110C for 1min
   - SU8 coat
      Spread: 500rpm for 10sec (100rpm/sec ramp)
      Coating: 3000rpm for 30sec (300rpm/sec ramp)
   - Soft bake at 95C for 2min
   - Exposure: 2 sec, offset -12
   - Bake at 95 C for 1min
   - Develop: SU8 developer, dip and shake for 60sec+pipet flush for 15sec
   - ISO rinse and N2 dry
   - Desum 1 min
c. SU8 curing (hot plate)
   - start at 95C
   - ramp up to 150C stay for 5min
   - ramp up to 205C stay for 5min
   - ramp up to 260C stay for 30min
   - ramp down to 205 C stay for 5min
   - ramp down to 150C stay for 5min
   - ramp down to 95C and take out the sample
   -Descum/CF4/Descum: 30 sec/30 sec/15 sec
*color will become dark red when hard baked in air
d. SiN adhesion layer deposition (PECVD, schedule: )
   - single layer of 1000A
e. Litho (stepper, schedule: )
   - nLoF2020 (spin at 4krpm for 30sec, bake at 110C for 1min)
   - Exposure: 0.55 sec, offset -6
   - Hard bake at 110C for 60sec
   - Develop: MF701 for 90sec
f. SiN etch using PE-II, 5sec (total 4000A of a SiN layer)
9. P probe pad
a. Litho (stepper, schedule: )
   - SF11 (3 layers, spin at 4krpm for 30sec, bake at 200C for 1min, 1min, 2 min)
   - AZ5214 (spin at 3krpm for 30sec, bake at 95C for 1min)
   - Exposure: 0.3 sec, offset 0
   - Hard bake at 110C for 60sec
- Flood exposure 1min
- Develop: MF701 for 90sec
- UV Exposure: 300sec
- Develop: SAL101 for 70sec
- UV Exposure: 300sec
- Develop: SAL101 for 60sec

b. Metal deposition (Ebeam #1, schedule: )
- Native oxide removal: BHF:DI (1:10) for 30sec
- Ti/Au (50/30000), use a rotating chuck with tilting by ~10deg, lower the sample position (7 inch above from the bottom)
- Lift off in 1165 at 80C