SOA gate array recirculating buffer with fiber delay loop


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Abstract: We present a compact variable delay buffer for storage of 40 byte packets. The recirculating buffer is based on an InP SOA gate array two-by-two switch which provides greater than 40 dB of extinction, sub-nanosecond switching, and fiber-to-fiber gain. The switch is used with a fiber delay loop 450 centimeters, or 23 ns, in length. The buffer is demonstrated with greater than 98% packet recovery at 40 Gb/s for up to 184 ns of storage.

References and links

1. Introduction
There is interest in optical routers to solve the capacity and power limits of electrical routers. Yet optical routers remain elusive, partly due to the lack of a practical optical buffer. Optical packet switching is a natural choice for optical routing, multiplexing not only wavelengths, but also packets of data in the time domain. However, this creates the possibility of contention between two packets, thus necessitating optical packet buffering.
A scalable, high bit-rate, and compact optical packet buffer has yet to be demonstrated [1]. The majority of optical buffering approaches can be generalized as either feedback or feed-forward buffers, many of which implement two-by-two or one-by-two switches [2, 3]. Although reasonable storage times have been demonstrated, there have not been any practical compact solutions. In this work, we present a simple recirculating buffer that operates without additional components in the delay loop and can be easily integrated with a silicon or silica-on-silicon delay chip. To the authors’ knowledge, this device has the best performance for a buffer approach amenable to integration.

2. Buffer requirements

Optical buffers must meet certain requirements for practical use in a router. It is necessary that a buffering approach can impart a delay of at least the length of the packet payload in order to provide contention resolution. It is also important for the buffering device to be bit rate scalable to 40 Gb/s or greater to offer an advantage over electrical domain counterparts. For acceptable network loads, they should have the capability to store packets of no less than 40 bytes with guard bands no more than several nanoseconds long. Packet payload length is one of the more difficult challenges for many buffering approaches, but unless the ratio of the payload length to the overhead of the header and guard bands is reasonable, optical buffers and packet switches will not afford an advantage. In addition, it is desirable to require less header processing for a given amount of payload. In order to accommodate short guard bands, buffers must be able to switch or reset in less than several nanoseconds.

Along with the above requirements, there are additional considerations needed in order to make optical routers competitive. Optical packet switches must lower the cost per bit for data transmission to make them advantageous. It is also necessary that optical buffers have low power consumption, low heat production, and a small footprint, which are the main challenges facing the scalability of electrical packet switches. For both cost and footprint, it is obviously important that the number and complexity of components included in a given buffer approach be kept to a minimum.

Although it is implausible that optical buffers will match electrical memory in cost and footprint in the near future, studies have shown that the buffering capacities need to be much less than believed, thus easing these requirements. Electrical routers at the edge of the network need large banks of memory, but optical routers intended for the core have different needs. Simulations show that if access links are slower than the backbone network and the traffic is smoothed, then only ten packet buffers per output port are needed for 80% throughput [4]. The number of necessary optical buffers per port affects the signal quality as well as being critical in reducing cost, footprint, and energy consumption. Although it will be small, transmission though each buffer will add power penalty and decrease the signal-to-noise ratio by up to 1 dB.

Lastly, in order to make the optical buffer more flexible, it is desirable for the buffer to be transparent to packet length and to provide dynamically variable storage time. And alike all other optoelectronic components, the buffering device should impart the least possible dispersion and optical power penalty.

3. Buffer design

A recirculating buffer approach is chosen to provide dynamically variable storage times with the granularity of the delay line length. Recirculating buffers have been pursued with success in the past using fiber loops [5, 6] and therefore show promise for a practical buffer if they can be designed to be amenable to integration without sacrificing performance. The buffer approach combines a two-by-two InP-based switch with 450 centimeters of fiber (Fig. 1). It is also possible to replace the fiber delay with waveguide delay chips for a more compact solution. The delay line length is chosen to be slightly longer than the length of a packet and its guard bands, thus allowing the greatest resolution in possible delay times.
The two-by-two switch must meet significant performance requirements to make the recirculating buffer successful. The switch itself must be bit-rate scalable up to 40 Gb/s, have low crosstalk (< -40 dB) and high extinction ratios (>40 dB) for cascadability [7], and be able to switch within packet guard bands. The semiconductor optical amplifier (SOA) gate matrix switch is the most promising switch choice for recirculating buffers because it has the highest extinction ratios while also providing fast switching and inducing little loss. During operation, the signal is split toward the two possible output ports and the switching amplifier is turned on for the desired path while the other path’s amplifier is left off to absorb the remainder. A fabricated switch was previously characterized with good performance up to 40 Gb/s and switching times less than 2 ns [8]. The second generation was redesigned for integration and better performance and enable error-free buffering (Fig. 2).

The InGaAsP/InP SOA gate matrix switch presented here has an improved integrated amplifier layout and waveguide routing. The switch uses an offset quantum well platform in which the quantum wells are grown above a bulk waveguide layer. This results in an offset between the peak of the mode and the gain region and thereby lowers the confinement factor. The benefits of this platform include ease of fabrication, the possibility of future integration with other standard photonic integrated circuits, and linear performance at higher output powers due to the lower confinement factor [9]. In order to further mitigate saturation effects, the amplifier directly before the delay is flared as it will experience the most power.

Many-body gain simulations were performed to optimize the placement and lengths of the amplifiers in order to distribute the gain and minimize saturation [10]. The simulations were used to create theoretical eye diagrams as well as simple gain plots. Figure 3 shows the expected and experimental gain provided by the longest and shortest amplifiers. The simulations fit well for modest gain, but begin to deviate at higher current densities due to heating, which was not accounted for in the model. Using the simulations, the total gain of each port configuration was designed to exceed the loss by only several dB. Therefore, during the first several circulations there is slight gain until the amplified spontaneous emission (ASE) builds up and detracts slightly from signal gain. The amplifier lengths range from 200 μm long for the switching amplifiers in the shortest path to 650 μm long for the input amplifier and the amplifiers on both ends of the delay.

Lastly, an additional component of the design is the tightly confining, deeply etched bend to avoid crossing waveguides while allowing the input and output ports to be positioned on the side opposite to the delay ports. The deep 90° bends are shown in the inset of Fig. 2.
4. Measurements

4.1 Measurement setup

The experiments were performed on devices that were soldered and wirebonded to aluminum nitride submounts and then affixed with thermal compound to a copper mount. The submounts were cooled to approximately 18°C. Lensed fibers were used to couple light on and off the chip at each of the four ports. The optical signal (1550 nm) was modulated using an SHF 50 Gb/s BERT with RZ 2^{31}-1 pseudo-random bit sequence (PRBS) data at 40 Gb/s. Packet measurements were made using 40-byte packets which contained 64-bit identifier strings for characterization. A variable attenuator and a polarization controller were placed in the setup before the device to maintain a TE-polarized input since the quantum well amplifiers are polarization dependent. A 1.2-nm bandpass filter was placed before the receiver to reduce the amplified spontaneous emission (ASE).

4.2 InP switch

Static measurements and bit error rate testing were performed using continuous data at 40 Gb/s to characterize the performance of the switch. The chip gain from the input port fiber to the delay fiber was approximately 2 dB. Fast switching was implemented using a signal converting board designed to provide constant current when turning on amplifiers quickly. The switching rise and fall times were measured using a fast photodetector and oscilloscope and were 1 ns or less for the longest amplifier (Fig. 4). The switching time varied by less than 150 ps with optical input power.

Fig. 4. Oscilloscope screen image showing the switching speed of a 650 micron long SOA. The time scale is 2 ns/div.
The sensitivity degradation for the four port configurations at 40 Gb/s is shown in Fig. 5a. The back-to-back measurement is taken as a reference for the system by bypassing only the device under test with a fiber patch cord. The measurements show negative power penalty due to reshaping from the amplifiers and the bandpass filter used to reduce the accumulated ASE. The dynamic range of the input power is shown below in Fig. 5b and is greater than 15 dB.

![Fig. 5. a) BER vs. optical power at 40 Gb/s RZ. b) Operable range of input powers for the path from the input port to the delay port.](image)

### 4.3 Buffering

The InP-based switch demonstrated successful optical buffering of packets when combined with a fiber recirculation loop. The fiber delay was chosen to be 23 ns, which is therefore also the resolution of the storage time. Optical signal-to-noise ratios (OSNR) were measured by taking the difference in power of the signal and the noise at a wavelength 1 nm away. These calculations were done for a range of the input power to the device for all storage times from 1 to 10 circulations. The back-to-back OSNR was 53 dBm. Fig. 6 shows the experimental OSNR data overlaid with theoretical calculations based on static measurements. As expected, the OSNR drops by the same value as the input optical power. The difference in OSNR with increasing number of circulations is due to the build up of ASE as already mentioned. The additional ASE was simply calculated by measuring the ASE from an output amplifier and multiplying by a factor of 3 to account for the length of the multiple amplifiers in the recirculation loop. The degradation of SNR in recirculating loops has been shown to decrease steeply for small numbers of circulations, but to slow down with increasing circulations [2], providing optimism for future generations.

![Fig. 6. Optical signal-to-noise ratios as a function of number of circulations for a range of input powers. The solid lines are theoretical.](image)

Packet recovery measurements demonstrate that the data was preserved. Each generated packet contained identical 64-bit strings of pseudo-random data that were checked at the
receiver. Packets were considered recovered if all 64 bits matched the known identifier string. Packet recovery is used as a Layer 2 metric to replace bit error rates for applications such as buffering when data may be reordered. First, the dynamic range of the buffer was tested for 4 circulations and shown to be error-free over an 8 dB range of input power (Fig. 7a). This measurement also served to determine the optimum operating input power. The buffer was then tested for maximum storage time. Up to 184 ns of buffering was possible with packet recovery of greater than 98%, as shown in Fig. 7b.

![Fig. 7. a) Packet recovery measurements for varying input power for a delay of 4 circulations. b) Packet recovery percentage as a function of received power for back-to-back and 1, 8, and 10 circulations.](image)

The primary limitation of this optical buffering approach is the ASE that builds up in the recirculation loop. This is confirmed by the improvement provided by placing a bandpass filter into the recirculation loop. The use of a 5-nm filter increases the maximum storage time to 230 ns, as shown in Fig. 8. The optical buffer could thus be improved with reduced overall losses, thereby allowing shorter amplifier lengths and decreasing the ASE. Reducing loop loss would also decrease the power consumption, bringing it from the 0.6 W currently necessary to compensate for loop losses to as low as 0.1 W, or 2.5 pJ/bit for a circulation (5 dB loop loss).

![Fig. 8. Improvement shown in packet recovery by using a bandpass filter in the delay line.](image)

5. Conclusions

In this work, we demonstrate a buffer that is randomly accessible in time increments of 23 ns and can store packets for up to 184 ns with greater than 98% packet recovery. The core of the buffer is a fabricated InP SOA gate array switch that has excellent extinction (40 dB), fast switching (1 ns) and sufficient gain to balance the recirculating losses. The buffer presented offers a compact solution for optical memory that can be easily integrated with a chip delay to meet the estimated buffering needs of future core optical routers.

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