Silicon Evanescent Amplifiers

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Abstract: Optical amplifiers are important elements of photonic integrated circuits. We present a hybrid silicon evanescent amplifier utilizing a wafer bonded structure of silicon waveguide and AlGaInAs quantum wells. A chip gain of 13 dB with a power penalty of 0.5 dB at 40 Gb/s data amplification is demonstrated.

Silicon photonics is an important research field for photonic integrated circuits with low cost and high functionality. Optical amplifiers are key components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. Recently we demonstrated a silicon evanescent laser and amplifier [1] combining the high optical gain of III-V quantum wells and a low loss silicon waveguide using a low temperature wafer bonding technique.

The silicon evanescent amplifier is a hybrid structure that consists of an offset multiple quantum well region bonded to a silicon waveguide fabricated on a silicon-on-insulator (SOI) wafer. Details of the structure are shown in Fig. 1a. With this architecture, the optical mode can obtain electrically pumped gain from the III-V region while being guided by the underlying silicon waveguide region.

The silicon waveguide was fabricated with a final height of 0.76 μm and width of 2 μm. The III-V structure including eight AlGaInAs quantum wells grown on a InP substrate is transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding with a 300 °C annealing temperature. After removal of the InP substrate, a mesa structure on the III-V layer is formed (Fig.1a) using standard lithography, and wet and dry etching processes. After Ni/AuGe/Ni/Au and Pd/Ti/Pd/Au contacts are deposited for n-contact and p-contact respectively, proton (H+) implantation on the two sides of the mesa is performed to create a 4 μm wide current channel for carrier confinement. Ti/Au probe pads are then deposited on the top of the mesa. The sample is diced orienting the waveguides at an angle of 7 ° and an antireflection coating of Ta₂O₅ (~5%) is applied to each facet after facet polishing. The final device length is ~ 1.36 mm. A cross-sectional SEM image of the final device is shown in Fig. 1b. More information on epitaxial structure and device fabrication process can be found in Ref. 1. The calculated overlap of the optical mode for the fabricated device dimensions are 74 % in the silicon waveguide and 3.4 % in the AlGaInAs quantum wells.

The device gain is measured by launching and collecting the signal through lensed fibers at both the input and output facets at 15 °C. The coupling efficiency from the device to the fiber is measured to be -5 dB by measuring the insertion loss at long wavelengths. Figure 2 shows the measured small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using 5 dB coupling loss. The maximum fiber-to-fiber gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. The inset of the figure represents the net modal gain, Γg-α, where Γ is the QW confinement factor, g is the material gain, and α is the waveguide loss. The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current density at the active region. At lower current densities, the gain increases logarithmically while at higher current densities it saturates due to device heating caused by the series resistance (7.5 Ω) and thermal impedance (40 K/W). The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA.

The 3 dB output saturation power from the chip is measured to be 11 dBm as shown in Fig. 3. The evanescent coupling scheme of the device structure typically provides 2 % to 3 % of QW confinement factor, resulting in higher output saturation powers than amplifiers with centered quantum wells whose typical confinement factor is around 5 % to 15 %. Moreover, the tapered or flared waveguide structure demonstrated with III-V amplifiers [2] can also be applied to this device by manipulating the silicon waveguide width without changing the III-V region for better output saturation output power.
measured noise figure varies between 13 dB and 10 dB depending on the current level. The internal noise figure of the device can be between 8 dB and 5 dB, considering the 5 dB coupling loss.

In the case of preamplification, dynamic characteristics and power penalty are also important for high speed data detection [3]. Figure 3 shows the measured 10 Gbps NRZ eye diagrams with three different input power levels. The measured data agrees well with simulated eye diagrams, which are calculated using the rate equation model for multiple quantum wells with a carrier life time of 1.1 ns. The degradation of the Q-factor of the signal can be observed with input power above -4 dBm, which is higher than centered quantum well amplifiers due to the lower optical confinement in the device. To investigate the dynamic performance of the device, BER measurements are employed at 3 different data rates, 2.5Gbps NRZ, 10Gbps NRZ and 40Gbps RZ. A PRBS of $2^{31}-1$ was used to carry out the measurements for 10 Gbps and 40 Gbps, while a shorter sequence of $2^{10}-1$ is chosen for 2.5 Gbps. The average input power is -16 dBm to keep the device unsaturated. A variable optical attenuator (VOA) is inserted between the output of the amplifier and the receiver to adjust the received power. The power penalty of the amplifier is extracted by comparing the BER performances of the transmitter-amplifier-receiver link with the back-to-back transmitter. As shown in Fig. 5, a low power penalty of 0.5 dB for all three data rates is achieved and it is mainly induced from the ASE noise. To compare the distortion due to the pattern effect, another BER curve with a higher input power of 2 dBm is also plotted in Fig. 5. An additional power penalty of 0.5 dB is required when pattern effects start to reduce the Q-factor of the signal.

References

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