HIGHLY EFFICIENT VERTICAL OUTFUSSAGING CHANNELS FOR LOW-TEMPERATURE INP-TO-SILICON DIRECT WAFER BONDING ON THE SILICON-ON-INSULATOR SUBSTRATE

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The authors report a highly efficient design for low-temperature, void-free InP-to-silicon direct wafer bonding on a silicon-on-insulator (SOI) substrate. By etching an array of small through holes in the top silicon layer, the generated gas by-products (H2O, H2) from bonding polymerization reactions and thus gaseous hydrocarbon can be absorbed and diffuse in the buried oxide layer, resulting in up to five orders of magnitude interfacial void density reduction (from >50 000 to ≤3 cm−2). The required annealing time is reduced to less than 30 min, a ~100X improvement compared to the previous outgassing design as well. Comprehensive studies in associated processing details, bonding surface energy, universality, and stability are also presented. Successful 50, 75, and 100 mm InP epitaxial layer transfer to the SOI substrate is also demonstrated, which indicates a total elimination of outgassing issues regardless of the wafer bonding dimension. Several incidental advantages leading to a flexible device design, low fabrication cost, and potential bonding strain relief are also discussed. © 2008 American Vacuum Society. [DOI: 10.1116/1.2943667]

I. INTRODUCTION

Semiconductor wafer bonding has recently been represented as an attractive, viable, large-scale hybrid material integration approach with the development of semiconductor wafer manufacture technology. When two mirror-polished, flat, clean wafers are brought into contact with each other at room temperature, regardless of wafer material and size, van der Waals force or hydrogen bond holds the two wafers in position to allow the bonded pair to transfer to the following stage. For example, thermal annealing for fusion bonding, electric field accession for anodic bonding, or long time storage for room-temperature bonding, all entail enhancing the bonding surface energy. Since polymerization reactions are usually involved in the surface bond formation for fusion bonding and anodic bonding, against the adhesive bonding by using interfacial adhesive polymer materials, removing the gas by-products is vital for achieving strong covalent bonds. Equations (1)–(3) represent the fundamental polymerization reactions in Si-based hydrophilic and hydrophobic direct bonding. The generated gas by-products of H2 and H2O have been proven to be the major trapped gases at bonding interface experimentally. A significant amount of gas formation and desorption of 2–3 monolayers (ML) of water molecules at the bonding interface of hydrophilic wafers after room-temperature mating, thus gaseous hydrocarbon from organic surface contamination during annealing, can lead to high internal pressure, subsequently resulting in local debonding, i.e., interface void formation. Other than the influence to mechanic property, electrical property at the bonding interface can vary with bonding quality. Typically, gas molecules, especially at high temperatures with a small atom size, such as H2, can diffuse out through the microporosity at the interface gradually or enter through a porous medium (such as SiO2) quickly. Interfacial voids can also be filled up due to native or thermal oxide viscous flow at high temperatures (>800 °C). An elevated temperature annealing is therefore preferred naturally due to resulted void-free, strong bonding and its processing simplicity with no need of prebond surface activation. For example, manufacturing of commercial wafer-bonded silicon-on-insulator (SOI) wafers up to 300 mm in diameter.

\[ \text{Si} - \text{OH} + \text{Si} - \text{OH} \rightarrow \text{Si} - \text{O} - \text{Si} + \text{HOH}, \quad (1) \]

\[ \text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2(g), \quad (2) \]

\[ \text{Si} - \text{H} + \text{Si} - \text{H} \rightarrow \text{Si} - \text{Si} + \text{H}_2(g). \quad (3) \]

However, high temperature annealing is normally forbidden in most of compound semiconductor-to-silicon bonding due to thermal expansion mismatch and potential thermal material degradation or decomposition of compound semiconductors. Similar to Eq. (1), hydroxides of some metals M with high electronegativity are also able to polymerize to form covalent bonds at low temperatures as shown in Eq. (4). Bonding-related residual gases are, therefore, inherent to the bonding mechanisms in general. Embedding a thick layer of porous material such as thermal SiO2 or plasma-enhanced chemical vapor deposition dielectrics has been reported as an efficient outgassing medium for H2O and H2 diffusion and absorption, but it is not applicable for situations where a true integration with a proximity of two mating materials is needed. Different prebond surface treatment methods have also been employed to obtain strong InP-to-Si bonding by partially replacing surface hydroxyl (–OH) groups with other terminating groups though the question of how to effectively remove gas by-products still remains unanswered.

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Si – OH + M – OH → Si – O – M + HOH. (4)

Recently, a hybrid Si evanescent device platform has been developed to allow active optoelectronic components to be fabricated on the SOI substrate by low-temperature, O₂ plasma-assisted InP-to-Si wafer bonding.16,17 This represents a significant breakthrough toward realization of low-cost Si-based all optical communications. Achieving a strong, void-free bonding is of direct impact to device yield, performance, and reliability. Since light travels in a type of hybrid waveguide composed of both a thin Si device layer in the SOI substrate and a thin InP-based compound semiconductor in the epitaxial layers17,18 with a waveguide dimension of a few micrometers, even a small local delamination in micrometer regime may cause optical scattering or loss of the hybrid waveguide structure. Top-view Nomaski-mode microscopic images (50X) in Figs. 1(a) and 1(b) show the transfer of ∼2 μm thick InP epitaxial layers onto the SOI substrate after annealing at 300 °C for 2 and 15 h, respectively. Evenly distributed interfacial voids of 2–20 μm in diameters with a density of ∼55 093 cm⁻² indicate a serious outgassing issue in Fig. 1(a). Extended annealing from 2 to 15 h in Fig. 1(b) reduces the void density to ∼27 546 cm⁻², while the outgassing issue is not suppressed because bigger size voids appear due to gas aggregation from adjacent voids.

An empirical way to facilitate gas outdiffusion is to create suitable “drainage” pipelines by etching ∼10 μm wide trenches or grooves, herein “in-plane outgassing channels (IPOCs),” on single or double wafers and extend them to the chip edges so that a vacuum in postbond annealing helps pull gas molecules out of bonding interface through IPOCs.19 Figure 1(c) shows the top-view Nomaski-mode microscopic image of the InP epitaxial layers transferred to the SOI substrate with highlighted IPOCs on the SOI substrate. The bonded pair is annealed at 300 °C in a 5 × 10⁻⁴ Torr vacuum for 15 h. In contrast to Figs. 1(a) and 1(b) without any sort of outgassing channels, the area immediately above IPOCs in Fig. 1(c) exhibits no void formation while others appear in a 500 μm wide channel-free central area, indicating that the effectiveness of IPOCs depends on the spacing of the channels. However, some close-loop layout on the SOI results in the impossibility of gas by-products inside the loop diffusing out through IPOCs, causing voids at channel joints as shown in Fig. 1(d), for example, a Si hybrid evanescent racetrack-ring resonator. In addition to the disadvantage of inflexibility in SOI layout design, IPOCs may also allow undesirable gas and liquid to diffuse back in during the post-bonding device fabrication or device operation, which is likely to cause local debonding and a device reliability issue.

In this article, we propose and demonstrate the design of a type of highly efficient vertical outgassing channels (VOCs) for achieving low-temperature, robust, void-free thin InP epitaxial layer-to-SOI direct bonding. The VOC concept is presented first, followed by a discussion of the fabrication process. The outgassing effectiveness of VOCs, which is evaluated by comparing interface void density on transferred thin InP epixtal layers, is studied by varying VOCs’ spacing S (i.e., density) and dimension t. Over five orders of magnitude void density reduction to essentially void-free bonding interface is demonstrated when an optimal VOC design is employed. Up to 100X annealing time reduction is also shown to be sufficient for desirable bonding quality and surface energy, thereby highly improving the production efficiency. The universality and robustness of this bonding process with VOCs is manifested by a successful transfer of III-V material, with relatively poor bondability, to the SOI substrate. At the conclusion, to show the scalability of the bonding process successful direct bonding of 50, 75, and 100 mm diameter InP epitaxial layers onto the SOI substrate is demonstrated.

II. OUTGASSING PRINCIPLE OF VOCS

As illustrated in the cartoon image, Fig. 2(a), VOCs are
essentially an array of holes with a few micrometers in diameter and etched through the top Si device layer to the underneath buried oxide (BOX) layer prior to contact with the III-V material. The generated gas by-product molecules plus a small amount of trapped air molecules including any gaseous impurities can migrate to the closest VOC and can promptly be absorbed by BOX in Fig. 1(b). Thereafter, they may also gradually diffuse out through the BOX layer, due to its open network of only 43% of the occupied lattice space and its large diffusion cross section, generally 0.3–3 μm thick. The underlying chemistry of this outgassing mechanism is illustrated in the Eqs. (5)–(7).21

\[
\begin{align*}
H_2O + SiO_2 & \rightarrow Si - OH + OH - Si, \\
2Si - OH + 2Si & \rightarrow 2Si - O - Si + H_2(g), \\
2Si - O + H_2 & \rightarrow Si - OH + OH - Si.
\end{align*}
\]

It is well known that water vapor can reside in molecular form at interstitial sites in SiO2 to a depth of several hundred angstroms at room temperature. Upon entering the oxide network, the water vapor combines with the bridging oxygen ions to form pairs of stable nonbridging hydroxyl groups, a process illustrated in Eq. (5).21,22 The presence of these hydroxyl groups in the oxide also tends to render it more porous to diffusing species, which is beneficial to outgassing as well. Large hydrogen permeability in thermal SiO2 (Ref. 23) expedites the absorption of generated H2 in Eqs. (2) and (7). Trapped oxygen molecules are more inert and do not react with the oxide network, but can react with Si or diffuse as interstitial molecules in SiO2 with an energy barrier sensitive to the local oxide ring topology.22

Figure 2(c) is a side-view scanning electron microscope (SEM) image of VOCs with channel dimension t=6 μm squares and S=100 μm center-to-center spacing. SEM cross-sectional view of a corresponding VOC with ~2 μm III-V epitaxial layers bonded on the top is illustrated in Fig. 2(d), demonstrating intimate contact of III-V and Si with no III-V deformation above VOC. The absence and undercut of BOX is due to the wet etch of SiO2 hard mask in HF solution after transferring the VOC pattern from the hard mask to the Si device layer, and has no negative impact on the effectiveness of the VOC outgassing effectiveness. This process is discussed in detail below.

III. EXPERIMENT

A. VOC patterning and wafer bonding process

Commercially available 150 mm (100) SOI wafers (boron doped, 1–10 Ω cm) used in this work contain 1 μm Si device layer and 1 μm BOX layer. Patterning VOCs in the SOI substrate starts from growing 1 μm SiO2 in wet oxidation to be the hard mask after a modified RCA1 (NH4OH:H2O2:H2O=0.2:1.5, 80 °C) cleaning for 10 min (Ref. 24) and native oxide removal in HF solution (0.5%) for 30 s. Standard contact photolithography is conducted, followed by transferring VOC pattern to the SiO2 hard mask in buffered HF (BHF) solution (HF:H2O=1:7) for ~10 min. Upon stripping off the photoresist in solvent, the pattern is then further transferred to the Si device layer by inductively coupled plasma reactive ion etching silicon etch in BC13/Cl2 plasma. Prior to removing the SiO2 hard mask, the SOI sample is cleaned again in a solution of H2SO4:H2O2=3:1 at 100 °C for 10 min, leaving a dust-free surface. The InP-based III-V sample cleaved from the 50 mm metal-organic chemical vapor deposition-grown epitaxial wafer is cleaned in acetone and isopropyl alcohol with gentle physical swab. Immediately after removing SiO2 hard mask on the SOI sample and native oxide on the III-V sample in BHF and NH4OH (39%) solutions, respectively, O2 plasma surface treatment is proceeded on both samples in a commercial EVG 801 LowTemp Plasma Activation System for 30 s. A thin (<5 nm) layer of highly strained native oxide is grown on both SOI and III-V samples,25 resulting in a very reactive hydrophilic surface. Subsequently, after contact with a solution rich in hydroxyl groups, for example H2O or H2O-rich solutions, higher surface hydroxyl group (–OH) densities are attainable.4 The final activation step involves terminating the hydrophilic surfaces with hydroxyl groups. It has been reported that surface activation in NH4OH solution resulted in higher bonding surface energy due to the conversion of some Si–OH to Si–NH2 possessing higher bond strength.24,26 Instead of dipping the samples in NH4OH solution directly, a NH4OH vaporization process has been developed to result in a more uniform and cleaner surface activation.27 The SOI and III-V samples are placed on a 125 °C hot plate with a glass cover for 5 min to introduce NH4OH vapor and vaporize liquid trapped in the VOC cavities, avoiding the gasification in the elevated temperature annealing which can subsequently cause debonding. Spontaneous mating at room temperature is then carried out manually. Further annealing at 300 °C is conducted in a commercial Suss SB6E wafer bonder to obtain strong covalent bonding. Relatively high external pressure is required to obtain high-quality bonding, as discussed in Sec. III below. The InP substrate is finally etched off in a solution of HC1:H2O=3:1 at room temperature, leaving a 200 nm InGaAs etch stop layer and a 2 μm thick InP-based epitaxial layer on the SOI substrate. The interfacial void density is then obtained by carefully counting the number of voids using a microscope in Nomaski mode for the best contrast.

B. Design of experiment

In order to study the outgassing efficiency of VOCs, a pattern with variable VOC spacing S and dimension t was designed. Figure 3 shows the VOC mask of a 9×9 mm2 square area for patterning 1×1 cm2 SOI sample with 1 mm wide stripe region around the edge for photoresist edge bead removal. Four 3×3 mm2 square regions with VOC spacing of 50, 100, 200, and 400 μm are located on the 9×9 mm2 mask area with 1 mm non-VOC margin to each other and the sample edge, minimizing the interaction among different regions and possible gas product diffusion and es-
cape to the sample edge. Square shape is used for all VOCs with the dimension varying from 2, 4, 6, to 8 $\mu m$ on four respective mask areas.

IV. RESULTS AND DISCUSSION

A. Interfacial void density studies

Red dash-line boxes in Figs. 4(a) and 4(b) of Nomaski-mode microscopic images (50X) highlight a VOC region of $S=50 \mu m$ around the sample corner, and regions of $S=50 \mu m$ (left) and $S=100 \mu m$ (right) with 1 mm non-VOC margin in between, respectively. The actual VOCs on the SOI substrate are about $9 \times 9 \mu m^2$ square holes with slightly rounded angles due to isotropic BHF wet etch in patterning the SiO$_2$ hard mask. The bonded pair is annealed at 300 °C for only 30 min with about 3 MPa external pressure applied. Evident void density reduction down to nearly zero is visible in VOC region of Fig. 4(a) while a great number of uniformly distributed voids still exist at non-VOC corner with density slightly decreasing toward VOC region due to smaller diffusion path to VOCs. A similar situation is exhibited in Fig. 4(b) where non-VOC central area with many voids is sandwiched by void-free $S=50 \mu m$ and $S=100 \mu m$ regions.

Figure 5 represents the relationship of interfacial void density versus channel spacing $S$ with different channel dimensions $t$ for bonded pairs annealed for 2 h at 300 °C with 3 MPa external pressure. Void density on the sample in Fig. 1(a) is plotted as a reference.

Fig. 3. VOC pattern design of experiment to study outgassing efficiency as a function of channel spacing $S$ and size $t$.

Fig. 4. Nomaski-mode microscopic images of an InP-SOI bonded pair after 300 °C annealing for 30 min, showing noticeable contrast between (a) VOC region ($S=50 \mu m$) and non-VOC corner, and (b) VOC regions ($S=50$ and 100 $\mu m$) with a 1 mm wide non-VOC margin in between.

Fig. 5. Interfacial void density vs VOC spacings of $S=400$, 200, 100, and 50 $\mu m$, and sizes of $t=9$, 7, 5, and 3 $\mu m$ for bonded pairs annealed for 2 h at 300 °C with 3 MPa external pressure. Void density on the sample in Fig. 1(a) is plotted as a reference.

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slightly smaller effective contact area, i.e., less surface hydroxy group contribution to gas by-product generation. Hence, parameter $t$ becomes the second-order influence factor for outgassing. It is noted that void density data in Fig. 5 are average numbers obtained from bonding 1 cm$^2$ samples with four isolated channel regions (Fig. 3) and 1 cm$^2$ individual ones with single VOC scheme.

It is well known that longer annealing time normally leads to stronger bonding surface energy which begins saturating to a maximum value after a certain period of annealing time when generated gas by-products are removed, either by absorption or diffusion, from the bonding interface completely. Thus, it is of interest to determine if there is a similar outgassing efficiency threshold in terms of annealing time. Interfacial void density as a function of annealing time at 300 °C is illustrated in Fig. 6. Similar outgassing efficiency is found on bonded pairs annealed for 2 h and 30 min while bonded pairs annealed for only 10 min shows significantly higher void density, indicating that outgassing efficiency may primarily rely on the amount of time for the gas transportation to the VOCs. The minimum annealing time at 300 °C annealing temperature in this work is likely to be around 30 min for the best outgassing efficiency. Further annealing time reduction in this temperature is believed to be attainable by reducing VOC spacing $S$.

Herein we note that previous low-temperature bonding with IPOCs needs 15–18 h annealing to obtain low void density (10–20 cm$^{-2}$) bonding, comparable to that of 30 min annealing with VOC design. Zhang and Raskin studied the void formation in low-temperature Si–Si bonding without any type of outgassing channels. A longer annealing time (>100 h in some cases) was found necessary to reach the saturation of bonding polymerization reactions, and stop new void formation, which supports the hypothesis that the efficiency in gas by-product removal determines the bonding quality and required annealing time, i.e., production efficiency.

Unlike the IPOC bonding process, the new process with VOC design requires higher external pressure to hold samples in position and prevent the debonding or local deformation of III–V material since trapped air in VOCs expands as soon as temperature ramping begins. Assuming a worse case scenario where the mass of trapped cleanroom ambient air (99% of O$_2$ and N$_2$) is constant (i.e., no absorption or diffusion in Si or BOX layer) through the entire temperature cycling from room temperature (20 °C) to 300 °C and back to room temperature, the required additional pressure can be calculated from the well-known Gay–Lussac’s Law in Eq. (8) since O$_2$ and N$_2$ can be treated as an ideal gas at relatively low temperature. $T, P_T, P_0$ in Eq. (8) represent the temperature $T$ in degree Celsius and the pressures at temperature $T$ and 0, respectively. The maximum internal pressure of $P_{300°C}$ in a VOC cavity is, therefore, 1.96 times greater than the pressure at 20 °C, $P_{20°C}$ at which VOC cavity is formed on spontaneous mating. $P_{20°C}$ herein is also equal to the pressure of 1.24 MPa, routinely used for bonding pairs with IPOCs in our laboratory in order to minimize the surface microroughness on III–V surface since no gas expansion takes place in a vacuum annealing chamber for the IPOC case. Thus, a pressure of 2.43 MPa is required to overcome the gas expansion and achieve the same quality bonding for VOC case as that of IPOC case.

$$P_T = P_0 \left(1 + \frac{1}{273.15} \frac{T}{T_0}\right).$$

Figure 7 shows the experimental data of interfacial void density versus external pressure for bonded pairs with $t=7$ μm and $S=100$ μm after 300 °C annealing for 1 h. Extremely high average void density over 4000 cm$^{-2}$ appears at bonded pair with no external pressure applied as expected, and decreases to around 290 cm$^{-2}$ when the regular 1.24 MPa used for IPOC case is applied. Low void density of 27 cm$^{-2}$, comparable to IPOC case (18 h annealing), is obtained when pressure is increased to 3 MPa, 2.41X of 1.24 MPa. The slightly higher pressure than the calculation from Gay–Lussac’s model in our experiments is believed due to the contribution of aggregation of H$_2$O gas by-product and small amount of trapped, tiny, airborne, organic particles, in addition to the potential error of the ideal Gay–Lussac’s model as compared to the real world application. The inset

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**Fig. 6. Interfacial void density as a function of annealing time periods of 10, 20, and 120 min for VOC spacings of $S=400, 200, 100$, and 50 μm, and fixed size of $t=9$ μm for bonded pairs annealed at 300 °C with 3 MPa external pressure.**

**Fig. 7. Interfacial void density as a function of external pressure for bonded pairs of $t=7$ μm and $S=100$ μm after 1 h annealing at 300 °C, showing that 3 MPa is required for VOC design in contrast to conventional 1.24 MPa pressure used for IPOC design. Inset: a 2×2 cm$^2$ mirrorlike InP epitaxial layers transferred to the SOI substrate with 3 MPa pressure applied.**
image in Fig. 7 is a 2×2 cm² sample annealed for 2 h at 300 °C with 3 MPa external pressure. A mirror-like epitaxial layer transfer is achieved after selectively removing the InP substrate. Lower pressure would be sufficient if spontaneous mating at room temperature is conducted in a vacuum environment.

**B. Bonding strength characterization**

It is not practical to apply external pressure during post-bonding device processing (up to 320 °C) after removing the InP substrate. Prevention of III-V delamination due to trapped gas expansion in VOC cavities relies on the surface energy of the bonded area around VOCs. Hence, bonding strength (i.e., surface energy) after annealing represents another critical factor in evaluating the bonding quality. In a Class 1000 clean room environment the standard crack-opening method is performed on about 1×1 cm² bonded pairs which are annealed for only 30 min. This appears to be sufficient for efficient outgassing in Fig. 6. Longer annealing time normally results in equal or higher surface energy so that only 30 min annealed samples are used for this measurement. Two opposite edges of SOI samples used in this measurement are angularly polished to a 45° angle at the bonding surface, allowing a 100 μm thick blade to be easily and repeatedly inserted into the correct bonding interface. The top InP samples with ~400 μm InP substrate remaining, however, are all broken at or before reaching the boundary of contacted area when the blade is attempted to be inserted through as shown consistently in the void-free infrared transmission images of Figs. 8(a) and 8(c), thus resulting in a failure to determine the equilibrium crack length. Yellow dot line in Figs. 8(a) and 8(c) highlights the contacted areas with respective VOCs of S=50 μm and t=9 μm and S =200 μm and t=7 μm, showing the crack of InP substrate close the edge of the VOC pattern. The blade stops at the positions shown in the figures when crack of InP presents. Figures 8(b) and 8(d), the respective top-view microscopic (25X) images for the blue dash-line boxes in Figs. 8(a) and 8(c), further confirm the maintaining of intimate InP–SOI contact so that InP breakage follows the contact boundary strictly. A small fringe of the top Si layer, between exposed BOX green border (from the step of photoresist edge bead removal) and InP substrate in Fig. 8(d), indicates relatively lower surface energy compared to the bonded pair with S =50 μm and t=9 μm in Fig. 8(b), which is expected due to significantly higher void shown in Fig. 5. The crack of the InP substrate on small size samples indicates the likelihood of the bonding surface energy higher than the fracture energy of bulk InP. A similar case that Maszara reported in measuring hydrophilic Si–Si bond as well. Accurate determination of the bonding surface energy requires a thinner blade and larger size samples with thicker InP substrate, which is much more expensive and beyond the scope of this work.

Alternatively, III-V–SOI bonded samples experience a harsh dicing test, a standard process for fabricating the Fabry-Pérot cavity devices as well. The bonded sample of only 2.2 μm thick epitaxial layers on the SOI substrate is cut by a 100 μm thick blade with over 10 000 rounds/min spin rate. Although the III-V side is up and there is no surface protection during dicing, the chipping of III-V epitaxial layer is no more than 6.2 μm and follows the SOI epitaxial material is covered by a layer of dicing dust shown in Fig. 8(e), also demonstrating the achievement of strong bonding. The III-V epitaxial material is covered by a layer of dicing dust shown in Fig. 8(e), proving that no type of surface protection is employed during the dicing test.

Another thermal cycling step of baking bonded pairs to 250 °C in the air for 5–10 min after the InP substrate removal is routinely employed to further verify the bonding strength since any voids become more visible with trapped gas by-products at bonding interface. On the other hand, remaining gases in VOC cavities would be able to cause delamination in this bake step if the bonding strength was not sufficiently strong to hold the III-V epitaxial layer and SOI together. No noticeable deformation or delamination of transferred III-V layers at or around VOCs is found, indicating high surface energy in the entire contacted area and a possible decrease in gas pressure inside VOC cavities from either absorption or diffusion. Void densities of S=50 and 100 μm cases remain constant after an additional bake (data not shown), showing the completed outgassing process and excellent reliability of this bonding process. This same test was performed on a sample bonded over 2 months earlier,
and no change in terms of void density and III-V deformation was noticed (data not shown), which indicates that H₂O absorption in the BOX layer [Eq. (5)] is not reversible as well.

It is also interesting to note that interfacial void formation characteristic is closely associated with surface states of materials, including surface roughness, surface epitaxial defects, hydroxyl group density after O₂ plasma treatment, etc. Figures 9(a) and 9(b) reveal the similar areas of bonded pair with III-V material from a different vendor after 300 °C annealing for 30 min as shown in Fig. 4. Unlike the high density of small size voids (<20 μm in diameter) in Fig. 4(a), voids in non-VOC areas display arbitrary shapes with more than 200 μm in one direction in Fig. 9. This is primarily due to a larger number of surface defects in this epitaxial wafer which are preferable nucleation sites for gas aggregation.¹³

The slightly rougher surface is helpful for gas by-product migrating relatively long distances to gather at nucleation sites. Bonding on 1 cm² sample without VOCs or IPOCs fails (data not shown) because the InP epitaxial layers are totally delaminated during postannealing substrate removal in HCl solution, indicating a intrinsically poorer bondability of this type of wafer and serious outgassing problems. Nevertheless, high-quality, void-free bonding is still attainable with the help of VOCs as shown in Fig. 9 where regions of S=100 μm and 50 μm (t=9 μm) are highlighted with red boxes. This demonstrates a robust and universal benefit of this process that can potentially lower the criteria for bonding wafer selection thereby greatly reducing the overall cost of manufacture. It should be noted that although the VOC model discussed above describes the general outgassing principle with the aid of a “gutter” layer, such as the BOX layer in this work, the values of interfacial void density observed in our experiments represent only those particular sets of wafers tested in particular conditions. More detailed studies on interfacial void formation characteristics associated with SOI and III-V material properties, surface chemistry and bonding process is underway.

Finally, the outgassing mechanism proposed and demonstrated in this article is further confirmed by accidentally not etching down to the BOX layer as shown in Fig. 10(b), a SEM cross-sectional image of a yellow dash-line highlighted region in Fig. 10(a). Due to the photoresist buildup at the edge of the sample, some VOC pattern is not transferred to the SiO₂ hard mask perfectly, resulting in Si device layer that is not completely etched through in some VOCs. Aggregated gas and trapped gas in VOCs cause the noticeable deformation of InP thin epitaxial layers, shown by those bouffant bubbles in some VOC sites in Fig. 10(a). Cleaving through the bubble in Fig. 10(b) releases trapped gases and subsequently the internal pressure, but poor bonding surface energy can be qualitatively judged by perfect InP breakage along its (100) crystalline orientation. Unlike the strong bonding showed in a similar cross-sectional view in Fig. 2(d), poor bonding in Fig. 10(b) results in the Si and InP broken independently upon cleave, showing nice (100) facet on InP and rough facet on the Si device layer.

C. Bonding scalability

According to the Figs. 5–7, each VOC appears capable of accommodating limited gas by-products from a neighboring region in a certain time period, resulting in an effective area coverage as a VOC at the center. Ideally, void-free bonding can be achieved as long as area coverage starts overlapping each other, eliminating the existence of the “dead zone,” which is most likely to be the case of S=50 μm in this work. In other words, the outgassing issue can be fundamentally eliminated if VOCs, with the appropriate scheme is employed, regardless of the wafer dimension. Figure 11 demonstrates the successful transfer of 50 mm (2 in.), 75 mm (3 in.), and 100 mm (4 in.) diameter InP-based epitaxial layers onto the SOI substrate with VOCs of S=100 μm and t=7 μm. The bonded wafers are annealed at 300 °C for 2–3 h with 3 MPa pressure, showing the same bonding quality as 1 cm² samples. To the best of our knowledge, 100 mm bonding is the record large InP-to-Si direct wafer bonding.
i.e., no interfacial oxide or polymer adhesion layer. The success in applying this same bonding process to variable sizes of wafer bonding demonstrates promising process scalability with VOCs provided that wafers are clean, flat, and smooth.

D. Additional advantages

This design of VOCs embraces several more merits and processing benefits in addition to those discussed above.

1. In contrast to previously used IPOCs where gas and liquid can flow back in, bonding with VOCs isolates the bonding interface completely from the outside environment, thereby improving bonding stability. Furthermore, the negative impact of local III-V breakage or peel off due to interface particles, surface scratches, or defects is small (data not shown) since the rest of bonded area is not subject to damage by hazardous gases or liquids.

2. Owing to the compatibility of the vertical outgassing process with conventional in-plane circuits and component layout, a flexible device pattern design is available.

3. A small footprint on SOI substrate even for VOCs with small spacing and relatively large dimension (i.e., $S=50 \ \mu m$ and $t=9 \ \mu m$ in this work) results. Table I lists the percentage of unbonded area due to the absence of etched Si material. A maximum of 3.24% area consumption leaves plenty of room for high-density device integration, and optical, electrical, and thermal interaction between SOI and III-V layers.

(4) Preliminary x-ray diffraction study (data not shown) indicates that VOCs may even serve as a “stress-relieving” pattern,$^{29}$ which contributes to void suppression, allowing thermally mismatched films to withstand postbonding device processing, and minimizing stress-induced defects. Further investigation is required to understand the underlying physics therein.

5. There are multiple ways to pattern and form VOCs which can be in combined into various and multiple shapes such as squares, circles, rectangles, etc. The thermal annealing with VOCs does not require vacuum or forming gas either. No difference is noticeable for using SOI wafers with 1 and 3 $\mu m$ BOX layer. This can all be achieved from this novel and flexible low cost fabrication process.

V. CONCLUSIONS

A simple, novel VOC concept has herein been introduced and the underlying chemistry discussed in detail. The primary gas by-products of H$_2$O and H$_2$ from bonding polymerization reactions at low temperature are absorbed by the thick BOX layer in SOI substrate through VOCs. Dramatic interfacial void density reduction up to five orders of magnitude from $50000 \ \text{cm}^{-2}$ to $3 \ \text{cm}^{-2}$ is demonstrated on properly selected VOC scheme when only thin InP epitaxial layers are left on the SOI substrate, demonstrating an extremely efficient outgassing capability. The required minimum annealing time period at 300 $^\circ$C is between 10 and 30 min for optimal bonding quality, the time period for the entire outgassing process to complete as well. It represents 36–108x time reduction compared to the previous IPOC design, and is an even larger reduction for the case of no outgassing channel. A 3 MPa external pressure has been found

![Fig. 11. 50 mm (2 in.), 75 mm (3 in.), and 100 mm (4 in.) InP epitaxial layers directly bonded to the SOI substrate with VOC of $t=7 \ \mu m$ and $S=100 \ \mu m$ after 300 $^\circ$C annealing for 2–3 h, showing a mirrorlike epitaxial transfer which leads to some reflection, i.e., a bright bar for 50 mm one and dark bars for 75 and 100 mm ones.](image-url)
necessary to overcome the expansion of trapped air in VOC cavities. Bonding strength is characterized by crack-opening method and a harsh dicing test, both showing high surface energy. An additional thermal bake step also exhibits the stability and reliability of bonding with VOCs. The robust and universal benefit of this VOC design is confirmed by the same demonstrated outgassing efficiency when the identical process is applied to two different InP epitaxial wafers with good and poor bondability. The successful epitaxial transfer of 50, 75, and 100 mm InP wafer to SOI substrate demonstrates great promise in further tooling up for mass production, indicating that VOC design is wafer scale independent and represents an approach to fundamentally resolve the outgassing problem in SOI-based direct wafer bonding. Moreover, several incidental advantages in device design and fabrication, bonding reliability, and bonding stress minimization are mentioned as well. The same outgassing principle can thus be applied to other low-temperature homogeneous or dissimilar material integration with a gutter layer involved.

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10 See http://soitec.com/en/about/ for showing commercially available 200 mm SOI substrates.