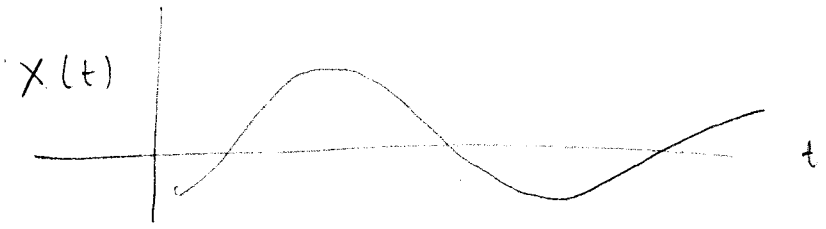
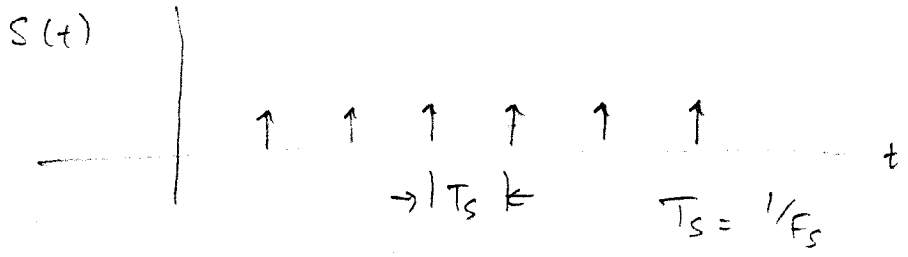
ECE594A Lecture Notes

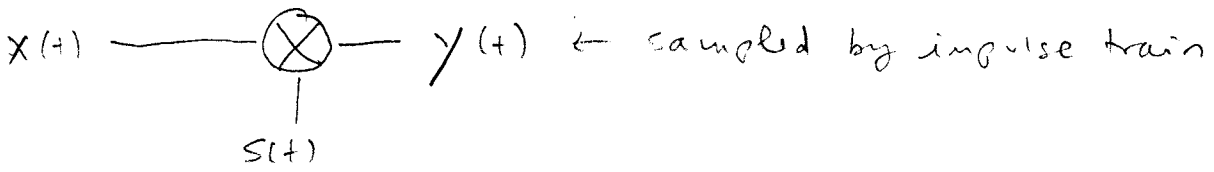
Track and Hold

1. Sampling basics
2. Sample-hold/track-hold performance metrics
    - Acquisition time
    - Settling time
    - Droop rate
    - Pedestal error
    - Aperture uncertainty
3. Basic MOS switch sampler
4. Nonidealities
    - Input dependent resistance
    - Charge injection
    - Clock feedthrough
    - Hold feedthrough
    - Output voltage limitation
5. Signal to noise limitations
    - Quantization error
    - Aperture error
    - Thermal noise
    - Signal to distortion ratio
6. Methods for improving MOS samplers
7. Diode bridge sampler
8. Emitter follower sampler

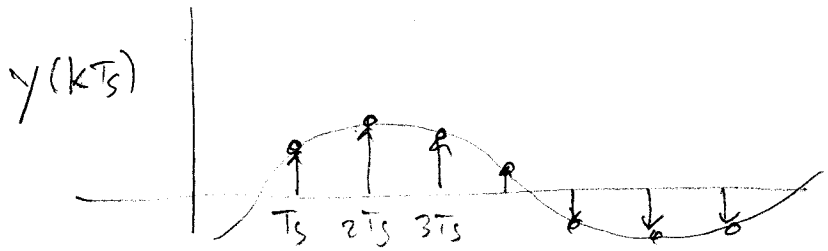
Sampling of Continuous Time Signals (Ideal)







← sampled by impulse train



$$y(t) = x(t) \cdot \sum_{k=-\infty}^{\infty} \delta(t - kT_s) = y(kT_s)$$

discrete samples at intervals kT_s.

Frequency response. Take Fourier Transforms

$$X(f) = \sum x(t)\, e^{-j2\pi f t}$$

$$\mathcal{F}(\delta(t)) = 1$$

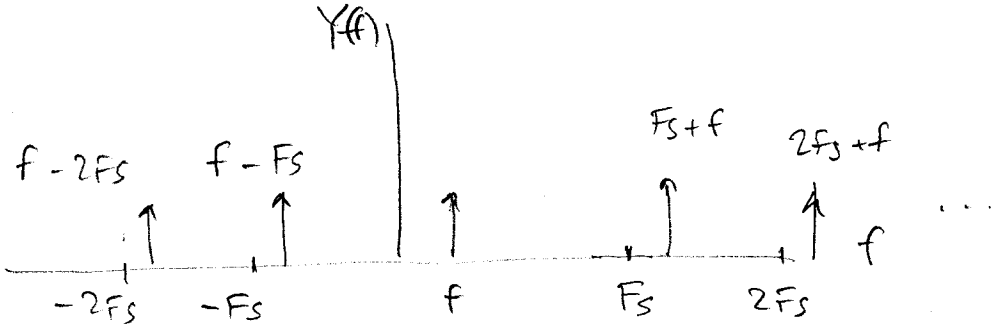
(convolution)

$$Y(f) = X(f) * \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_s}\right)$$

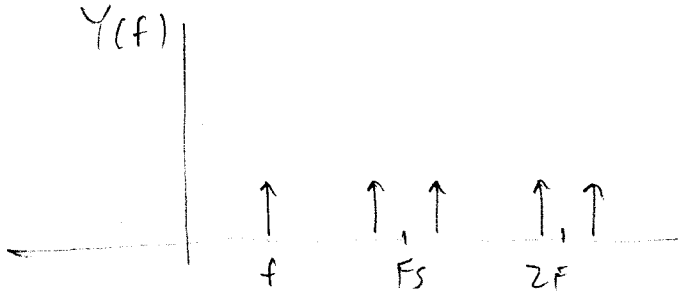
$$= \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right)$$

We see that the signal is replicated at intervals of $n \cdot \frac{1}{T_s}$.

Suppose $x(t) = \cos 2\pi f t$



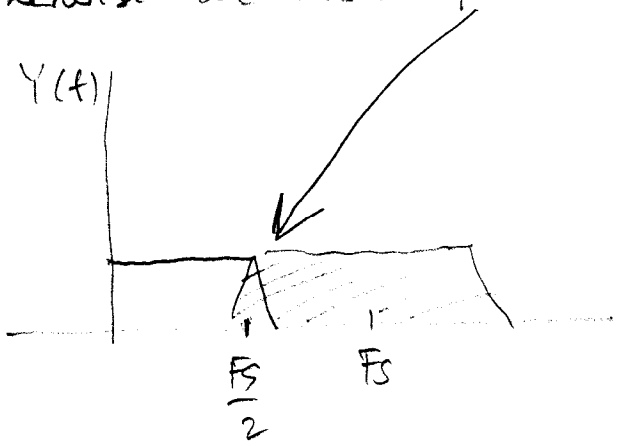
If we neglect phase and consider only positive freq.



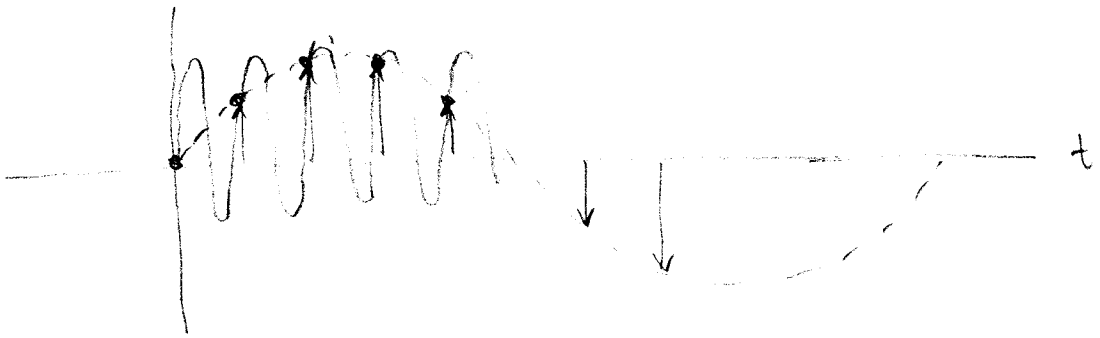
We see that the signal is replicated (shifted) in frequency. This can lead to the problem of aliasing.

$2f < F_s$ (Nyquist rule)

otherwise we have spectral overlap



Also, we could not distinguish a signal at $f + nF_s$ from a signal at f.



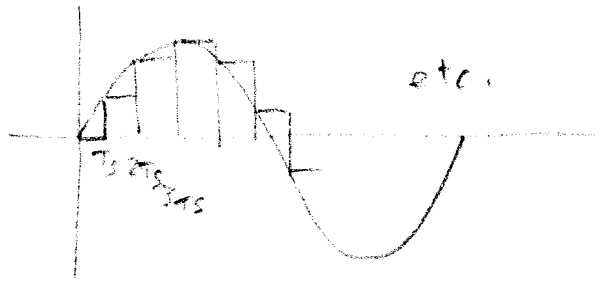
Same sample values.

So, for Nyquist rate sampling, sampled signal must be band limited to below $\frac{F_s}{2}$.

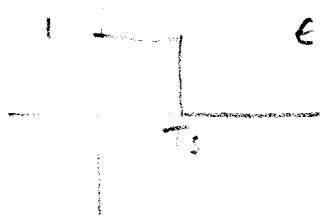
1. LPF
2. Higher than Nyquist sampling rate

Hold Function (zero order)

Since it is impractical to generate impulse trains, the sampled value is generally captured and held for $\epsilon \leq T_s$.

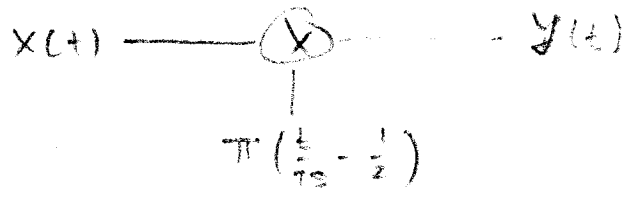


so, we have a rectangle function $\Pi\left(\frac{t}{T_s} - \frac{1}{2}\right)$



$\epsilon = T_s$

$= u(t) - u(t - T_s)$



This has the effect of taking the periodic train of impulses and convolving with the rectangle.

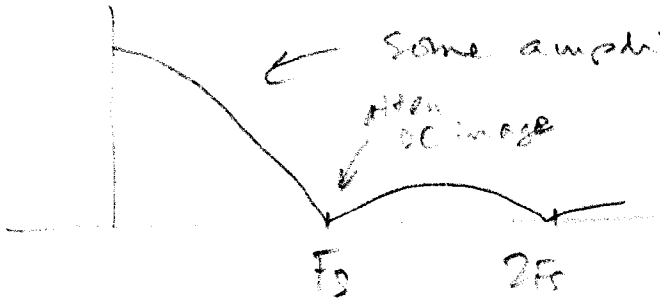
$$y(t) = \left[x(t) \sum_{k=-\infty}^{\infty} \delta(t - kT_s) \right] * \Pi\left(\frac{t}{T_s} - \frac{1}{2}\right)$$

So we multiply freq. responses to get spectrum of sample-hold.

$$Y_{SH}(f) = Y(f) \cdot \mathcal{F}\left\{\Pi\left(\frac{t}{T_s} - \frac{1}{2}\right)\right\}$$

$$= \underbrace{e^{-j\pi f T_s}}_{\text{phase}} \cdot \frac{\sin(\pi f T_s)}{\pi f T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right)$$

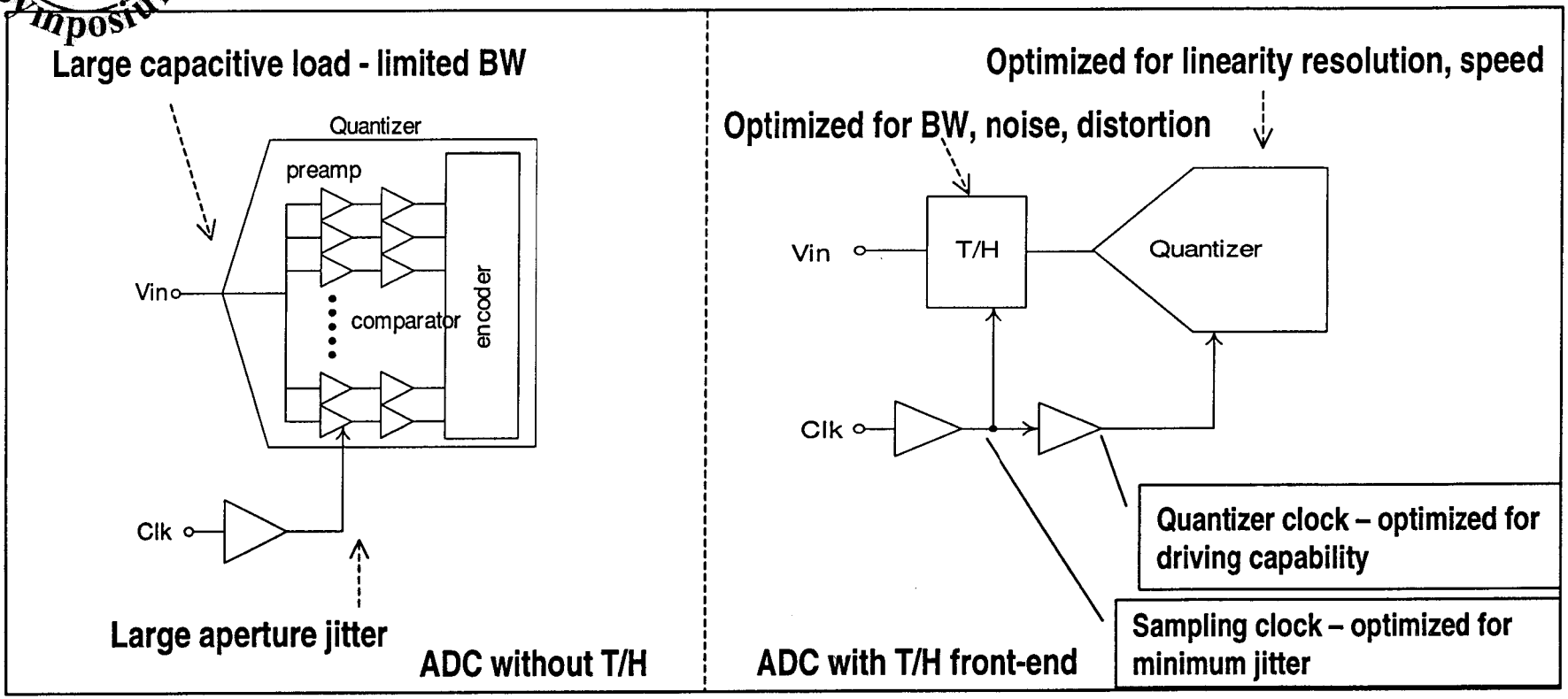
$$|Y_{SH}(f)| = \left| \frac{\sin(\pi f T_s)}{\pi f T_s} \cdot Y(f) \right|$$



can be corrected by equalizing inverse sinc filter if necessary (in case of DAC for example).

ADC doesn't need correction —
samples the held signal — ideal case.

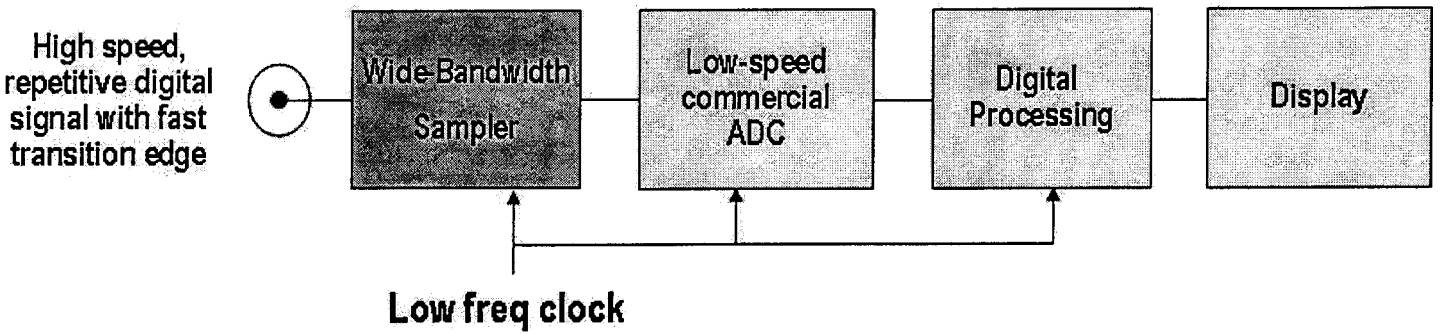
Why Track and Hold?

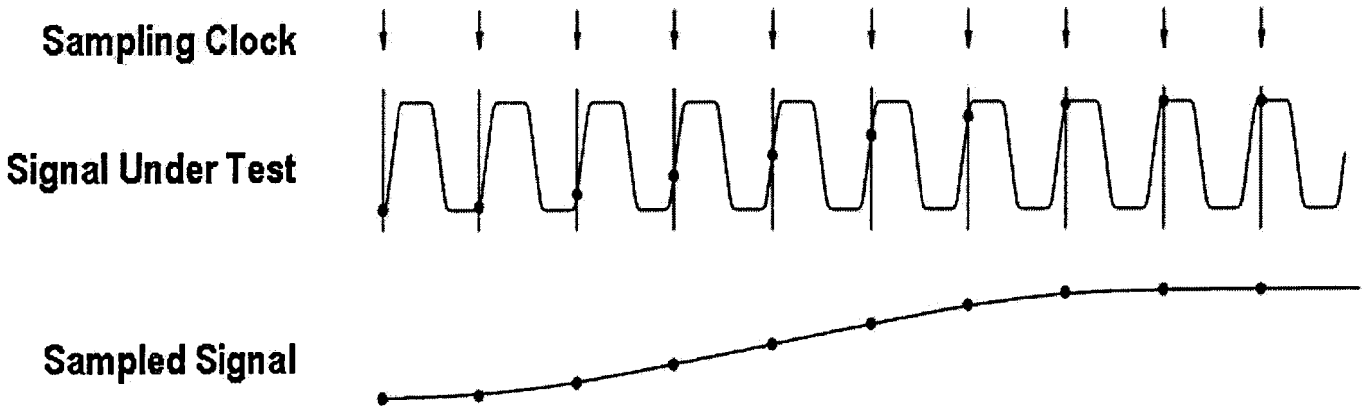


- T/H is essential for multi-stage ADC architecture
  - Pipeline ADC
  - Subranging ADC
  - Folding converter
  - Algorithmic converter

Wide-band T/H in sub-sampling application

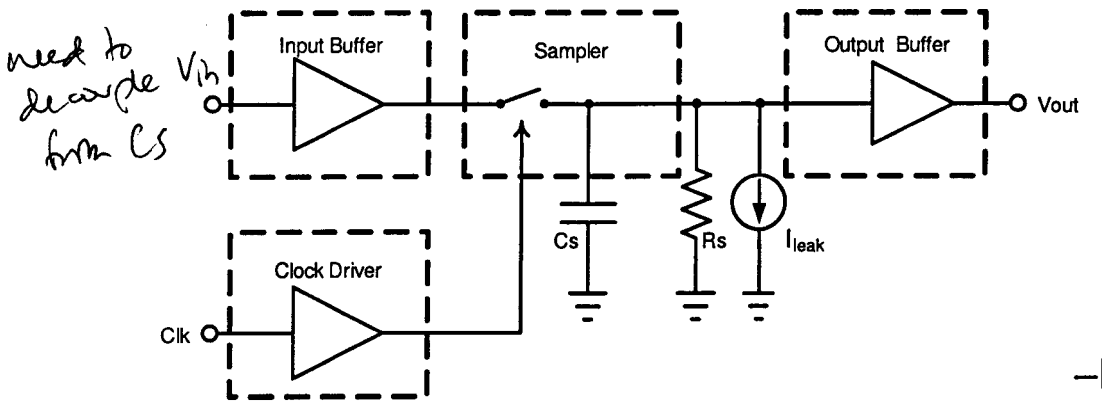
- **Used in ATE, Oscilloscope, Jitter Measurement, Signal Integrity Tester for OC**





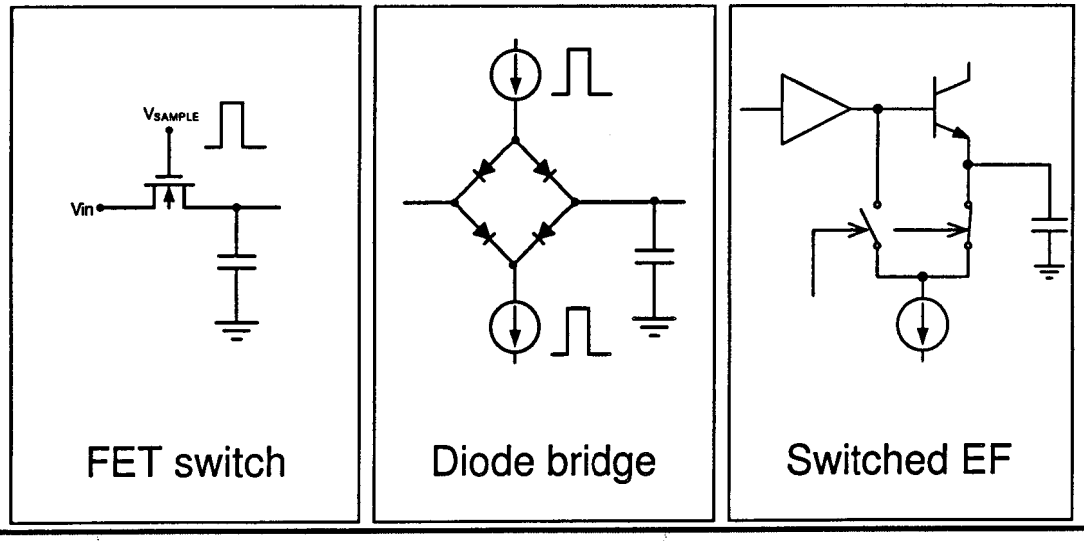
T/H architectures

Input buffer / Sampling switch / Hold capacitor / Clock driver / Output buffer



A/D can have very high C_{IN}

Sampler implementation

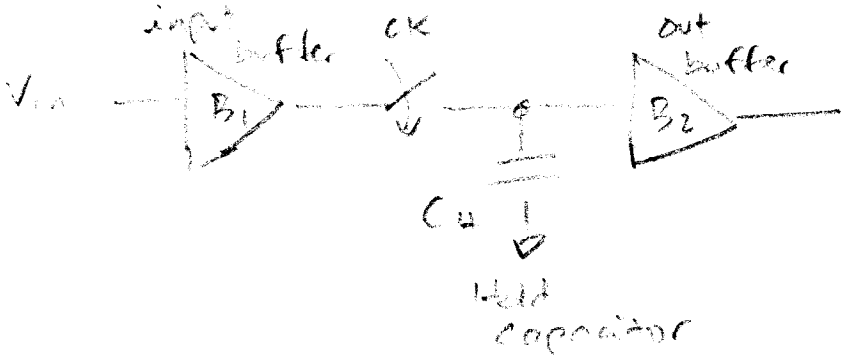


–FET switch
- No static power
- Non-linear charge injection
- Limited bandwidth

–Diode bridge
- Widest bandwidth

–Switched emitter follower
- Good linearity, large dynamic range

Simple open loop S/H



at $t = nT_s$, switch closes.

Acquisition Time:

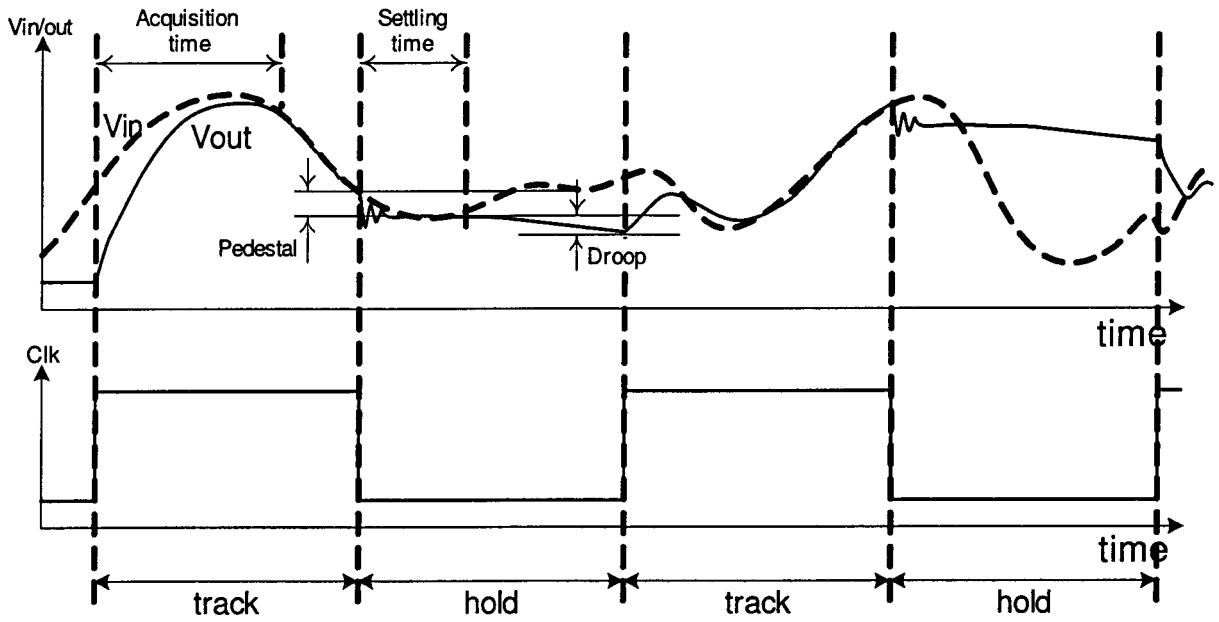
time to experience full scale transition and settle within an error band.
(full data path)

Hold Settling Time.

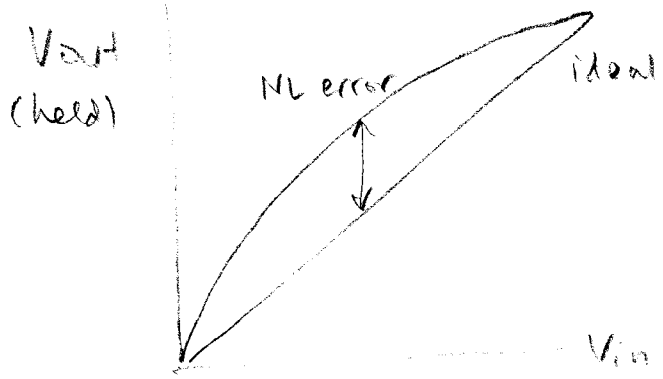
B_2. time after hold command to settle within error band

DR. Max input − Min input

T/H operation



- Performance requirement
  - Large track mode bandwidth
  - Small track mode distortion
  - Low noise
  - Small or linear pedestal error
  - Small droop
  - Fast recovery



Pedestal.

error when switch from sample to hold

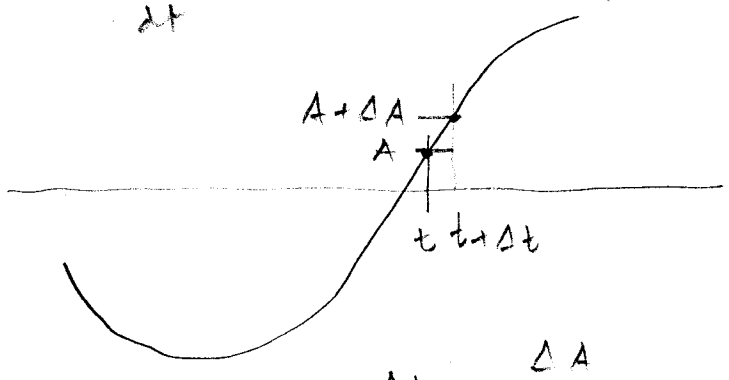
Droop.

discharge of C_H

Aperture Jitter or Uncertainty

Let $V_{in} = A \sin \omega t$

$$\frac{dV_{in}}{dt} = A\omega \cos(\omega t)$$



$$\Delta t = \frac{\Delta A}{A\omega \cos \omega t}$$

For N bit accuracy, $\left(\pm \frac{1}{2} LSB\right)$

$$\frac{\Delta A}{2A} < \frac{1}{2^N} \qquad \Delta t = \frac{2A}{2^N \cdot A\omega \underbrace{\cos \omega t}_{1}}$$

So,

$$\Delta t < \frac{2^{-N}}{\pi f_{in} \cos(2\pi f_{in} t)} = \frac{2^{-N}}{\pi f_{in}}$$

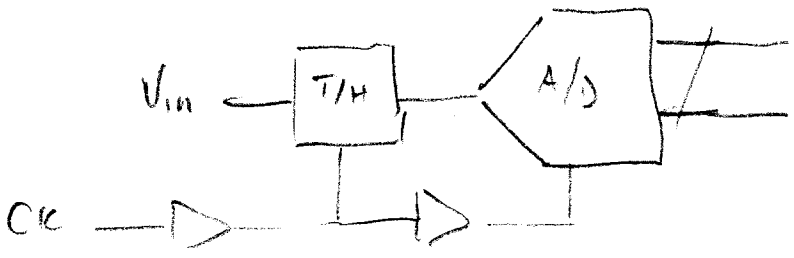
(for greatest slope)

ex. 14 b, 500 MHz

$$\Delta t < 40 \text{ fs}$$

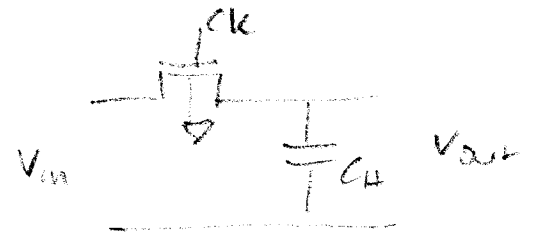
serious requirement for high speed samplers, ADCs.

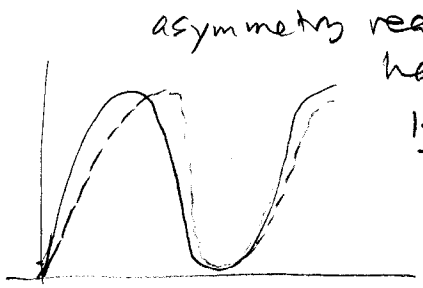
of course, placing T/H before A/D is helpful — can be optimized for minimum aperture jitter and allows A/D to be optimized for accuracy and/or speed



MOS Switch

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$





problems:

1. Resistance depends on V_{GS} which depends on V_{in}.

   V_{in} would like large width W to get more speed.

   R_{on} ↓ , t_{acq} ↓

   t_{acq} will depend on V_{in}

2. Charge injection.

$$Q_{ch} \approx WL C_{ox} (V_{GS} - V_{TH})$$

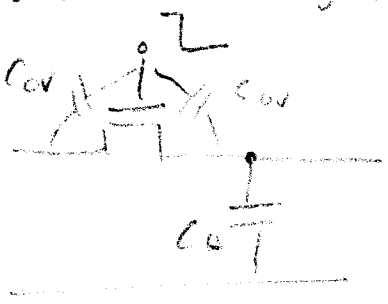
when turn off device, this channel charge must leave through S/D. This causes a gain error since Q_{ch} depends on V_{GS}.

V_{TH} depends on body effect.

This can introduce nonlinear $Q_{ch}(V_{in})$.

HD, IMD is generated.

3. Clock Feedthrough



$$\Delta V_{out} = \frac{C_{ov}}{C_{ov} + C_L} V_{ck}$$

overlap cap Cov

charge sharing

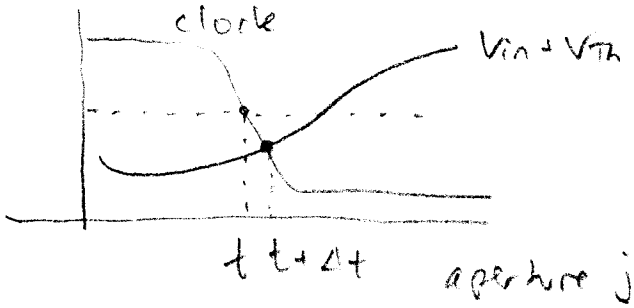
produces offset error

4. Sampling instant depends on Vin.

Switch turns off when $V_{GS} - V_{TH} < 0$.

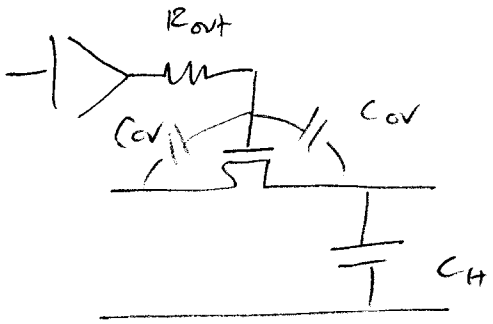
But, V_{GS} depends on Vin.

need fast clock edge

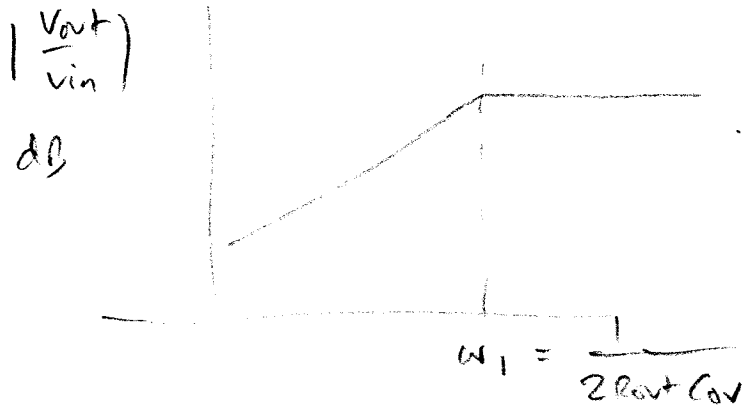


aperture jitter is signal dependent.

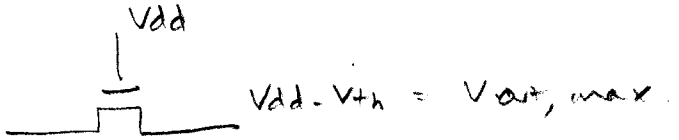
5. Hold feedthru.

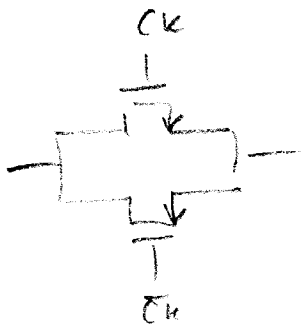


$$\frac{V_{out}}{V_{in}} = \frac{C_{ov}}{C_H} \frac{R_{out} C_{ov} s}{2 R_{out} C_{ov} s + 1}$$



6. Reduced output range.





avoids threshold drop
rail - rail

Less resistance, variation.
charge injection not helped: different $V_{GS} - V_{th}$

Today (Lec 3)

Sig/Noise limiters.

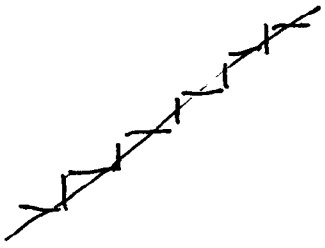
- Quantization error
- SNR due to aperture – sig. dependence
- SDR
- Thermal Noise

Methods for improvement of samplers

Quantization error

$$y = Gx + e$$

Gain → straight line through center



$\pm \frac{\Delta}{2}$ = error bound.

m = # bits

Signal power: $P_S = \frac{A^2}{2} = \frac{(2^{m-1}\Delta)^2}{2} = 2^{2m-3}\Delta^2$

Quantization Noise power:

$$P_n = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12}$$

SNR due to quantization noise:

$$SNR = \frac{P_S}{P_n} = \frac{2^{2m-3}\Delta^2}{\Delta^2/12} = \frac{3}{2}2^{2m} = (6.02m + 1.76)d$$

We saw that very small aperture uncertainty was needed for high frequency TH to remain accurate to $\pm \frac{1}{2}$ LSB.

Another way to look at this is to consider the maximum signal-to-noise ratio that can be attained by a given aperture uncertainty τ.

$$SNR = 20 \log \left[\frac{V_{FS}\,(rms)}{Noise\,(rms)} \right]$$

$$V_{FS}\,(rms) = \frac{V_{FS}}{2\sqrt{2}} \qquad \left(\text{full scale}/2 \cdot \frac{1}{\sqrt{2}} \right)$$

$$N\,(rms) = \tau \cdot \left[\frac{d(V_{in})}{dt} \right]_{rms}$$

$$= \tau \cdot \sqrt{\frac{1}{T} \int_0^T \left(\frac{dV_{in}}{dt} \right)^2 dt} = \frac{\sqrt{2}}{2} \pi V_{FS} F_{in}$$

$$SNR = 20 \log \left(\frac{1}{2\pi F_{in} \tau} \right)$$

8 bits $\Rightarrow$ $SNR = (6N + 1.76)\,dB$

$\cong 50\,dB$

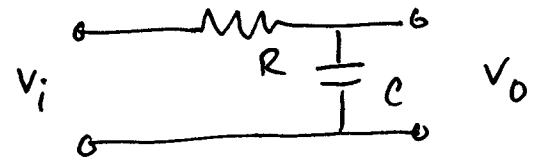
600 MS/s $\rightarrow$ $F_{in} = 300\,MHz$ $\longrightarrow$ $\tau = 1.68\,ps$

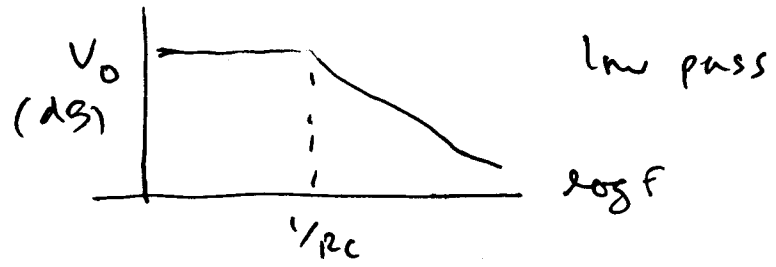
Thermal Noise.

channel/switch resistance

part of the speed-noise tradeoffs

$$\bar{V}_n^2 = 4kTR\Delta f$$





$$|V_o| = |V_{in}| \frac{1}{\sqrt{1+\omega^2 R^2 C^2}}$$

$V_i = \bar{V}_n$

Total noise power

$$N = \int_0^\infty |V_o|^2 df = \frac{kT}{C}$$

large C, low thermal noise floor

but lower speed.

Signal-to-Distortion Ratio. (SDR)

[Ref. Lim and Wooley, "A High Speed Sample and Hold Technique ...," J. Solid State Cir., Vol 26, #4, April 1991.]

input dependent sampling creates harmonic distortion. In the appendix to the above paper, the authors present some empirical results from simulations:

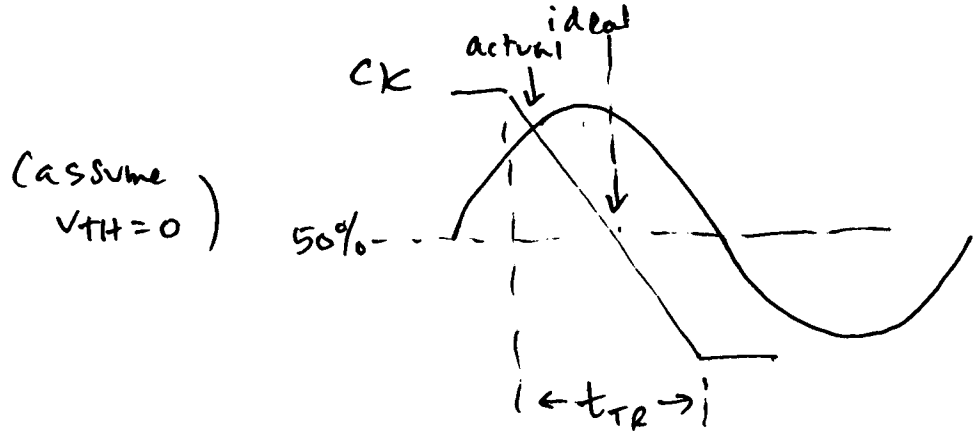
$$V_{out} = A \sin\left\{2\pi f_{in}\left[t - \frac{A}{V_{CL}} \cdot t_{TR} \cdot \sin 2\pi f_{in} t\right]\right\}$$

reconstructed signal (sine wave)

A = signal amplitude

V_{CL} = clock voltage amplitude

t_{TR} = clock transition time



$$SDR = 20 \log \left(\frac{V_{CK}}{t_{TR}} \right) \left(\frac{1}{A f_{IN}} \right) - 4$$

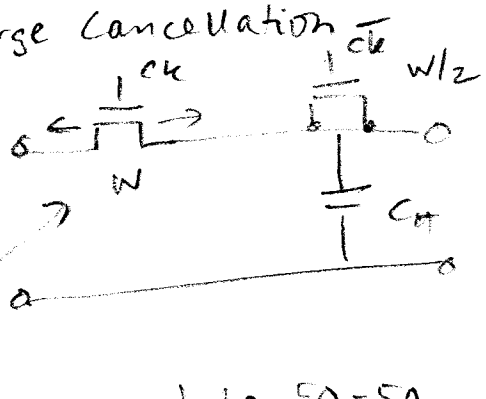
Clock slew rate

$\left(\text{Sig. slew rate} \right)^{-1}$

So SDR may be limited by input-dependent sampling

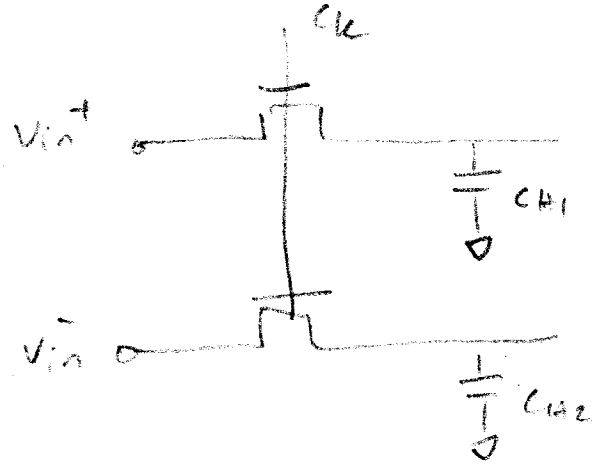
Charge injection offset error.

Charge cancellation



split may not be 50-50. Depends on source and load impedances. Some error remains

Differential version



charge injection shows up as CM offset

BUT

$V_{in}^+ > V_{in}^-$, so amount of charge injection is not equal.

a 6-b, 1.3 GSample/s A/D converter in 0.35μm CMOS

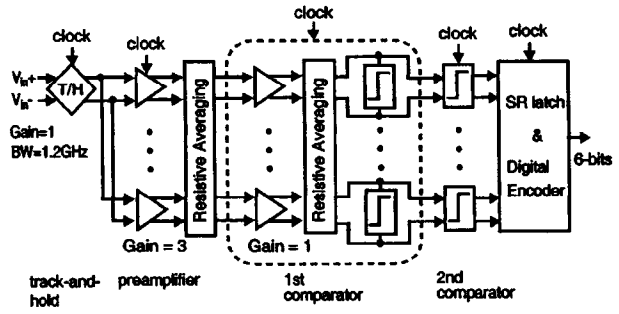


Fig. 2. Block diagram of 6-b flash A/D converter.

comparator. However, the preamplifiers in the array suffer from random offsets. Collective averaging of the preamplifier outputs across a properly designed resistor network lowers the impact of the offsets, improving accuracy of the threshold comparison without degrading bandwidth [13]. A comparator must quickly recover from large overdrive when the changing input voltage rapidly approaches the comparator's threshold from far away. To aid this, the gain of the comparator's input differential pair is about one, which widens its bandwidth. The resulting net amplification of 3 is not sufficient to overcome the dynamic random offsets in the regenerative latch for 6-b accuracy. Resistor averaging is also used within the comparators to lower the impact of offsets. Interpolation is not used in this work, because it degrades bandwidth [12], [13]. The second comparator array provides rail-to-rail logic swing for the digital back end consisting of the SR latch and ROM-based digital encoder.

III. Offset Averaging

A. Accuracy Improvement With Averaging Network

Fig. 3 shows a preamplifier array with averaging resistors $R1$ connecting adjacent output nodes. In this work, offset averaging is treated and optimized based on the concept of spatial filtering [13], [14]. The $R0$–$R1$ network forms a spatial filter with impulse response $h(n)$

$$h(n) = h(0) \cdot b^{|n|}, \qquad b = e^{-|\operatorname{acosh}(1+R1/2R0)|} \tag{1}$$

where n represents the index of differential pairs in the array. The ratio $R1/R0$ determines the width of the impulse response. An array of differential pairs injects two different types of stimuli currents in the averaging network. First, differential signal currents $\Delta I_s(n)$ limited by the linear region of the differential pair enter the network. Second, "noise" currents $\Delta I_{os}(n)$ due to transistor random mismatches also enter the averaging network. A well-designed averaging network should filter out the random currents, without losing valuable signal current, nor should the network lower bandwidth. Averaging is optimum when W_{ZX} (the number of differential pairs in the unclipped linear region of their characteristic) is greater than the impulse response width of the network W_{IR} [13].

Dummy preamplifiers are inserted to compare the input signals with thresholds beyond the actual full scale, so that the tails of the averaging network's impulse response remain undistorted at the ends of the full scale. A circular arrangement with sufficient dummy preamplifiers maintains translational symmetry of the array across the input full scale.

B. Speed Improvement With Averaging Network

It is by now well known that averaging improves accuracy. What is not as well appreciated, as explained below, is that averaging also improves speed.

The input random offset voltage is inversely proportional to the square root of the transistor gate area [15]. Therefore, preamplifier FET size may be related to the target ADC resolution as follows.

$$\sigma V_{os} \approx \frac{A}{\sqrt{(W \cdot L)_{\text{input}}}} \leq \frac{1}{4} \cdot \text{LSB}. \tag{2}$$

References [13], [14] show that the optimum averaging network lowers random offset by up to 3×, with a spatial impulse response W_{ZX} 18 nodes wide. With this network connected to the outputs of a preamplifier array, a given accuracy is maintained with 9× smaller FETs than if no averaging were used. The bandwidth as set by the output pole of this differential pair, shown in Fig. 4, is

$$\text{BW}_{\text{single}} = \frac{1}{R0 \cdot (C_{\text{wire}} + C_{\text{load}} + C_j)}. \tag{3}$$

With averaging, the wiring and junction capacitance are 9× lower due to transistor scaling (3× less gm). For the same bias current, the load resistance $R0$ must be 3× larger for equal voltage gain, which means that

$$\text{BW}_{\text{withavg}} = \frac{1}{3 \cdot R0 \cdot (C_{\text{wire}}/9 + C_{\text{load}} + C_j/9 + C_{\text{network}})} \tag{4}$$

where C_{network} is the parasitic capacitance of the averaging network. Comparing the two terms from (3) and (4)

$$\frac{\text{BW}_{\text{single}}}{\text{BW}_{\text{withavg}}} = 3 \cdot \left[1 + \frac{C_{\text{network}}}{C_{\text{wire}} + C_{\text{load}} + C_j} - \frac{8}{9} \cdot \left(\frac{C_{\text{wire}} + C_j}{C_{\text{wire}} + C_j + C_{\text{load}}}\right)\right] \approx \frac{1}{3}. \tag{5}$$

The second term in (5) is much less than 1, while the third term is close to 1. Therefore, use of the averaging network raises preamplifier bandwidth by 3×.

IV. Circuit Descriptions

A. Track-and-Hold

An input T/H improves the dynamic performance of an ADC. By holding the analog sample static during digitization, the T/H largely removes errors due to skews in clock delivery to a large number of comparators, limited input bandwidth prior to latch regeneration, signal-dependent dynamic nonlinearity, and aperture jitter [11]. The on-chip T/H circuit shown in Fig. 5 precedes the flash quantizer. This simple circuit, consisting of a passive nMOS switch connected to a sampling capacitor through a dummy switch [16], [17], offers just the required linearity. The dummy switch lowers the common-mode jump after the track-to-hold transition. The main sources of distortion

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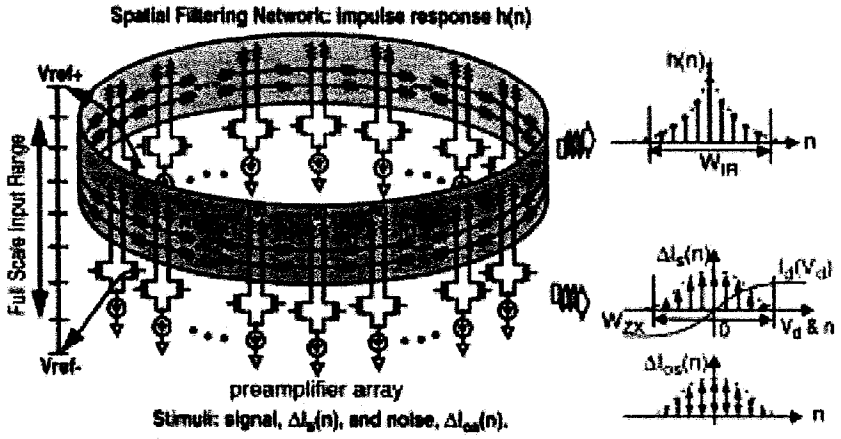


Fig. 3. Preamplifier array with resistor averaging network.

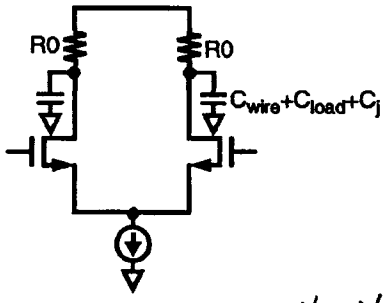


Fig. 4. Single differential amplifier.

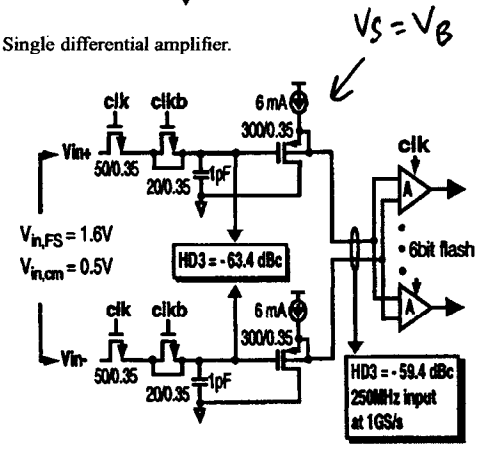


Fig. 5. On-chip track-and-hold.

are signal-dependent charge injection on switch opening, nonlinearity of the source follower, and dynamic current into the signal-dependent input capacitance of the quantizer.

FET charge injection and clock feedthrough cause distortion by adding/removing charge on the hold capacitor when the switch disconnects the signal source [18]. A dummy switch driven by the complement of the switch clock lowers these effects [19]. Because both the source and drain of the dummy switch are connected to the hold node, its W/L ratio is initially chosen as half the size of the switch, and then tuned through simulation. A low input common-mode voltage, 0.5 V, enables use of only nMOSFETs for the sampling and dummy switches. Unlike a complementary switch, nMOS (or pMOS)-only switches effectively cancel charge feedthrough, even with process variations.

Sample jitter due to the input-dependent switch opening is another distortion source and is described by the following output equations with a differential sine input.

$$V_{\text{out}} = V_{\text{outp}} - V_{\text{outn}} = 2 \cdot A \cdot \sin(2\pi ft) \cdot \cos\left(2\pi f \cdot \frac{A}{V_{\text{CL}}} \cdot t_{\text{TR}} \cdot \sin(2\pi ft)\right) \quad (6)$$

where V_{CL} is the maximum clock voltage, t_{TR} is the transition time of a clock edge, f is the input frequency, and A is the input amplitude [20]. For given V_{CL} (3.3 V), t_{TR} (0.15 ns), f (500 MHz), and A (0.4 V), the total harmonic distortion is -68 dB for the differential output, and -25 dB for the single-ended.

The low-input common-mode voltage of 0.5 V allows a larger gate overdrive to turn on the switch, which lowers track-mode distortion due to nonlinear channel resistance. The source is tied to the well in the pMOS source follower to eliminate nonlinear body effect. Simulations show that when acquiring samples of a 250-MHz full-scale sine wave at 1 Gsample/s, the T/H delivers samples to the quantizer input with third-harmonic distortion of about -60 dBc.

B. Preamplifier

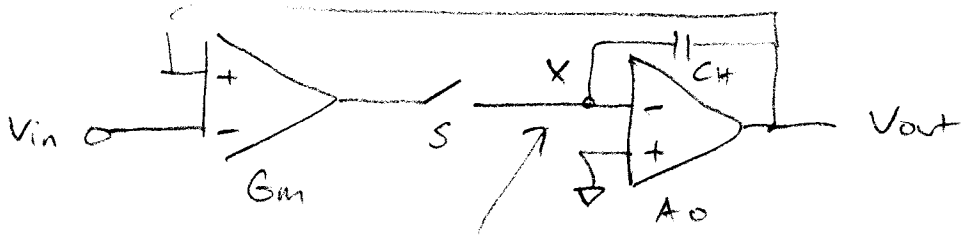
The preamplifier stage should be wideband and provide sufficient gain to overcome comparator offsets. It should also recover from large overdrive within one clock cycle. An open-loop low-gain-stage amplifier is gain-bandwidth limited, therefore unsuitable for use at high speeds because of poor overdrive recovery [6], [21]–[23].

The following analysis addresses the fundamental limitation of an open-loop single-pole amplifier stage in overdrive recovery and justifies quantitatively that an amplifier with a reset switch meets the speed requirement. Consider a simple one-stage single-pole amplifier, shown in Fig. 4. The preamplifier is completely unbalanced at $t = 0-$. With a step input applied to

- but, doesn't help charge injection since $V_{GS} - V_{th}$ isn't equal on both devices.
- But, resistance variation w/ V_{in} is reduced.
- Clock edge misalignment causes sampling instant shift that depends on V_{in}.

How are these errors addressed?

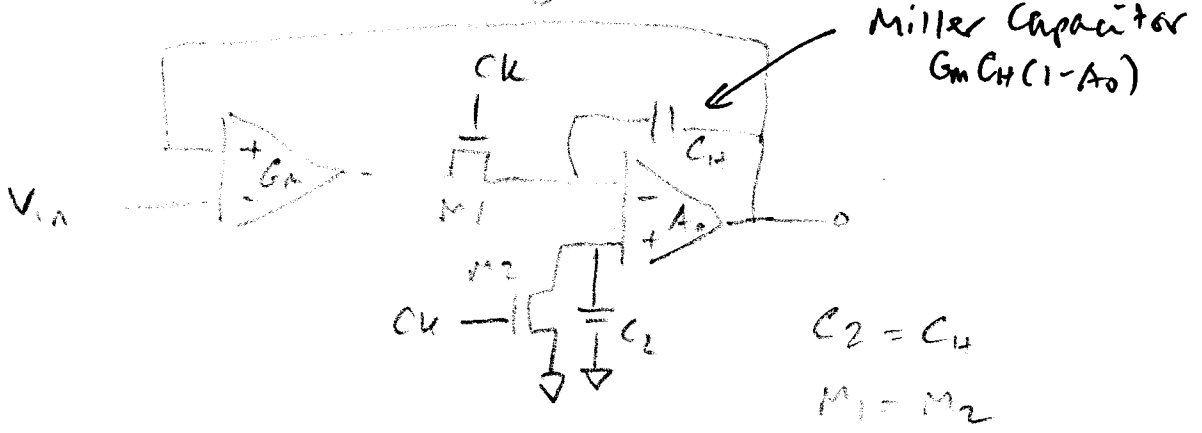
1. Closed Loop Architectures



virtual ground node. $V_X \cong 0$.
not input dependent.

- Feedback keeps Vout = Vin when S is closed.
- Holds Vout when open
- Constant Vx on S means no Vin dependent charge injection or pedestal error.
  offset is constant. No nonlinearity,

This can be modified to cancel offset (pedestal) and clock feedthrough

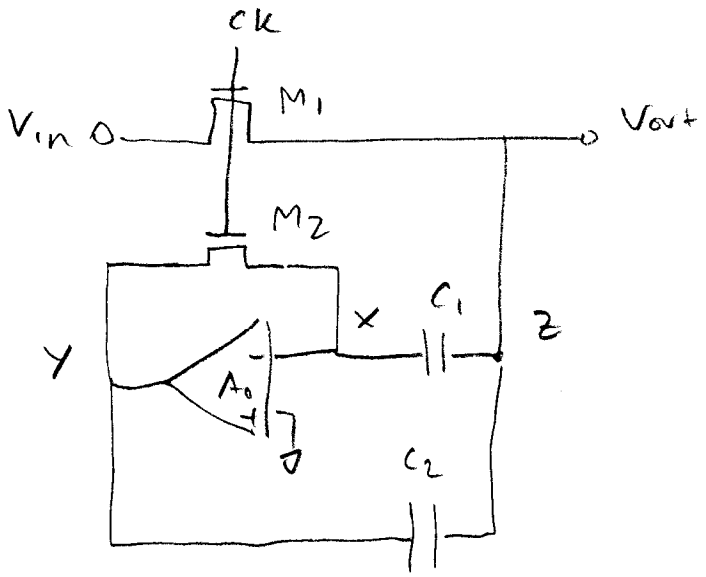


- Common mode cancellation

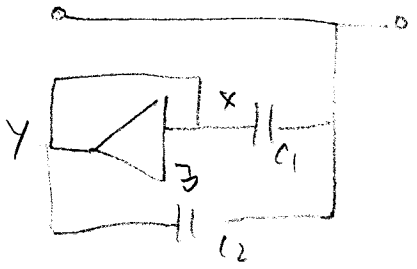
Problem: stability vs speed — tends to be slow.

- $G_m C_H (1-A_0)$ forms dominant pole
  can easily overcompensate.
- if undercompensate, then settling time is degraded

Pedestal error can also be reduced in an open-loop architecture by using separate sample and hold capacitors. Faster architecture.

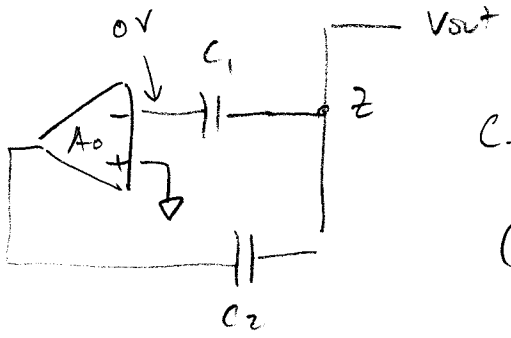


Track



in acq. mode, M_1 and M_2 are on. $V_x = V_y \overset{=0}{,}$ so C_1 and C_2 have the same charge. $V_{in} = V_{OUT}$.

Hold: M_1, M_2 off. Node z sees Miller multiplied capacitance C_2

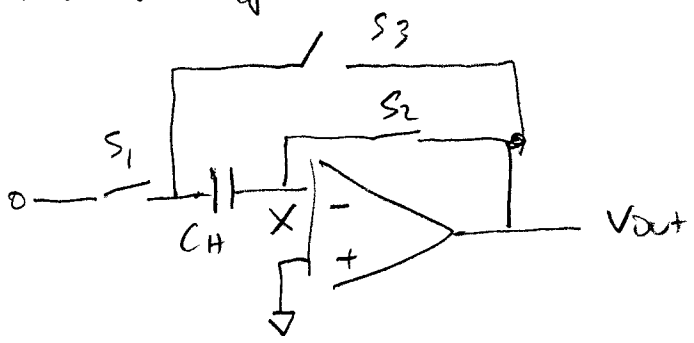


$$C_{eff} = \frac{A_0 C_2}{C_1 + C_2}$$

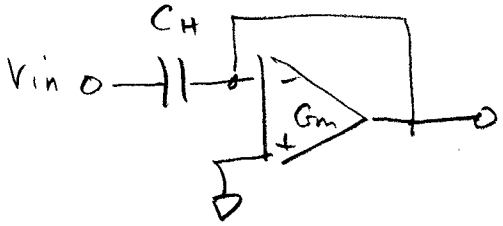
(cap. divider)

Node X and Y are at ground when enter hold, so no nonlinear charge injection.

Switched Cap S/H (no tracking)

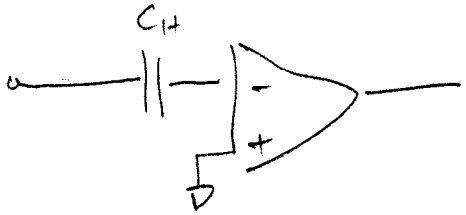


Sample: S_1, S_2 on. $V_X = 0 = V_{out}$



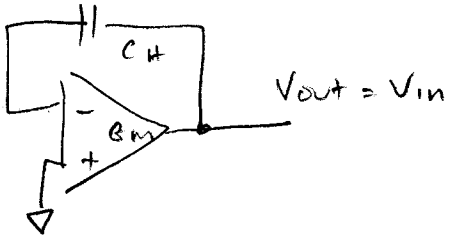
C_H is charged to V_{IN}

Hold: turn off S_2 first, C_H retains V_{in}



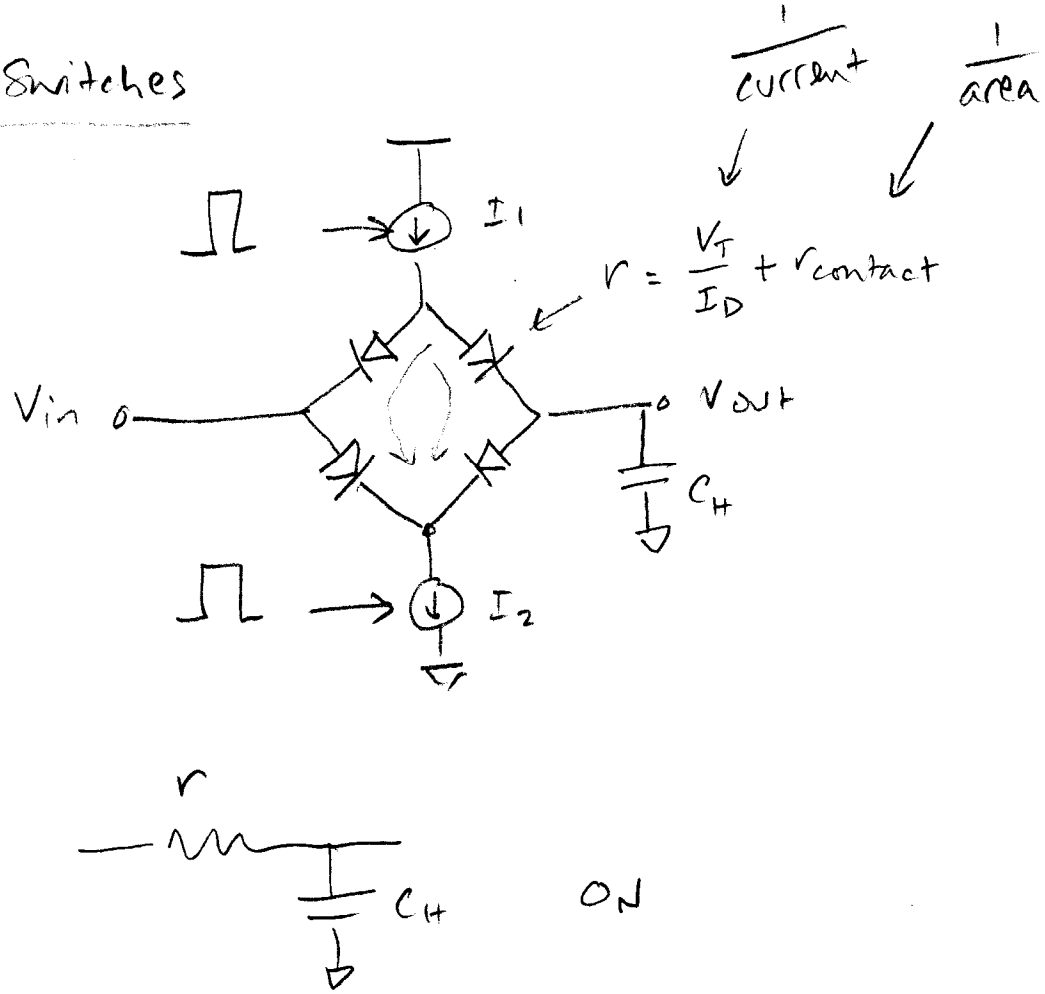
S_2 charge injection is not input dependent. in diff. config, CM.

next turn off S_1, and S_3 on.

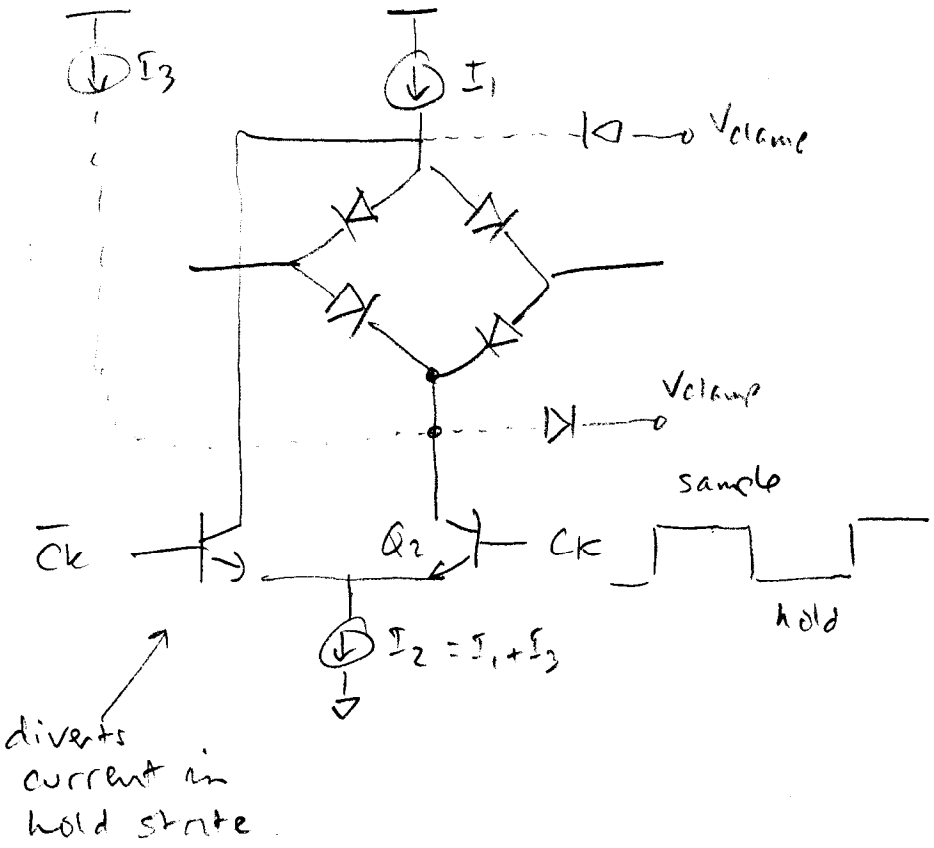


S_1 charge injection doesn't affect charge on C_H.

Diode Switches



Better implementation



V_{clamp} + D5, D6 prevents saturation of Q_2.

↑
mid input range

both off in sample
on in hold state.

Diode Bridge.

Sources of error.

1. signal dependent bridge current.
   no pnp current source

3. input dependent pedestal offset

2. on-resistance varies with V_{in}

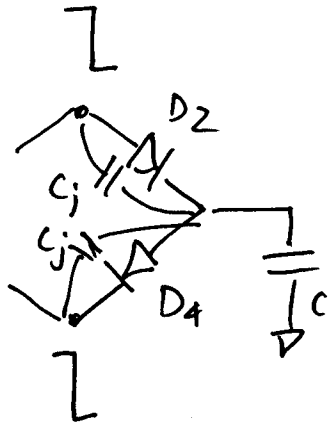
   C_H charges through D_2. Decreases r

   D_1, D_4 conduct less. Increases r

These changes must be small relative to on-resistance of switch.

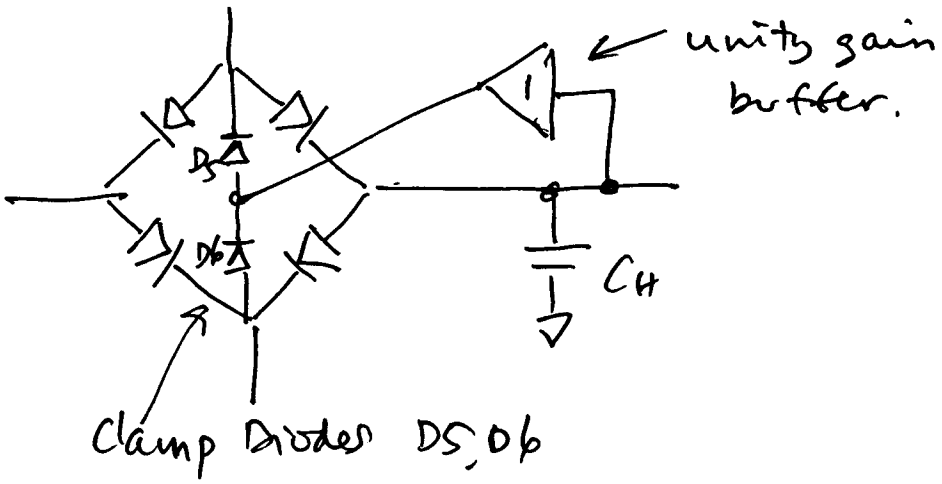
$$V_X = V_{in} + V_D \qquad \text{(track)}$$
$$V_Y = V_{in} - V_D$$

$$V_X = V_{B1} - V_D \qquad \text{(hold)}$$
$$V_Y = V_{B1} + V_D$$

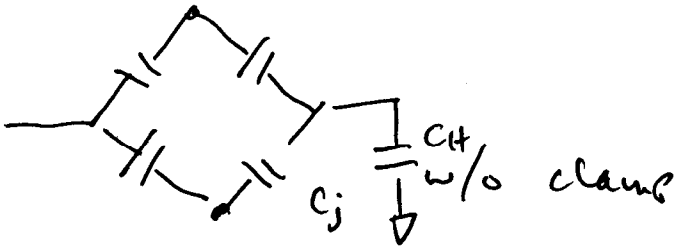


because junction capacitance of D_2, D_4 depends on voltage, pedestal has nonlinear term.

Compensate by tracking V_{B1} with Vout.



4. Hold-mode feedthru.



with clamp - less feedthru but depends on R_{on}.

An 8-Bit 2-Gsample/s Folding-Interpolating Analog-to-Digital Converter in SiGe Technology

Farhang Vessal, *Student Member, IEEE,* and C. Andre T. Salama, *Fellow, IEEE*

***Abstract*—This paper deals with the design and implementation of an 8-bit 2-Gsample/s folding-interpolating analog-to-digital converter (ADC) using a SiGe technology with a unity gain cutoff frequency f_T of 47 GHz. The high-speed high-resolution ADC has applications in direct IF sampling receivers for wideband communication systems. The converter occupies an area of 3.5 mm × 3.5 mm including pads and exhibits an effective resolution bandwidth of 700 MHz at a sampling rate of 2 Gsample/s. The maximum DNL and INL are 0.5 and 1 LSB, respectively. The ADC dissipates 3.5 W (including output buffers) from a 3.3-V power supply.**

***Index Terms*—Analog-to-digital converter (ADC), folding-interpolating, heterojunction bipolar transistor (HBT).**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are widely used in modern communication systems to interface analog waveforms with digital signal processing (DSP) circuitry. By moving the ADC closer to the system front-end, the majority of the processing can be performed in the digital domain. To take advantage of the increasing speed and sophistication of digital signal processing, the ADC must operate at high sampling rates and low voltages, and remain immune to a noisy digital environment. This brief describes the design and implementation of an 8-bit 2-Gsample/s ADC with an on-chip track-and-hold amplifier (THA) using a SiGe heterojunction bipolar transistor (HBT) technology with a f_T of 47 GHz. Compared to conventional bipolar junction transistors (BJTs), SiGe HBTs have improved high-frequency behavior and low base resistance.

II. Block Diagram

The block diagram of a folding-interpolating architecture is illustrated in Fig. 1. The output of the track-and-hold circuit is applied to the input of four folding amplifiers where it is compared to reference voltages generated by a resistor ladder. The output of the folding amplifiers is a set of phase-shifted sinusoid-like signals which are, in turn, applied to an array of comparators. The outputs of the comparators are the representation of the input signal in thermometer codes. These codes are eventually converted back to binary codes by a digital encoder to produce the six least significant bits (LSBs). The two most significant bits (MSBs) are produced by a coarse quantizer. The folding-interpolating architecture is very suitable for high-resolution converters that require a large analog bandwidth.

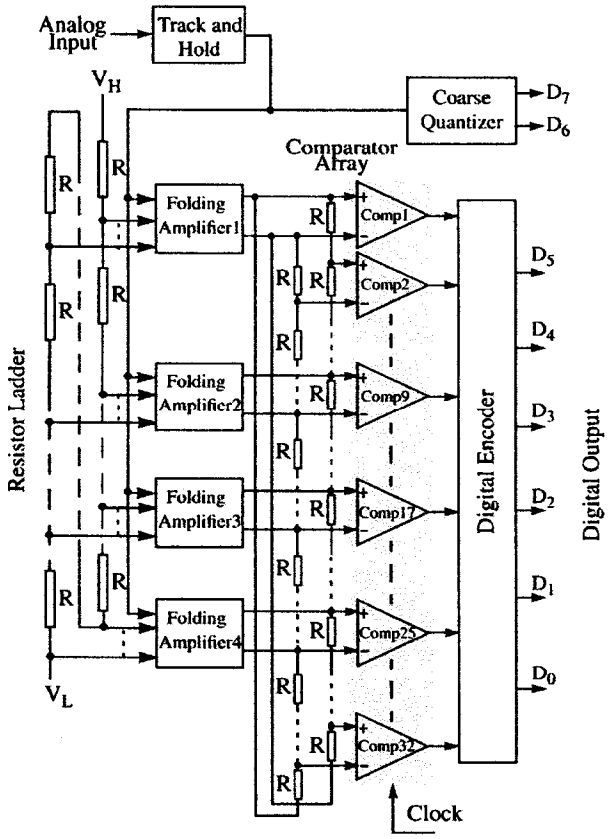


Fig. 1. Block diagram of the folding-interpolating ADC.

A. Track-and-Hold Amplifier

The THA at the front-end of the converter performs the time sampling of the input signal. A simplified circuit diagram of the THA circuit is given in Fig. 2 [1], [2]. It consists of an input buffer, sampling switches, and output buffers. The differential input buffer consists of a differential pair Q_1 and Q_2 with degenerative feedback (R_1, R_2), loaded with resistors R_3 and R_4. The differential input signals are applied to the bases of the transistors Q_1 and Q_2. The differential output of the input buffer go to the track-and-hold switches. Each track-and-hold switch consists of three transistors (Q_3, Q_4, Q_5), a current source (I_2) and a holding capacitor (C_H). There is a compromise between the droop rate and the bandwidth of the THA in choosing the proper value for C_H. Lowering the value of C_H increases the bandwidth but deteriorates the droop rate. In this work, a value

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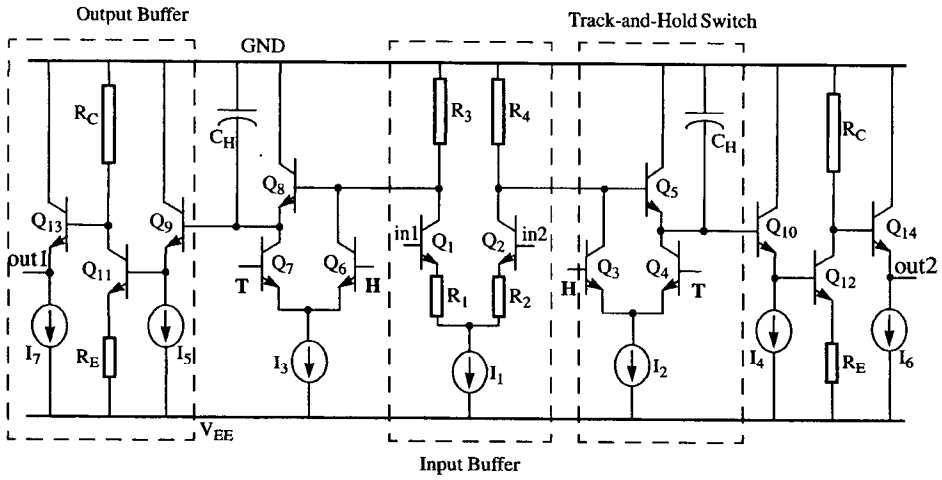

Fig. 2. THA circuit.

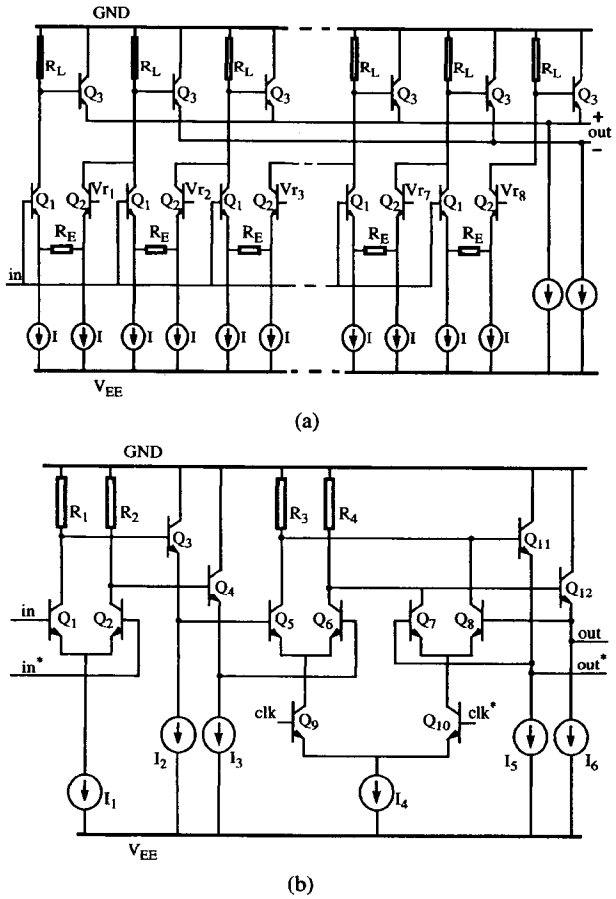

Fig. 3. (a) Folding amplifier circuit. (b) Comparator circuit.

of 0.9 pF was chosen for C_H to get an analog bandwidth of at least 4 GHz and a droop rate of 10 mV/ns.

B. Folding Amplifier

The topology of the folding amplifier used in this implementation is shown in Fig. 3(a). The basic function performed by the folding amplifiers is the conversion of the increasing (or decreasing) input signal into a number of sinusoid-like output signals [1]. Each folding amplifier generates eight zero-crossings, equidistantly spaced over the input range. Four folding amplifiers are used in parallel, generating the required 32 zero-crossings. To ensure that the ADC achieves the required 8-bit resolution, accurate zero-crossing points must be generated by the folding circuits. In order to reduce the mismatch between Q_1 and Q_2 in each differential pair, these transistors should be large enough, but increasing the size of these transistors affects the loading capacitance of the previous stage (THA) in the system; therefore, a compromise must be considered in choosing the size of Q_1 and Q_2 during the design of this stage. In this design, the size of these transistors was chosen to be $0.5 \times 5\ \mu m^2$. Biasing conditions are a tradeoff between bandwidth and power consumption. The bandwidth of the circuit is inversely proportional to the value of R_L. A large R_L leads to a serious analog bandwidth limitation. In addition, the shape of the sinusoid-like waveforms must exhibit high linearity around the zero-crossing points because linear interpolation between two adjacent folding signals is necessary. The interpolation is implemented using a resistive string because of its simplicity and power efficiency. In this design, differential interpolation is implemented by applying the differential outputs of the folding amplifiers to the differential resistive strings. This differential implementation improves the accuracy of the converter.

C. Comparator

The comparators consist of a two-stage preamplifier (Q_1–Q_4) and a latch (Q_5–Q_{10}), as illustrated in Fig. 3(b). Such a comparator architecture reduces the kickback noise to an acceptably low level and provides a relatively high gain, which in turn lowers the offset contributed by the latch and improves the metastability behavior of the comparator. Transistors Q_5 and Q_6 form a tracking differential pair (track pair) that produces a differential voltage across resistors R_3 and R_4. A second differential pair, Q_7 and Q_8 (latch pair), connected in a positive-feedback configuration, latches the differential signal. To reduce