Lec. 4

April 6, 2005

DA Converters

Read Ch 4,5

Digital to Analog Converters

Analog output is linearly proportional to a digital input. (ideal DAC)

$$A = REF \cdot \frac{D}{2^m}$$

↑ voltage or current reference

differential nonlinearity (DNL) error

For an ADC, DNL error is defined as the difference between the ideal and the measured code transitions for successive codes. An ideal ADC would have finite digital codes exactly 1LSB apart (DNL = 0). For a DAC, DNL error is the difference between the ideal and the measured output value between successive DAC codes. An ideal DAC would have analog output values exactly one code apart (DNL = 0). A DNL specification of greater than or equal to 1LSB guarantees monotonicity (see monotonic).

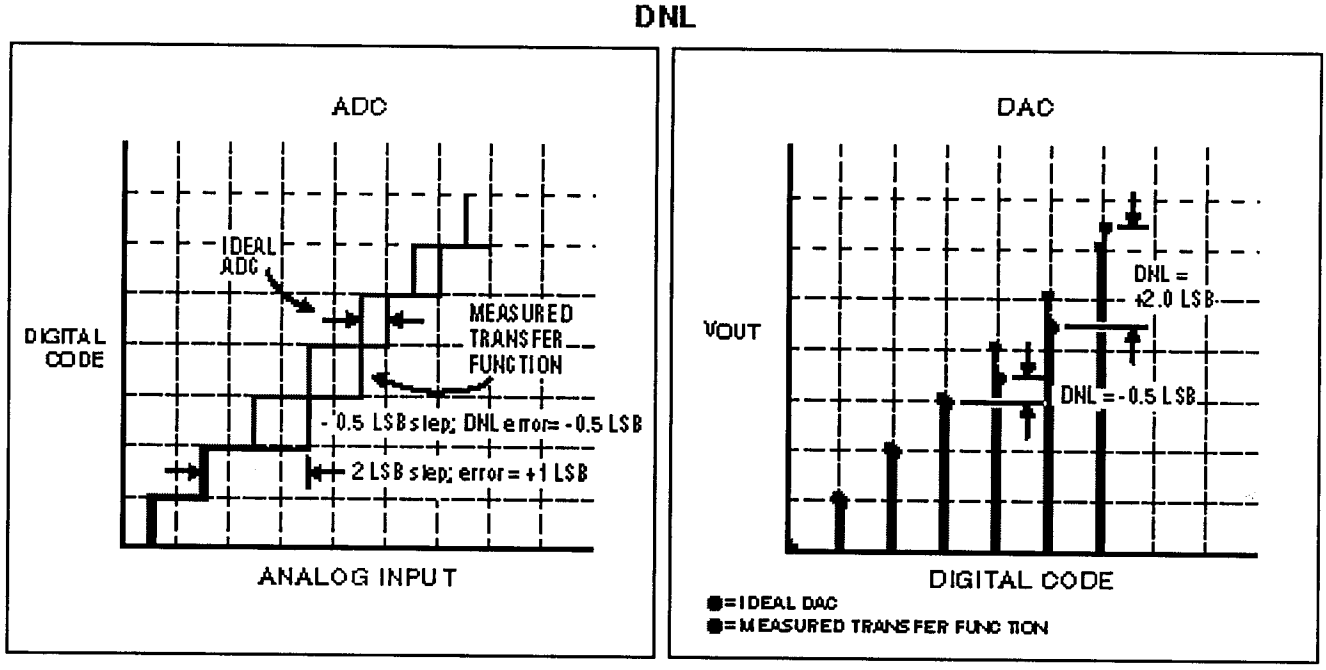


Figure 2. DNL for a) ADC and b) DAC [Maxim. AN641]

See also application note *INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs)* [Maxim AN283] ↗

Monotonic. For DAC, the output must always increase as the digital input code increases. (DNL > −1 LSB)

integral nonlinearity (INL) error

INL is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-fit straight line or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. "Relative accuracy" is a term often used to refer to INL. Maxim typically uses the end-point method when specifying INL for data converters. The end-point method is the more conservative of the two methods and is typically 2x better than the best-fit straight line method.

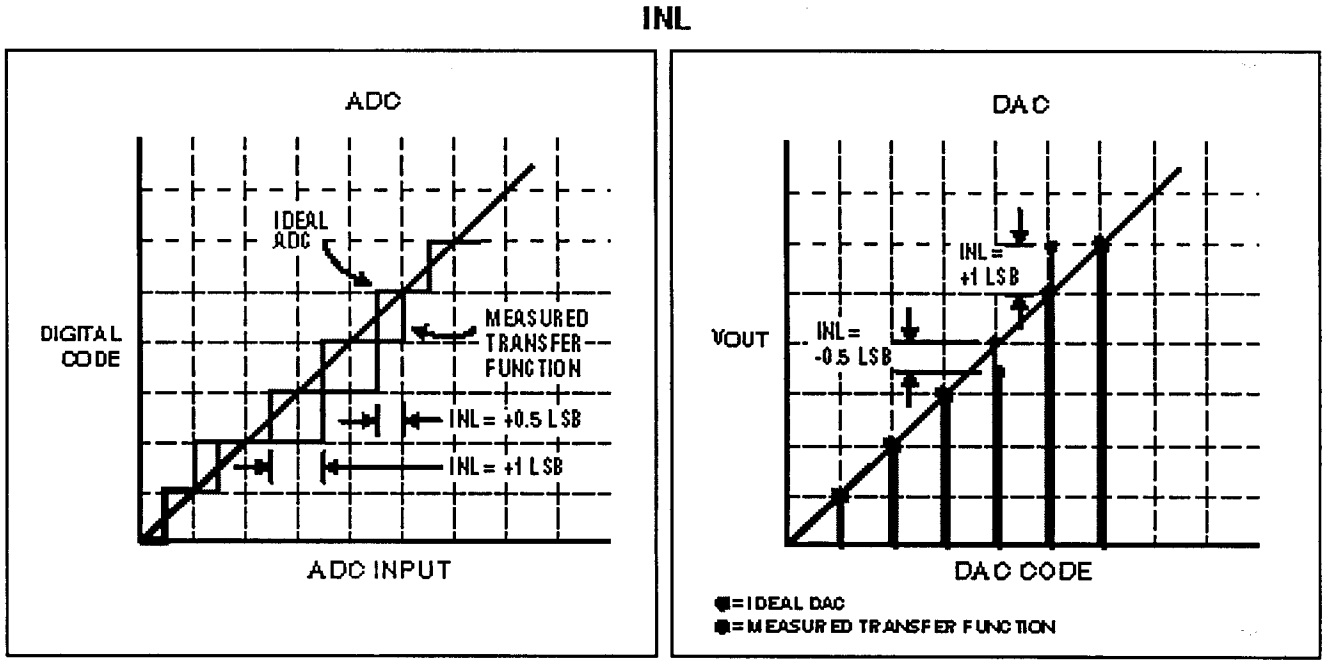
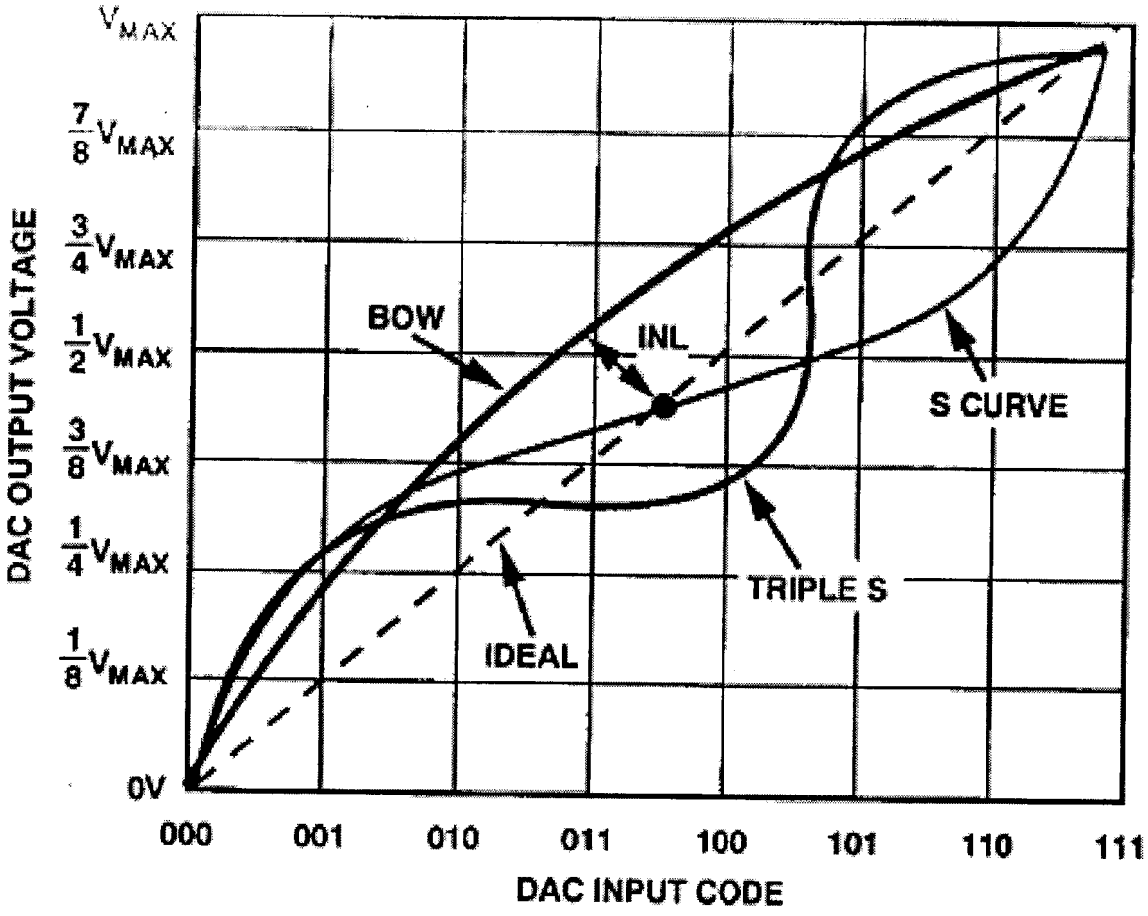


Figure 6. INL for a) ADC and b) DAC [Maxim AN641]

All curves have same INL



Bow: 2nd order HD/IMD
S: 3rd order HD/IMD

Figure 8. INL Curves—All 1 LSB

Analog Devices AN-237

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or a percent of full-scale range (%FSR). It can be calibrated out with hardware or in software.

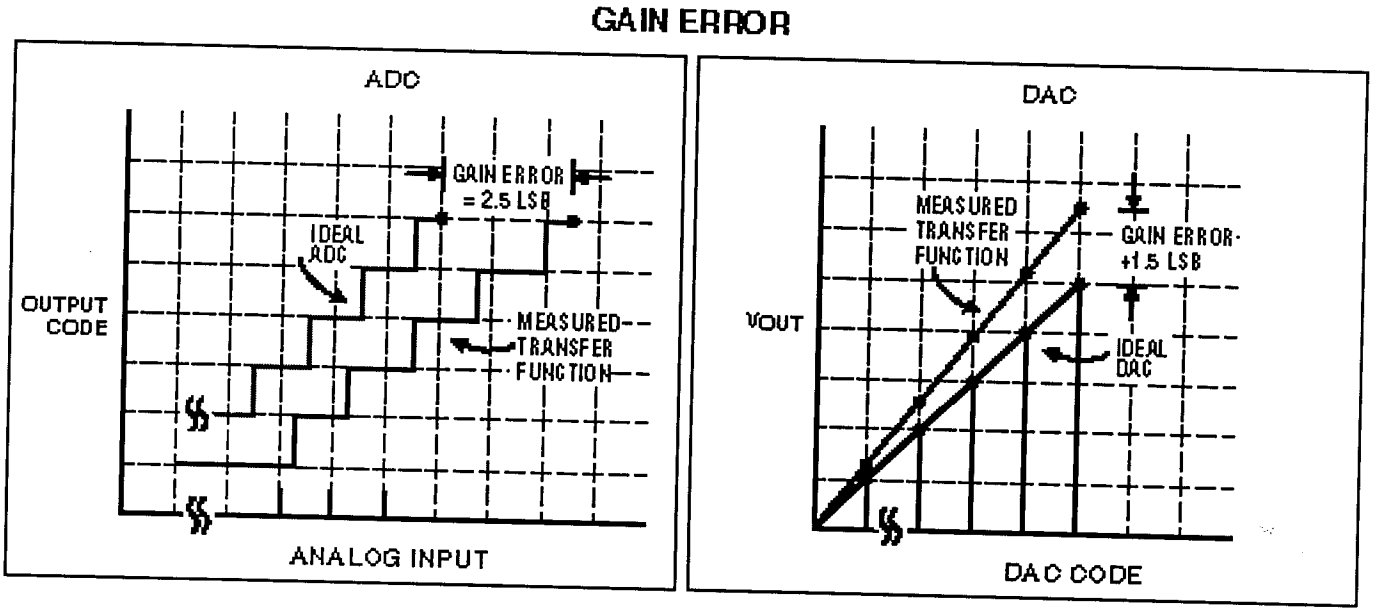


Figure 5. Gain Error for a) ADC and b)DAC [Maxim AN641]

Settling Time. For DAC, output reaches its final value within $\pm \frac{1}{2}$ LSB during its settling time.

O

[Maxim AN641]

offset binary coding
Offset binary is a coding scheme often used for bipolar signals. In offset binary coding, the most negative value (negative full-scale) is represented by all zeros (00...000) and the most postive value (positive full-scale) is represented by all ones (11...111). Zero-scale is represented by a one (MSB) followed by all zeros (10...000). This is similar to straight binary, which is typically used for unipolar signals.

offset error (bipolar)
Offset error in bipolar converters is measured similarly to the offset error in unipolar converters. However, the error measured at zero-scale is at the midpoint of the bipolar transfer functions. See offset error (unipolar).

offset error (unipolar)
Offset error, often called "zero-scale" error, is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal data converter, the first transition occurs at 1/2 LSB above zero. For an ADC, the zero-scale voltage is applied to the analog input and is increased until the first transition occurs. For a DAC, loading a code of all zeros into the DAC and measuring the analog output voltage determine the offset error.

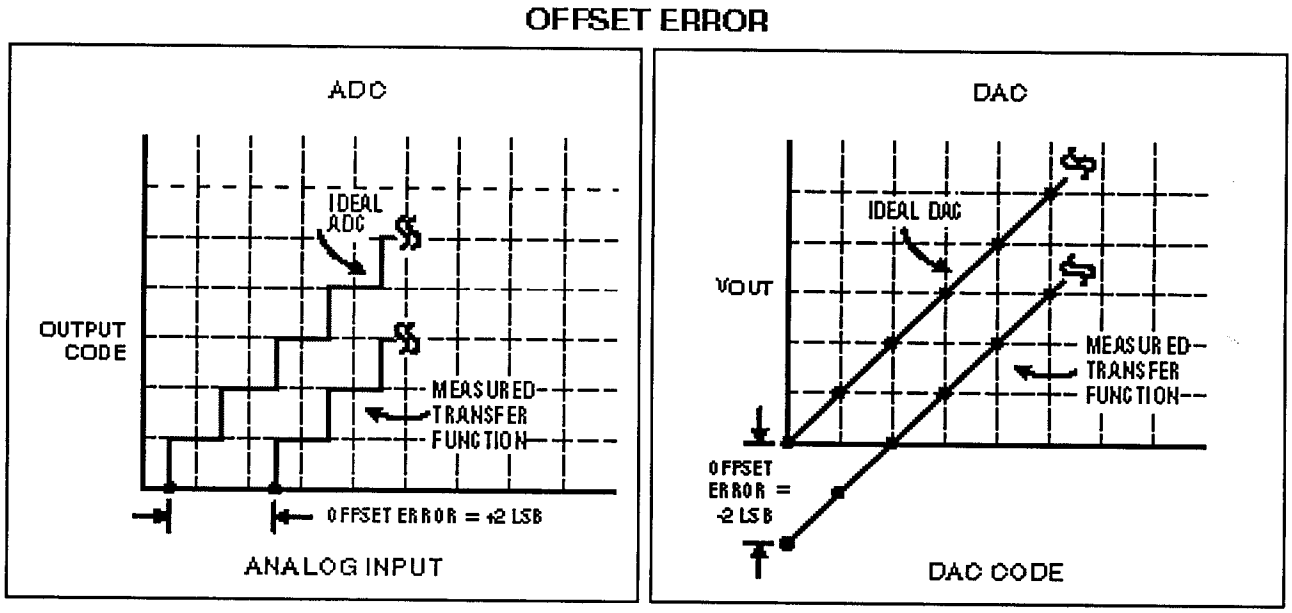
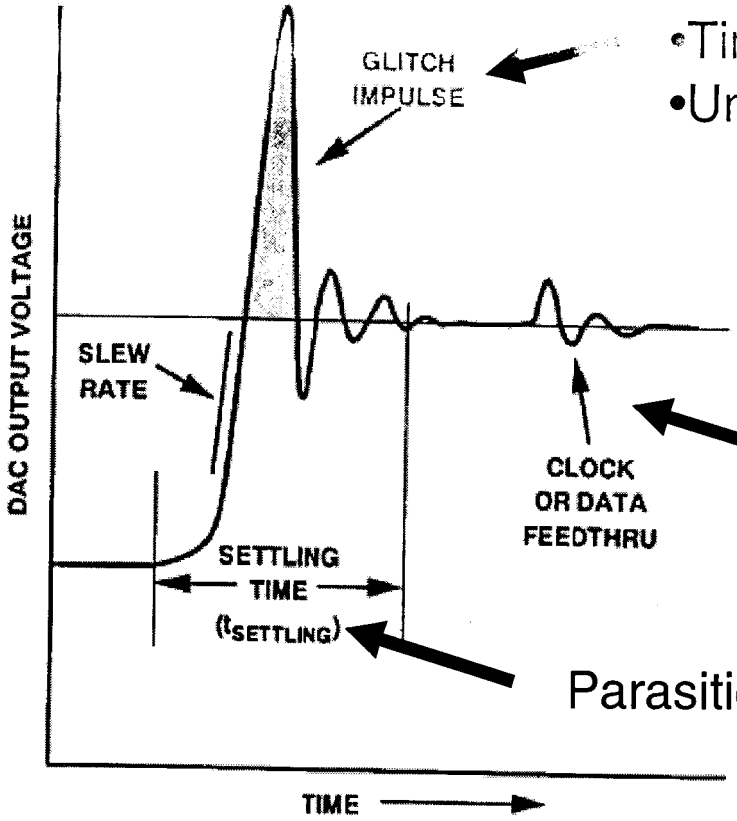


Figure 7. Offset Error for a) ADC and b) DAC

offset error drift
Offset error drift is the variation in offset error due a change in ambient temperature. This is typically expressed in ppm/° C.

Transient Response



- Time skew between data bits
- Underdamped amplifier
- Substrate coupling
- PC board layout
- Parasitic capacitance

Figure 9. DAC Transition

Analog Devices AN-237

Sources for SFDR limitations in DAC

1) *Code-dependent settling time constants:* The time constants of the MSB's, ULSB's, and LLSB's are typically not proportional to the currents switched.

2) *Code-dependent switch feedthrough:* Due to signal feedthrough across switches that are not sized proportionally to the currents they are carrying, and therefore shows up as code-dependent glitches at the output.

3) *Timing skew between current sources:* Imperfect synchronization of the control signals of the switching transistors will cause dynamic nonlinearities. Synchronization problems occur because of both delays across the die and improperly matched switch drivers. Thermometer decoding can make the time skew worse because of the larger number of segments.

4) *Major carry glitch:* This can be minimized by thermometer decoding, but in higher resolution designs where full thermometer decoding is not practical, it cannot be entirely eliminated .

5) *Current source switching:* Voltage fluctuations occur at the internal switching node at the sources of the switching devices; since the size of the fluctuation is not proportional to the current's being switched, it again gives rise to a nonlinearity.

6) *On-chip passive analog components:* Drain/source junction capacitances are nonlinear; on-chip analog resistors also exhibit nonlinear voltage transfer characteristics. These devices therefore cause dynamic nonlinearities when they occur in analog signal paths.

7) *Mismatch considerations:* Device mismatch is usually considered in discussions of static linearity, but it also contributes to dynamic nonlinearity because switching behavior is dependent on switch transistor parameters ... These differ for devices at different points on the die, introducing code dependencies in the switching transients.

[2] Bugeja

General observations. Freq. domain

1. Higher slew rate is better. So is ~~fast~~ settling time.
   closer to ideal transition

2. Rising and Falling time differences creates harmonic distortion

3. Minimize glitch area. Time skews cause DAC output to approach intermediate state. Adds unwanted energy to spectrum.

4. Layout is important.

5. DAC performance improves as $f_a << f_c/2$.
   ac artifacts become smaller fraction of each clock cycle.

6. Avoid integer ratios of f_c/f_a.
   aliasing will be concentrated near the desired output.
   $(Af_a \pm Bf_c)$

Lec. 5

DA Converters

April 11, 2005

Read Ch 4, 5

HW 2 Due 4/18

With the performance metrics in mind, now let's look at some of the DAC design details.

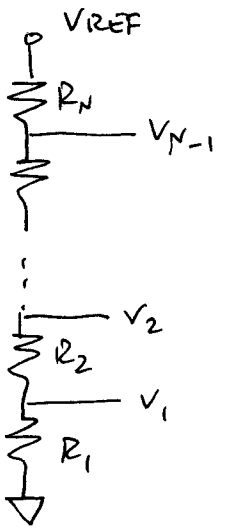
- Reference division
- Current switch
- RZ vs NRZ output

Read:

Razavi Ch 4, 5

To generate an analog output from a digital input code, some kind of voltage, current, or charge division is necessary. Then, switches can add or remove quantities as controlled by the input.

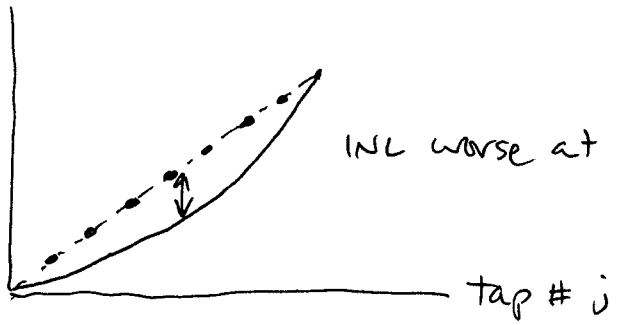
Ex. Voltage division:



m-bits $\Rightarrow$ 2^m identical resistors

variations of resistance create INL and DNL.

example: linear gradient in R : add ΔR to each R_j



$$V_j = \frac{j R + \frac{j(j-1)}{2} \Delta R}{NR + \frac{N(N-1)}{2} \Delta R} V_{REF}$$

ideally $V_j = \frac{j}{N} V_{REF}$

Note that we can get nonlinearity from this otherwise linear network because we are selecting taps with a switch.

other sources of error:

$$R = \frac{\rho L}{Wt} + 2R_c$$

linewidth variation can cause W, L to vary $\Delta W, \Delta L$
doping or resistivity nonuniformity : $\Delta\rho, t$
contact resistance : random interface resistivity.

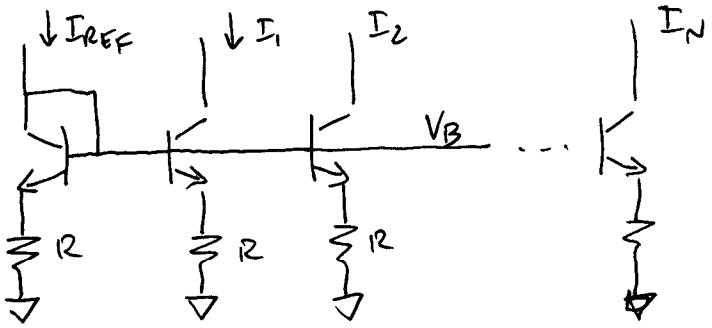
These effects are random : Gaussian distribution

make L, W large. R large compared with R_c.

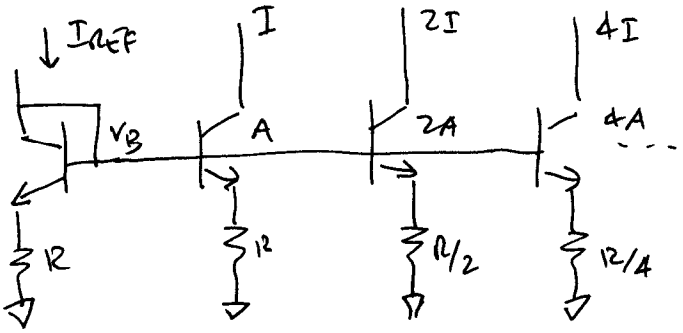
tradeoff area, speed for accuracy.

Finally, for a high accuracy DAC, 2^m resistors can be a very large number.

Ex. current replication



thermometer code (segmented) array always monotonic.

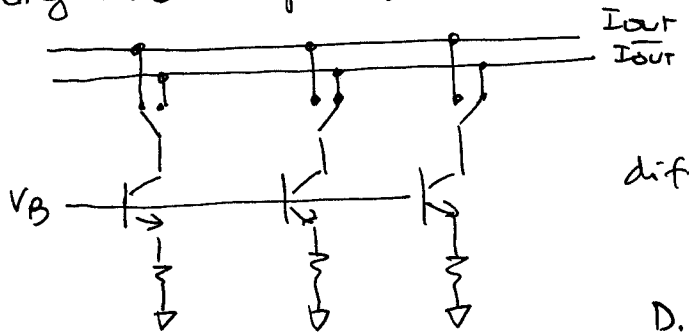


binary array & code

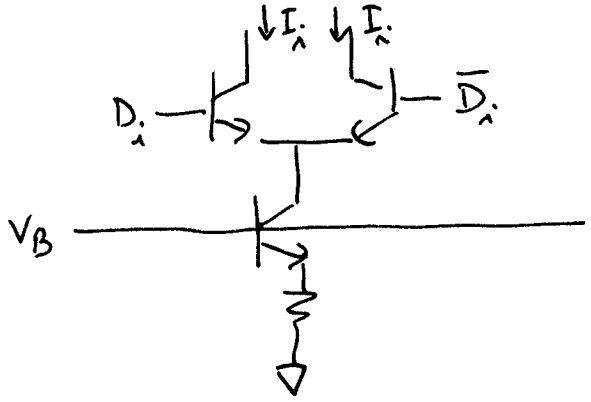
accuracy depends on current source mismatch.

The binary array MSB error can be > 1 LSB

Switching and outputs:



differential switches



Current Mismatch Error.

From Gray and Meyer:

$$\frac{\Delta I}{I} \approx \frac{1}{1+\frac{g_m R_E}{\alpha}} \frac{\Delta I_S}{I_S} + \frac{g_m R_E}{\alpha + g_m R_E}\left(\frac{\Delta \alpha}{\alpha} - \frac{\Delta R_E}{R_E}\right)$$

1. $R_E \ll \frac{1}{g_m}$. Then mismatch is dominated by ΔI_S:

$$\frac{\Delta I}{I} \approx \frac{\Delta I_S}{I_S}$$

geometry matching. Requires large transistors

5-10% for small devices.

2. $R_E \gg \frac{1}{g_m}$

$$\frac{\Delta I}{I} \approx \frac{\Delta \alpha}{\alpha} - \frac{\Delta R_E}{R_E}$$

$\uparrow$ 0.001 $\nearrow$

large R_E also suppresses emitter contact mismatch.

For MOS Current Mirrors

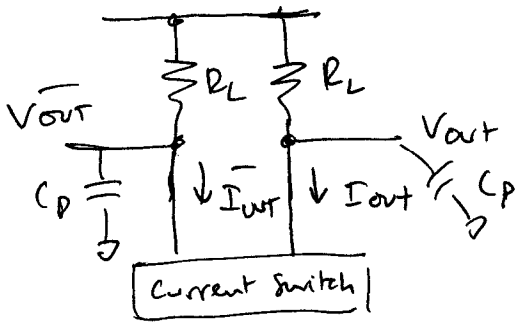
$$\frac{\Delta I_D}{I_D} = \frac{\Delta(C_{ox} v_{sat})}{C_{ox} v_{sat}} + \frac{\Delta W}{W} - \frac{\Delta V_{Th}}{V_{GS} - V_{Th}}$$

clearly gets worse for small widths and highly scaled devices.

Source degeneration is not as effective since g_m is smaller for MOS

$g_m R_S >> 1$ to be of use,

Then, may lose too much headroom.



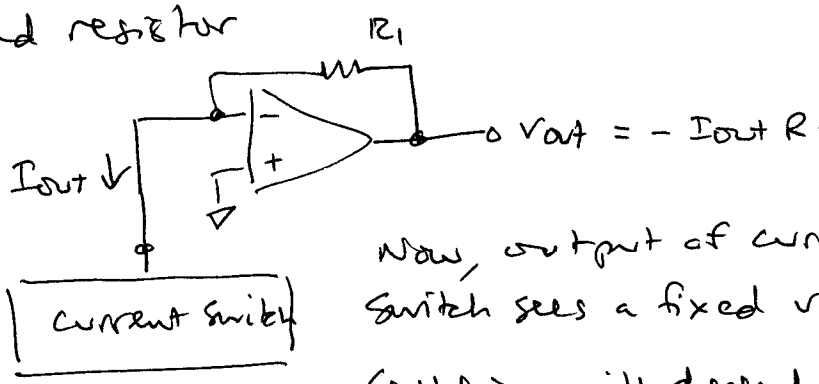
R_L can be 50 Ω off-chip but requires large currents 20mA / Volt.

Settling speed depends on $R_L C_p$

C_p = parasitic capacitance due to wiring, components.

output experiences entire voltage swing.

a transimpedance amp could be used instead of the load resistor

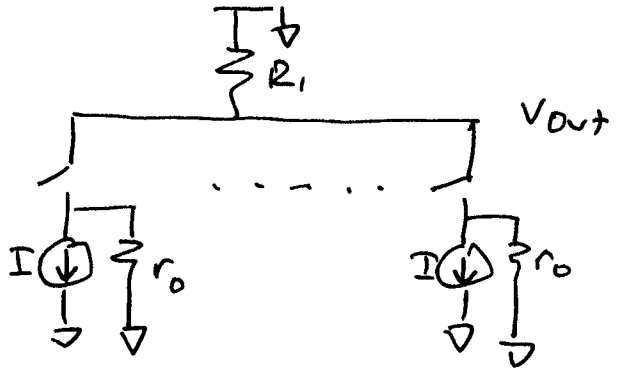


Now, output of current switch sees a fixed voltage.

Settling will depend on the amplifier.

The output impedance of the current source is a source of error for this type of DAC.

If you have an array of 2^N current sources of equal width (N-bit segmented) driven by a thermometer code:



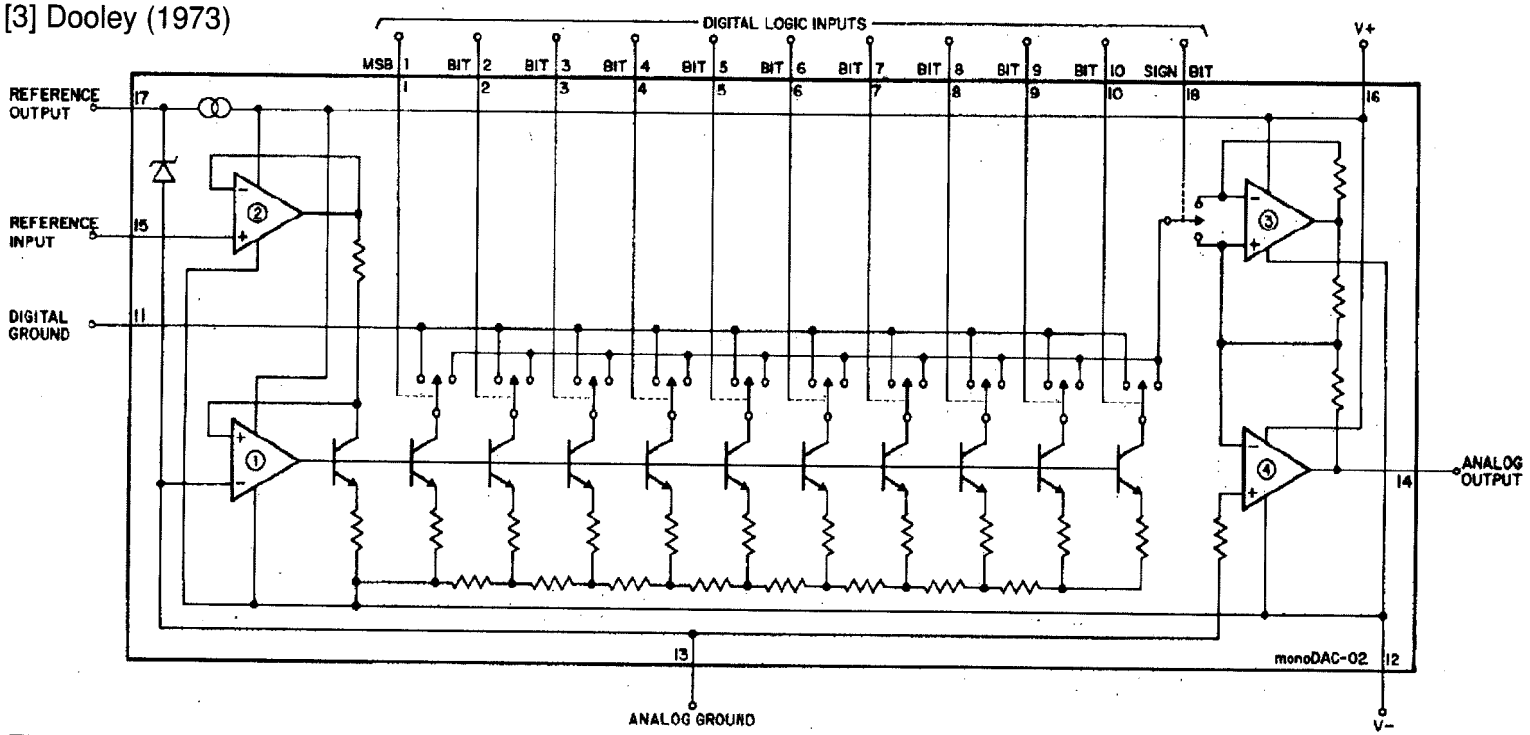
$$V_{out} = -nI\left(R_1 \| \frac{r_o}{n}\right) \qquad \text{where } 0 \le n \le N$$

This produces integral nonlinearity.

maximum of $IR_1^2N^2/4r_o$

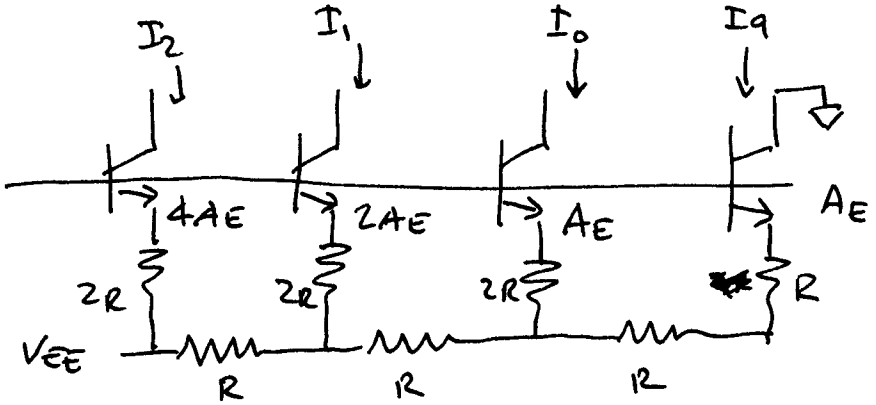
Current-scaling DAC

[3] Dooley (1973)



- Early attempt to achieve high-resolution monolithic DAC using binary current scaling
- (+) Complexity
- (+) Large current mismatch due to non-equal current densities through current sources. To overcome this problem, large transistor-scaling is necessary.

Current Steering. R-2R Ladder: Emitter

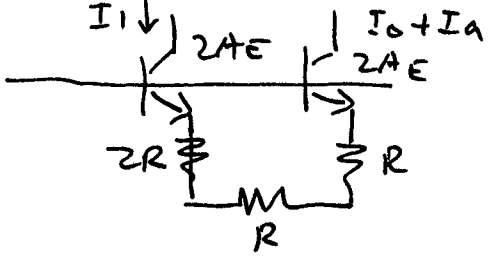


R-2R ladder scales emitter currents – binary weight
Device areas must also be scaled in proportion to current to keep V_{BE} the same.

For large # bits, the voltage drop can become quite small across LSB emitter resistor.
This is bad, because $2I_E R >> \Delta V_{BE}$ to maintain accuracy. If R is large, then physical area of resistors becomes large.

How it works.

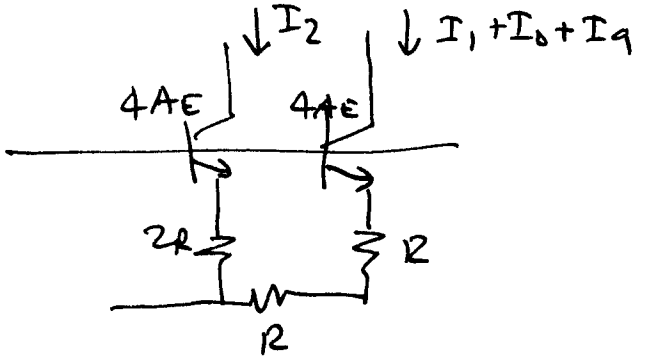
1. $I_0 = I_a$: Same A_E, R_E
2. Replace with single device: $2A_E$



These now have equal currents

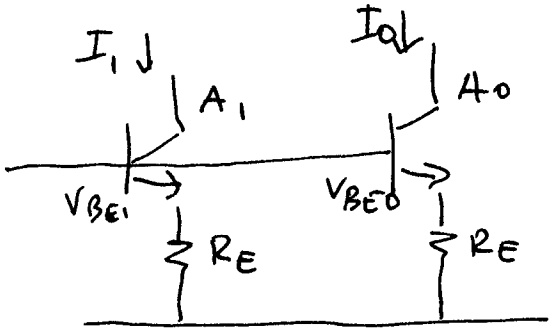
$$I_1 = I_0 + I_a = 2I_a$$

3. Continue to replace with $4A_E$ device



as we continue up the ladder, we see each step produces binary weighting.

Why emitter areas must be scaled:



$$I_0 = I_{S0} \exp\left(\frac{qV_{BE}}{kT}\right)$$

$$\left(\frac{kT}{q} = V_T\right)$$

neglect α.

$$I_1 R_E + V_{BE1} - V_{BE0} - I_0 R_E = 0$$

$I_1 = I_0$ only if $V_{BE1} = V_{BE0}$

$$V_{BE_i} = V_T \ln\left(\frac{I_i}{I_{S_i}}\right)$$

$I_S \propto A_E$

$$V_{BE_1} - V_{BE_0} = V_T \ln \frac{I_1}{I_{S_1}} - V_T \ln \frac{I_0}{I_{S_0}}$$

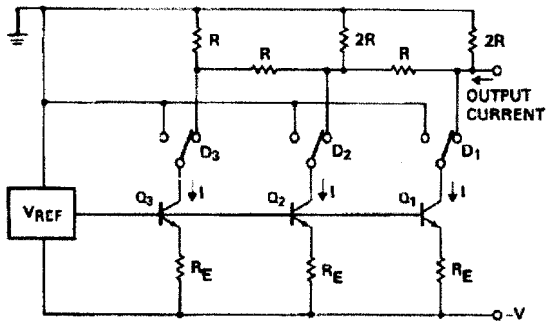
$$= V_T \ln \left(\frac{I_1}{I_0} \cdot \frac{I_{S_0}}{I_{S_1}} \right)$$

So, unless $A_{E_1} = A_{E_0}$, I_1 cannot be equal to I_0.

R-2R Attenuator — a better approach.

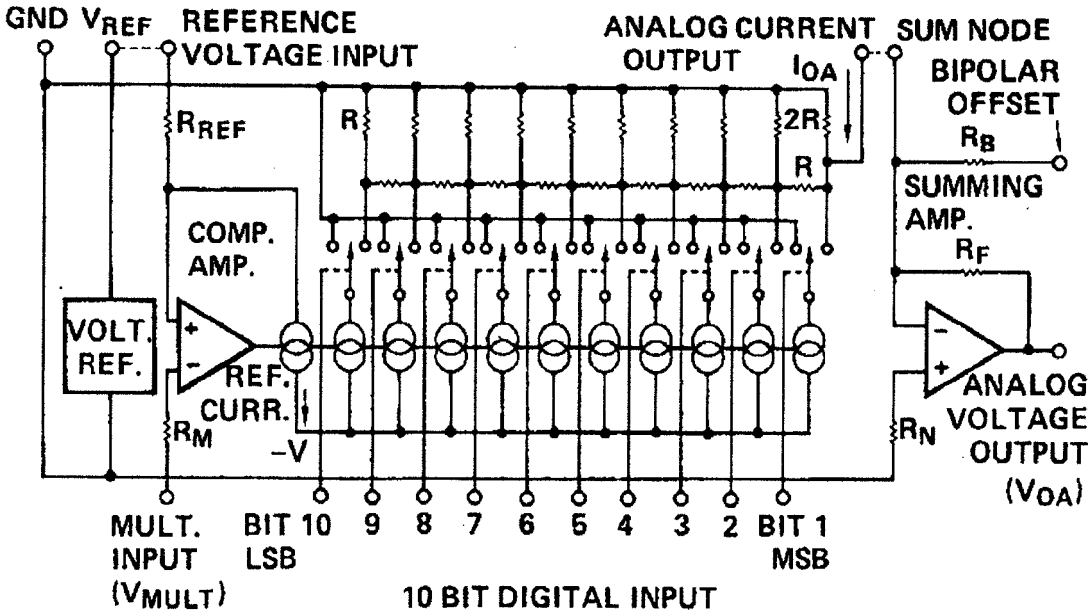
- put the R-2R ladder on the output,
- All current sources can be identical.
- R_E can be large enough to correct for V_{BE} errors while taking up minimal die area. Voltage drop is the same (across R_E) for all bits.

Attenuation-scaling DAC

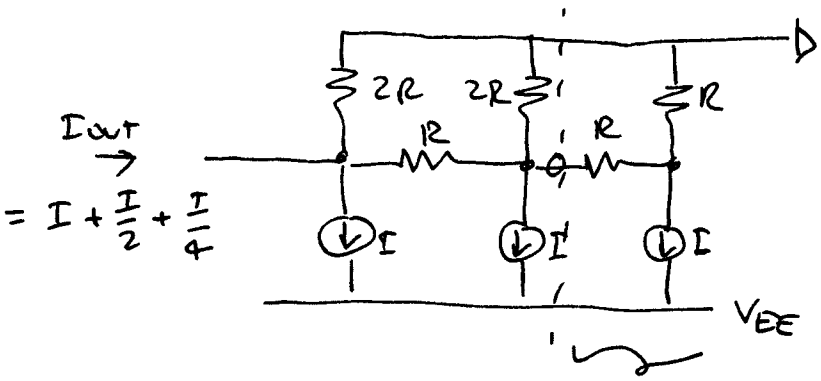


[4] Kelson (1973)

- Early attempt to achieve high-resolution monolithic DAC using binary attenuation network
- (+) Unary current source : better current matching, small chip area
- (-) Non-equal time constant for each bits -> causes distortion



How it works.

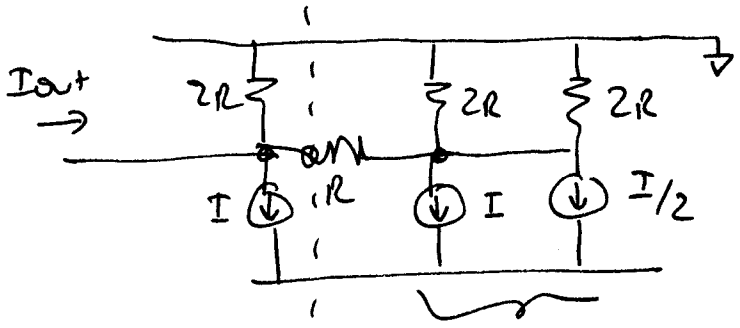


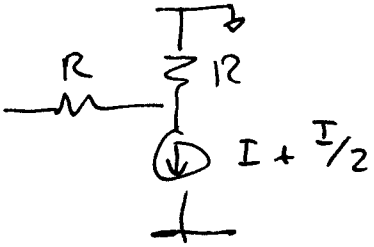
Norton equivalent:

$V_{OC} = -IR$

$I_{SC} = -\frac{I}{2}$

$R_{eq} = 2R$

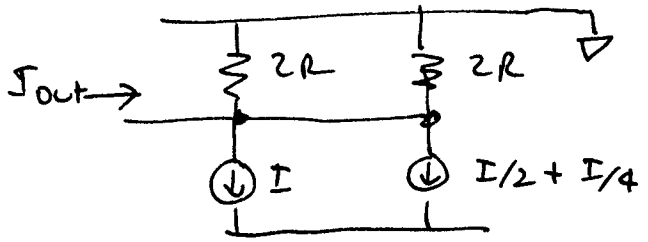




$V_{OC} = -\left(I + I/2\right)R$

$I_{SC} = \frac{I}{2} + \frac{I}{4}$

$R_{eq} = 2R$



DACs based on binary arrays

\+ low complexity

BUT

\- need high accuracy to keep DNL < 1 LSB. can be non-monotonic if not.

suppose MSB = 1
all other bits = 0
} for example 1000

Then switch MSB off and all LSB's on: 0111

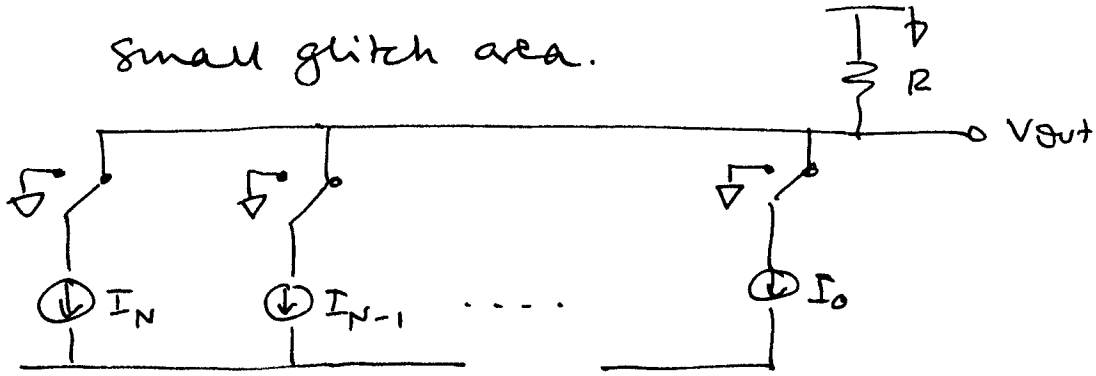
This can create DNL > 1 LSB

also glitch area can be large even if monotonic. You are switching $I = 2^m I_0$

Segmented DAC with thermometer code.

high complexity but always monotonic

small glitch area.



$2^m - 1$ current sources for m bits

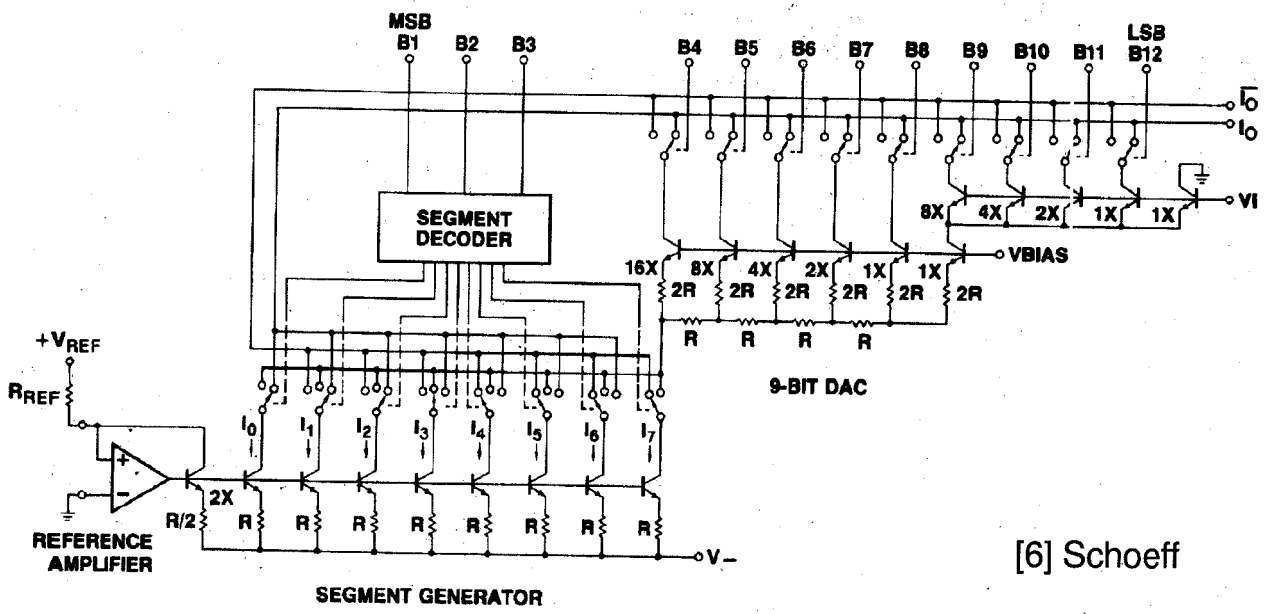
large output capacitance

So, combine the two ideas!

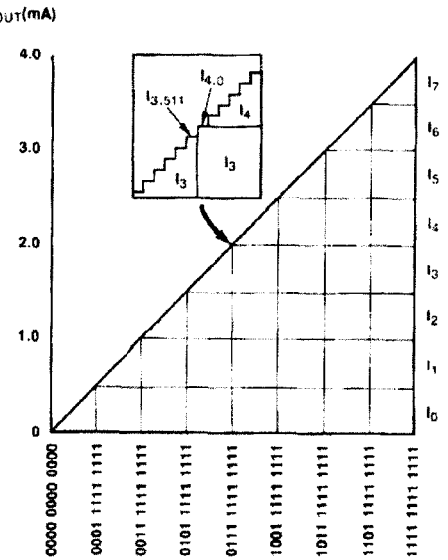
use binary DAC for fine increments

segmented DAC for larger currents.

Segmented DAC



[6] Schoeff



- Use of thermometer code – Inherently monotonic
- Partial use of current scaling
- Good trade-off between complexity, accuracy and speed. Can also be used with attenuation scaling

Spurs - harmonically related. INL, DNL are static measures
- caused by dynamic nonlinearities
- SFDR typically falls off rapidly as signal frequency increases
- increasing the number of bits lowers the quantization noise floor but has little effect on SFDR.

where do these come from?

Code dependencies

settling time. (R/2R ladders for example)

switch feed thru
- switches not sized in proportion to current

timing skew of digital control signals

major carry glitches

current source voltage glitches

nonlinear capacitances (drain, source)

device mismatches —
variation in V_{TH} causes switching uncertainty - code dependent

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Ref. A. Bugeja et al, "A 14-b, 100MS/s CMOS DAC Designed for Spectral Performance," JSSC Vol 34, # 12, pp1719-1732, Dec. 1999.

How do we minimize these defects?

1. Add T/H to output.

output sampled only after DAC has settled
hold output constant.

This eliminates DAC dynamic nonlinearity and performance should approach static limit for ideal TH.

BUT

TH often worse than the DAC as far as dynamic nonlin. is concerned!

These have been discussed already.

So, this approach is not used for high speed DACs.

NRZ vs RZ spectra

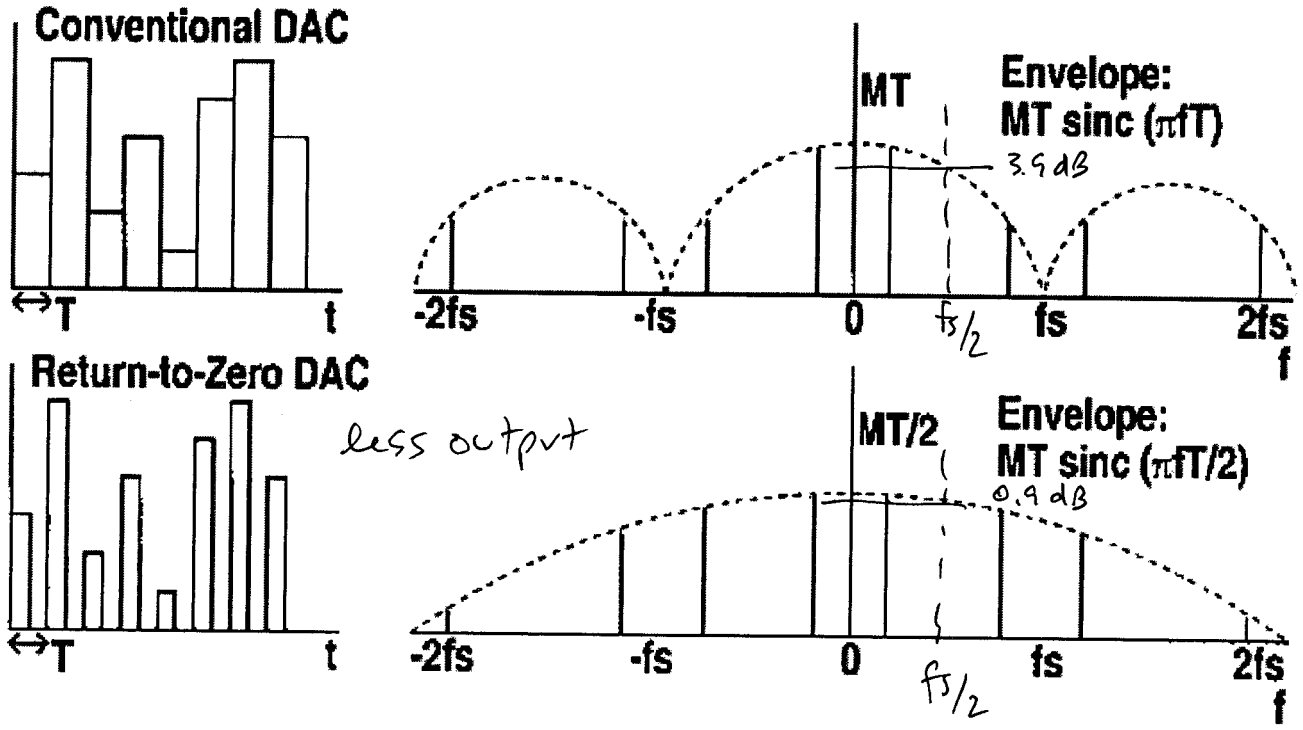


Fig. 5. Spectral comparison.

A. Bugeja, et al., "A 14-b, 100 MS/s CMOS DAC Designed for Spectral Performance," IEEE JSSC, Vol 34, #12,
B. pp. 1719-1731, Dec. 1999.

RZ DAC Schematic

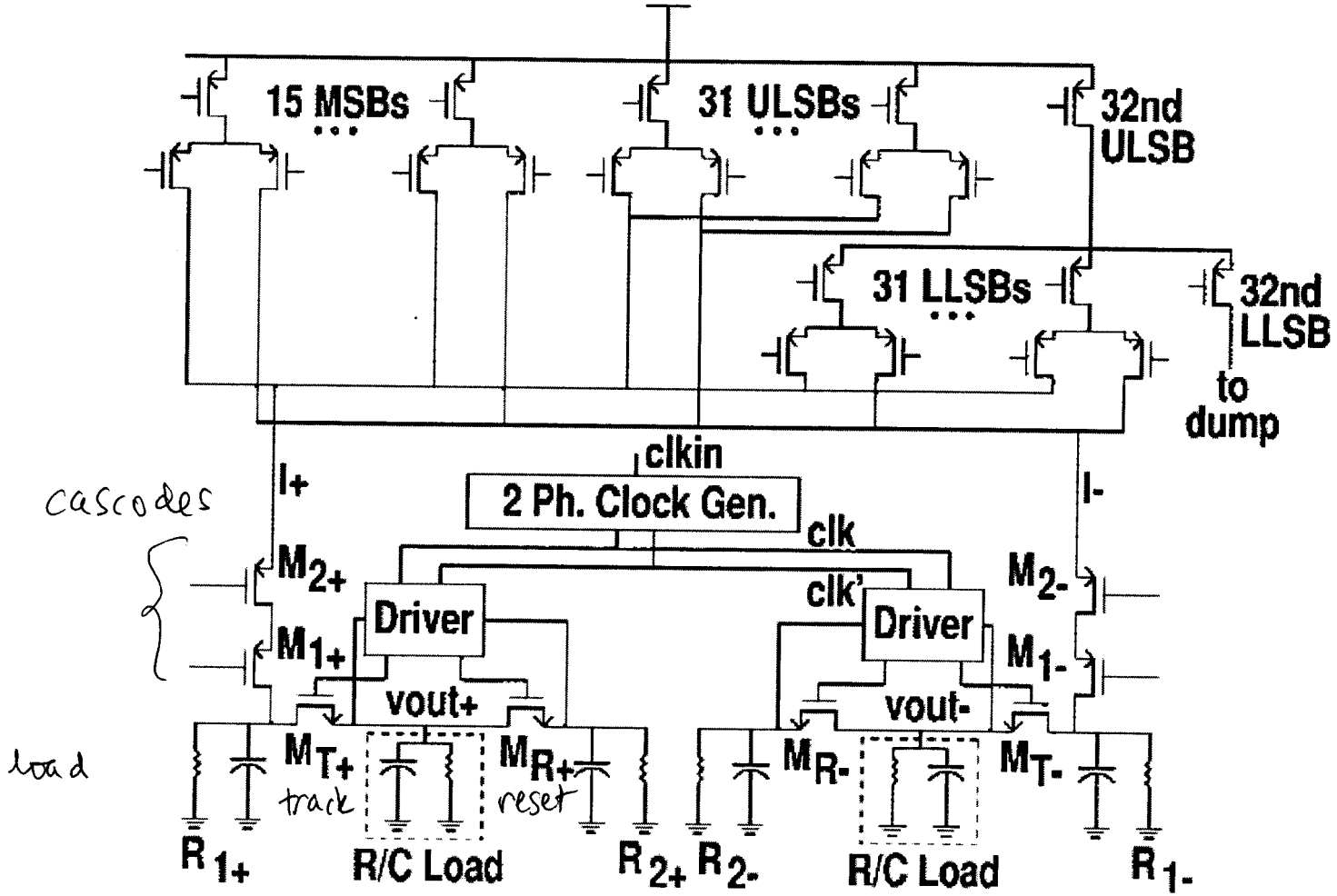


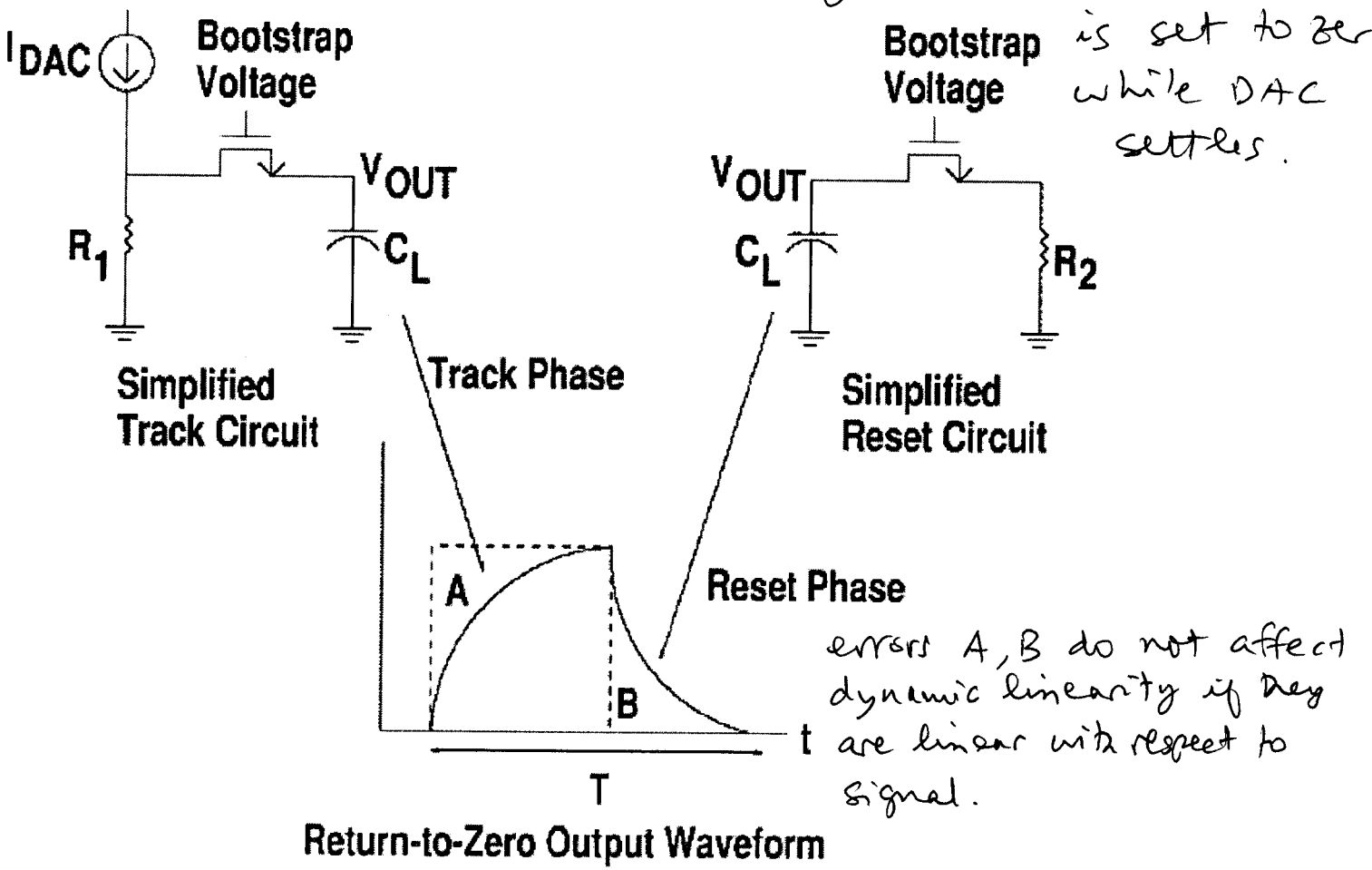
Fig. 3. Return-to-zero high-speed DAC.

A. Bugeja, et al., "A 14-b, 100 MS/s CMOS DAC Designed for Spectral Performance," IEEE JSSC, Vol 34, #12,
B. pp. 1719-1731, Dec. 1999.

RZ operation

Track switch active after DAC has settled.

precedes current switch of next cycle so output is set to zero while DAC settles.



errors A, B do not affect dynamic linearity if they are linear with respect to signal.

A. Bugeja, et al., "A 14-b, 100 MS/s CMOS DAC Designed for Spectral Performance," IEEE JSSC, Vol 34, #12,
B. pp. 1719-1731, Dec. 1999.

RZ has less charge injection than the track-hold

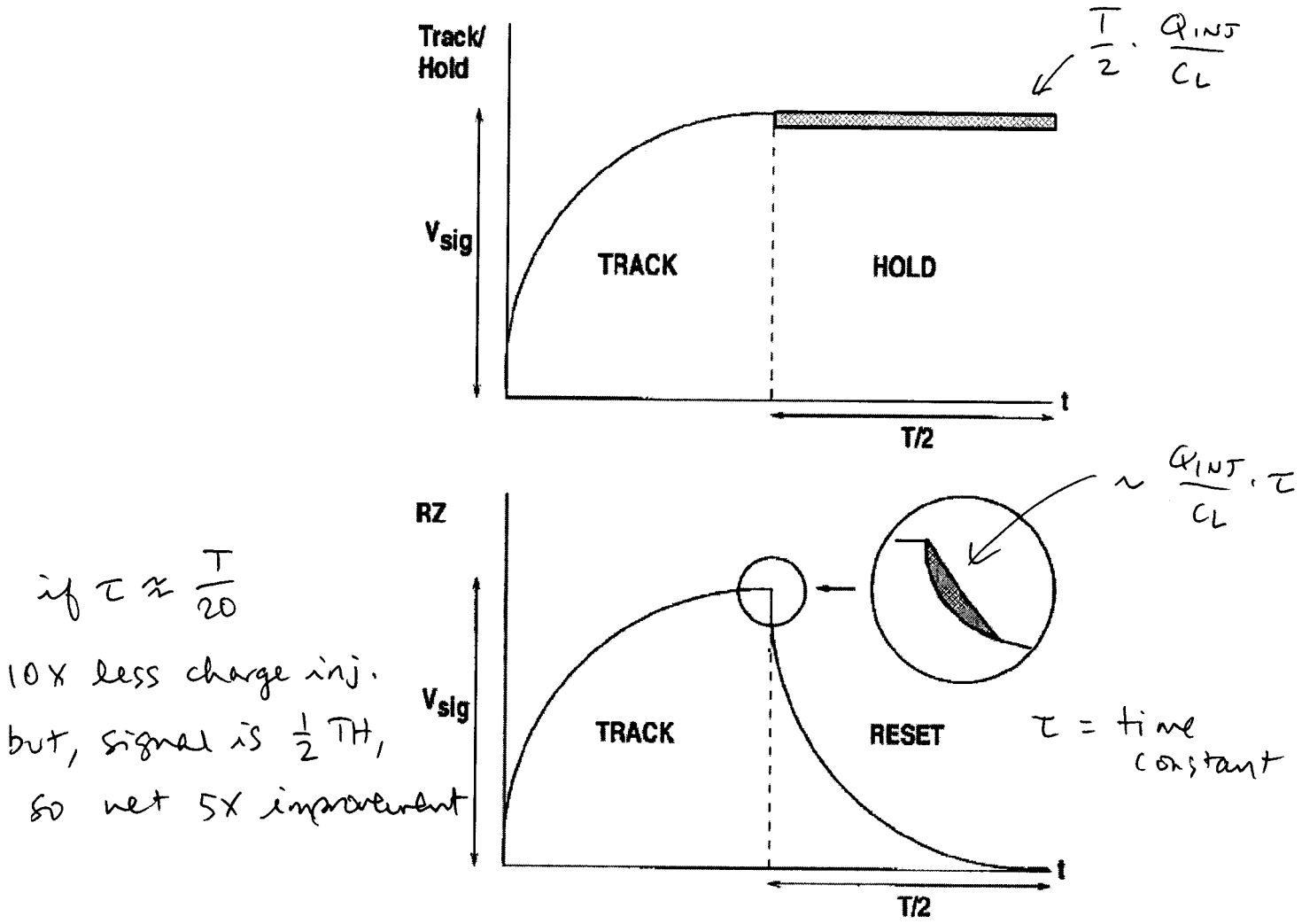


Fig. 6. RZ versus track/hold.

A. Bugeja, et al., "A 14-b, 100 MS/s CMOS DAC Designed for Spectral Performance," IEEE JSSC, Vol 34, #12,
B. pp. 1719-1731, Dec. 1999.

6.1 A 1.2GS/s 15b DAC for Precision Signal Generation

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DAC sample rates over 1GHz with low spurious levels will enable new applications, particularly in signal simulation test equipment. Hundreds of MHz are needed in radar simulations, while predistortion in communication channels may require five times the nominal transmit bandwidth to cover 5th-order products, spreading out to over 100MHz. This circuit was designed to meet the simultaneous requirements of very wide signal bandwidth and high dynamic range.

In Fig. 6.1.1, two data ports at 600MS/s are multiplexed together for a 1200MS/s data stream. The nine LSBs switch nine unit current sources to the taps of a differential R/2R ladder. The six MSBs are decoded into 64 current request signals which are pseudo-randomly scrambled for dynamic element matching (DEM) of the 64MSB unit currents, which are added to the output of the R/2R ladder. In optional modes, a single port can accept data at up to 1200MS/s and the DEM can be disabled to allow a trade-off between DNL and noise. The input receivers accept either LVDS- or ECL-level signals at 1200MHz. MOS source followers level shift the inputs to a more positive common-mode voltage, and the signal is then applied to a bipolar differential pair.

For data alignment, the on-chip data phase detector generates an early/late indication of whether the internal latch clock is centered in the data eye. The early/late data phase detector is similar to a design by Alexander[1]. A separate input flip-flop is clocked with a 180-degree clock at the data transition. If the data captured before and after that transition are different, the out-of-phase flip-flop will indicate whether the transition was early or late. The indications are latched on the DAC to allow timing adjustment by the data source.

To improve INL and DNL, dynamic element matching of the 64MSB current sources is used. The eight least-significant current request lines, which include the three least-significant MSBs and an extra bit from the LSBs, are applied to one eight-way barrel shifter which is controlled by three pseudo-random bits. The eight output lines for those less-significant MSBs are fanned out, one each to eight additional eight-way barrel shifters, which have as their additional 56 inputs the values of the top three MSBs weighted in the ratio of 8:16:32 to match their significance. Three more pseudo-random bits control the second tier of shifters. Each current source is thus used an equal fraction of the time for any particular input code. The pseudo-random controls are generated from multiple delays of a 1b pseudo-random (PR) sequence that comes in as a 16th bit with the data.

Any mismatch or skew in the timing of either the switching of the current sources or the arrival of the currents at the output results effectively in jitter when DEM is in use or in non-linearity otherwise. For deglitching and precise time alignment of the current switching, resampling allows the data-selected current to settle before it is connected to the output. A single series switch for all of the output current was not linear enough for the target performance, so the resampling is done separately for each current source as shown in Fig. 6.1.2. The unit current source is an NPN transistor with a tail resistor. The data pair switches the current to the left or right upper pair, which are the resamplers, at the start of the clock cycle. During settling, the current is dumped to the positive rail and is then switched to the output R/2R ladder, which is referenced to the positive rail. Since each unit current source has its own output resampler, the linearity of the resampling devices versus the current they are passing is not important [2]. The output waveform after resampling is return-to-zero (RZ) with zero current between the resample times. This reduces the $\sin(x)/x$ roll-off versus a non-return-to-zero (NRZ) waveform, but for better SNR below the Nyquist frequency, a second set of current sources and switches was included. This produces the same RZ waveform delayed by half a clock cycle, the sum gives an NRZ result.

The 5.2×5.9mm² chip, made with 40GHz f_t NPNs and 0.35µm CMOS, is shown in Fig. 6.1.3. The largest features visible are the tail resistor arrays which used a common-centroid structure and were sized for negligible contribution to current-source mismatch compared to the transistor mismatches. The package is a 256-pin ball-grid array. The chip uses 1.6A from the 3.3V main supply and about 110mA from the V_{REF} supply for a total dissipation of about 6W.

Figure 6.1.4 shows the worst-case harmonic versus signal frequency for 1200MHz and 500MHz clocks. At 1200MS/s, harmonics remain below -70dBc up to $f_s/4$ and under –63dBc up to Nyquist, while for the reduced-rate clock, the corresponding harmonic levels are –83dBc and –74dBc respectively.

Figure 6.1.5 shows the noise spectral density (NSD) versus clock rate for a typical chip measured in each case near $f_s/4$. For low clock rates, there is an increase of 3dB/octave as the frequency is reduced, due to a constant RMS noise (from fixed mismatches) in a decreasing Nyquist bandwidth. As the clock rate is increased, a floor is reached at –161dBc/Hz and at a 1200MHz clock rate, it is –159dBc/Hz. The chip operates correctly up to 2000MS/s, but testing was very limited above 1200MHz due to the lack of a suitable data source. INL is shown in Fig. 6.1.6 with DEM off and on. The DNL is improved by over a factor of 3 typically with DEM, but the overall INL acquires a strong third-order component due to switching transients around the data pairs in the current sources.

When the resampling switches are disabled, and the current flows continuously from the data switches to the output, performance on a typical test is degraded by about 6dB. A major benchmark for testing is with a multi-carrier wide-band signal, such as WCDMA. With four occupied 5MHz channels at around 300MHz, the typical ACPR (adjacent channel power ratio) was 73dB for a signal crest factor of 14.7dB. Direct generation in a cellular phone band at 900MHz ($3f_s/4$) is shown in Fig. 6.1.7. With a reduced crest factor of about 8dB, the measured ACPR was 69dB.

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switch (resamp) used to block glitches.
each current has its own switch.
unit identical currents. no linearity problems.
RZ mode gives better HF performance

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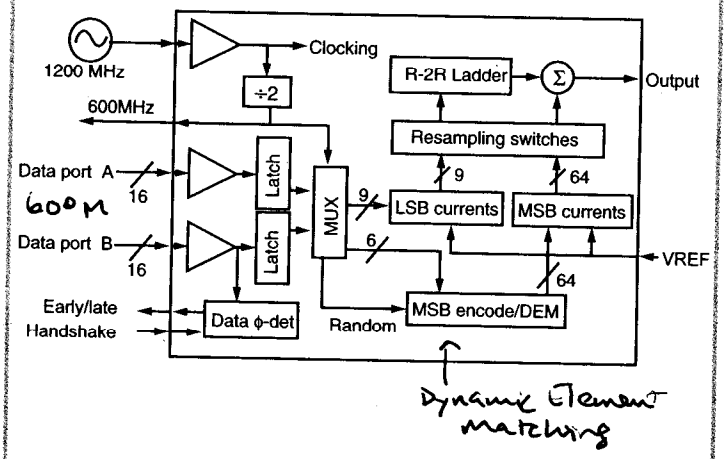

Figure 6.1.1: DAC Block Diagram.

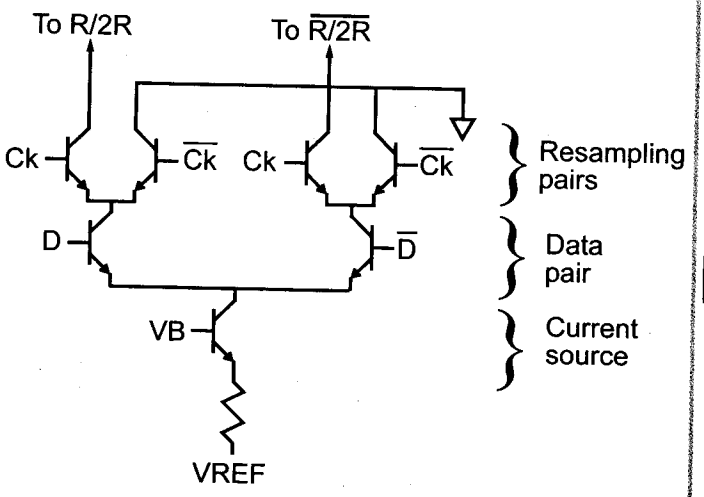

Figure 6.1.2: Current source resampling.

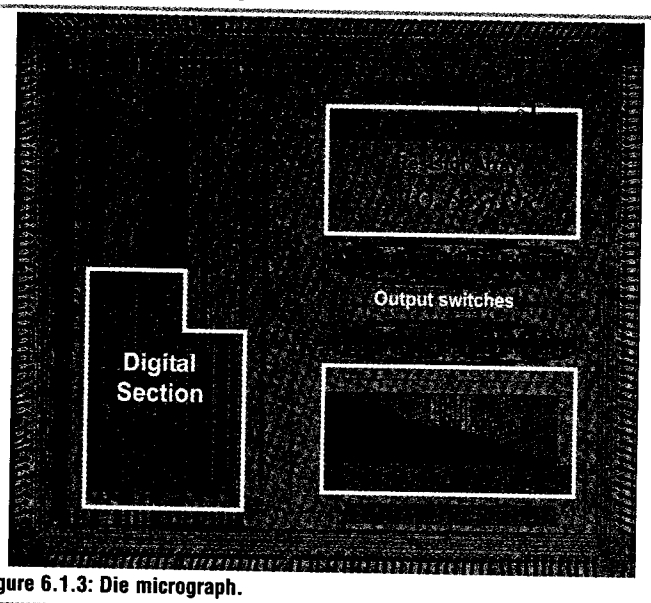

Figure 6.1.3: Die micrograph.

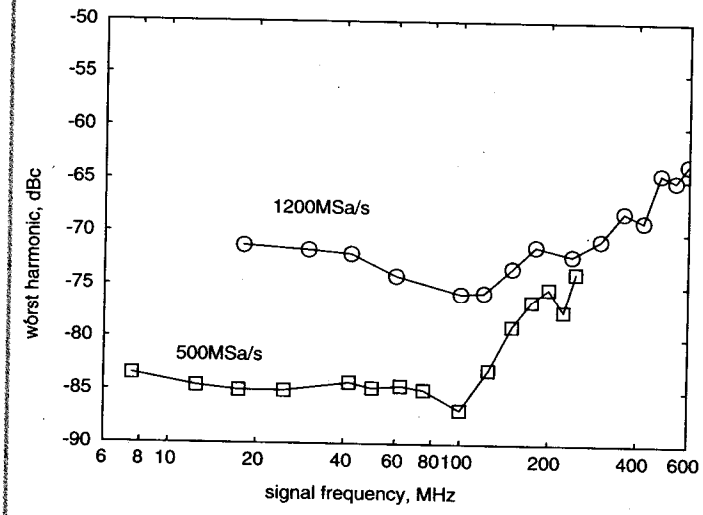

Figure 6.1.4: Worst harmonic versus signal frequency, fs as a parameter.

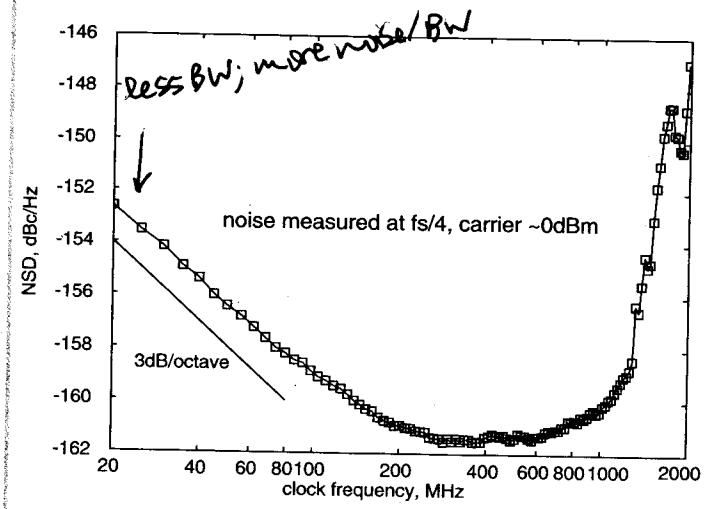

Figure 6.1.5: Noise spectral density versus clock rate.

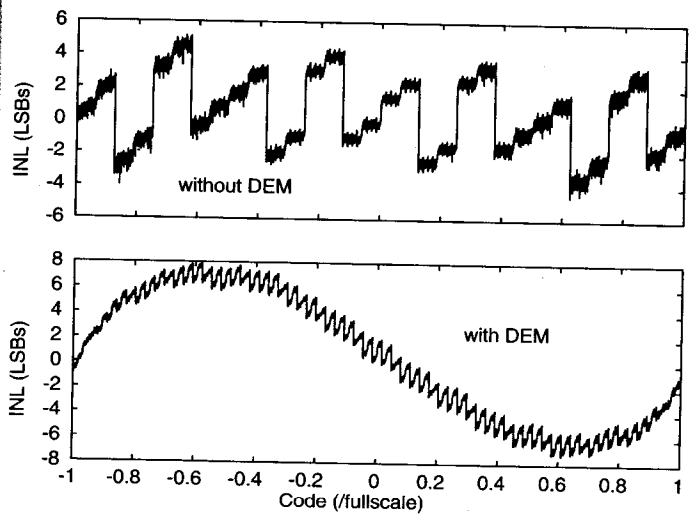

Figure 6.1.6: INL with and without DEM.

Continued on Page 587

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